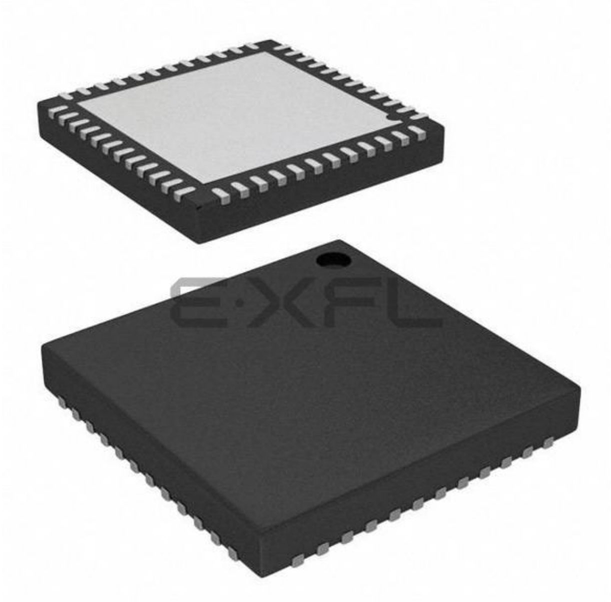

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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART, USB
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	38
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246lti-125t

4.3.1.5 Program Branching Instructions

The 8051 supports a set of conditional and unconditional jump instructions that help to modify the program execution flow. Table 4-5 shows the list of jump instructions.

Table 4-5. Jump Instructions

Mnemonic	Description	Bytes	Cycles
ACALL addr11	Absolute subroutine call	2	4
LCALL addr16	Long subroutine call	3	4
RET	Return from subroutine	1	4
RETI	Return from interrupt	1	4
AJMP addr11	Absolute jump	2	3
LJMP addr16	Long jump	3	4
SJMP rel	Short jump (relative address)	2	3
JMP @A + DPTR	Jump indirect relative to DPTR	1	5
JZ rel	Jump if accumulator is zero	2	4
JNZ rel	Jump if accumulator is nonzero	2	4
CJNE A,Direct, rel	Compare direct byte to accumulator and jump if not equal	3	5
CJNE A, #data, rel	Compare immediate data to accumulator and jump if not equal	3	4
CJNE Rn, #data, rel	Compare immediate data to register and jump if not equal	3	4
CJNE @Ri, #data, rel	Compare immediate data to indirect RAM and jump if not equal	3	5
DJNZ Rn,rel	Decrement register and jump if not zero	2	4
DJNZ Direct, rel	Decrement direct byte and jump if not zero	3	5
NOP	No operation	1	1

4.4 DMA and PHUB

The PHUB and the DMA controller are responsible for data transfer between the CPU and peripherals, and also data transfers between peripherals. The PHUB and DMA also control device configuration during boot. The PHUB consists of:

- A central hub that includes the DMA controller, arbiter, and router
- Multiple spokes that radiate outward from the hub to most peripherals

There are two PHUB masters: the CPU and the DMA controller. Both masters may initiate transactions on the bus. The DMA channels can handle peripheral communication without CPU intervention. The arbiter in the central hub determines which DMA channel is the highest priority if there are multiple requests.

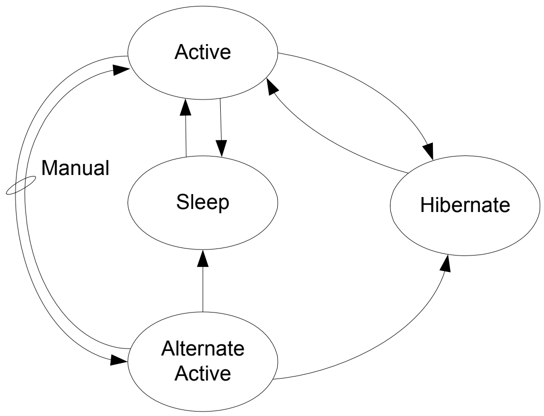
4.4.1 PHUB Features

- CPU and DMA controller are both bus masters to the PHUB
- Eight Multi-layer AHB Bus parallel access paths (spokes) for peripheral access
- Simultaneous CPU and DMA access to peripherals located on different spokes
- Simultaneous DMA source and destination burst transactions on different spokes
- Supports 8, 16, 24, and 32-bit addressing and data

Table 4-6. PHUB Spokes and Peripherals

PHUB Spokes	Peripherals
0	SRAM
1	IOs, PICU, EMIF
2	PHUB local configuration, Power manager, Clocks, IC, SWV, EEPROM, Flash programming interface
3	Analog interface and trim, Decimator
4	USB, USB, I^2C, Timers, Counters, and PWMs
5	Reserved
6	UDBs group 1
7	UDBs group 2

Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 µs is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins - no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and Precision Reset (PRES).

6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar panels or single cell battery supplies, may use the on-chip boost converter to generate a minimum of 1.8 V supply voltage. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides such as driving 5.0 V LCD glass in a 3.3 V system. With the addition of an inductor, Schottky diode, and capacitors, it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage V_{BAT} from 0.5 V to 3.6 V, and can start up with V_{BAT} as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (V_{OUT}) in 100 mV increments. V_{BAT} is typically less than V_{OUT}; if V_{BAT} is greater than or equal to V_{OUT}, then V_{OUT} will be slightly less than V_{BAT} due to resistive losses in the boost converter. The block can deliver up to 50 mA (I_{BOOST}) depending on configuration to both the PSoC device and external components. The sum of all current sinks in the design including the PSoC device, PSoC I/O pin loads, and external component loads must be less than the I_{BOOST} specified maximum current.

Four pins are associated with the boost converter: VBAT, VSSB, VBOOST, and IND. The boosted output voltage is sensed at the VBOOST pin and must be connected directly to the chip's supply inputs, VDDA, VDDD, and VDDIO, if used to power the PSoC device.

The boost converter requires four components in addition to those required in a non-boost design, as shown in Figure 6-6 on page 35. A 22-µF capacitor (CBAT) is required close to the VBAT pin to provide local bulk storage of the battery voltage and provide regulator stability. A diode between the battery and VBAT pin should not be used for reverse polarity protection because the diodes forward voltage drop reduces the V_{BAT} voltage. Between the VBAT and IND pins, an inductor of 4.7 µH, 10 µH, or 22 µH is required. The inductor value can be optimized to increase the boost converter efficiency based on input voltage, output voltage, temperature, and current. Inductor size is determined by following the design guidance in this section and the electrical specifications. The inductor must be placed within 1 cm of the VBAT and IND pins and have a minimum saturation current of 750 mA. Between the IND and VBOOST pins, place a Schottky diode within 1 cm of the pins. This diode shall have a forward current rating of at least 1.0 A and a reverse voltage of at least 20 V. Connect a 22-µF bulk capacitor (CBOOST) close to VBOOST to provide regulator output stability. It is important to sum the total capacitance connected to the VBOOST pin and ensure the maximum CBOOST specification is not exceeded. All capacitors must be rated for a minimum of 10 V to minimize capacitive losses due to voltage de-rating.

  - Input or output or both for CPU and DMA
  - Eight drive modes
  - Every pin can be an interrupt source configured as rising edge, falling edge or both edges. If required, level sensitive interrupts are supported through the DSI
  - Dedicated port interrupt vector for each port
  - Slew rate controlled digital output drive mode
  - Access port control and configuration registers on either port basis or pin basis
  - Separate port read (PS) and write (DR) data registers to avoid read modify write errors
  - Special functionality on a pin by pin basis
- Additional features only provided on the GPIO pins:
  - LCD segment drive on LCD equipped devices
  - CapSense
  - Analog input and output capability
  - Continuous 100 µA clamp current capability
  - Standard drive strength down to 1.7 V
- Additional features only provided on SIO pins:
  - Higher drive strength than GPIO
  - Hot swap capability (5 V tolerance at any operating V_{DD})
  - Programmable and regulated high input and output drive levels down to 1.2 V
  - No analog input, CapSense, or LCD capability
  - Overvoltage tolerance up to 5.5 V
  - SIO can act as a general purpose analog comparator
- USBIO features:
  - Full speed USB 2.0 compliant I/O
  - Highest drive strength for general purpose use
  - Input, output, or both for CPU and DMA
  - Input, output, or both for digital peripherals
  - Digital output (CMOS) drive mode
  - Each pin can be an interrupt source configured as rising edge, falling edge, or both edges

7.1.4 Designing with PSoC Creator

7.1.4.1 More Than a Typical IDE

A successful design tool allows for the rapid development and deployment of both simple and complex designs. It reduces or eliminates any learning curve. It makes the integration of a new design into the production stream straightforward.

PSoC Creator is that design tool.

PSoC Creator is a full featured Integrated Development Environment (IDE) for hardware and software design. It is optimized specifically for PSoC devices and combines a modern, powerful software development platform with a sophisticated graphical design tool. This unique combination of tools makes PSoC Creator the most flexible embedded design platform available.

Graphical design entry simplifies the task of configuring a particular part. You can select the required functionality from an extensive catalog of components and place it in your design. All components are parameterized and have an editor dialog that allows you to tailor functionality to your needs.

PSoC Creator automatically configures clocks and routes the I/O to the selected pins and then generates APIs to give the application complete control over the hardware. Changing the PSoC device configuration is as simple as adding a new component, setting its parameters, and rebuilding the project.

At any stage of development you are free to change the hardware configuration and even the target processor. To retarget your application (hardware and software) to new devices, even from 8- to 32-bit families, just select the new device and rebuild.

You also have the ability to change the C compiler and evaluate an alternative. Components are designed for portability and are validated against all devices, from all families, and against all supported tool chains. Switching compilers is as easy as editing the from the project options and rebuilding the application with no errors from the generated APIs or boot code.

7.1.4.2 Component Catalog

The component catalog is a repository of reusable design elements that select device functionality and customize your PSoC device. It is populated with an impressive selection of content; from simple primitives such as logic gates and device registers, through the digital timers, counters and PWMs, plus analog components such as ADC and DAC, and communication protocols, such as I^2C, and USB. See Example Peripherals on page 45 for more details about available peripherals. All content is fully characterized and carefully documented in datasheets with code examples, AC/DC specifications, and user code ready APIs.

7.1.4.3 Design Reuse

The symbol editor gives you the ability to develop reusable components that can significantly reduce future design time. Just draw a symbol and associate that symbol with your proven design. PSoC Creator allows for the placement of the new symbol anywhere in the component catalog along with the content provided by Cypress. You can then reuse your content as many times as you want, and in any number of projects, without ever having to revisit the details of the implementation.

7.1.4.4 Software Development

Anchoring the tool is a modern, highly customizable user interface. It includes project management and integrated editors for C and assembler source code, as well the design entry tools.

Project build control leverages compiler technology from top commercial vendors such as ARM® Limited, Keil™, and CodeSourcery (GNU). Free versions of Keil C51 and GNU C Compiler (GCC) for ARM, with no restrictions on code size or end product distribution, are included with the tool distribution. Upgrading to more optimizing compilers is a snap with support for the professional Keil C51 product and ARM RealView™ compiler.

7.1.4.5 Nonintrusive Debugging

With JTAG (4-wire) and SWD (2-wire) debug connectivity available on all devices, the PSoC Creator debugger offers full control over the target device with minimum intrusion. Breakpoints and code execution commands are all readily available from toolbar buttons and an impressive lineup of windows—register, locals, watch, call stack, memory and peripherals—make for an unparalleled level of visibility into the system.

PSoC Creator contains all the tools necessary to complete a design, and then to maintain and extend that design for years to come. All steps of the design flow are carefully integrated and optimized for ease-of-use and to maximize productivity.

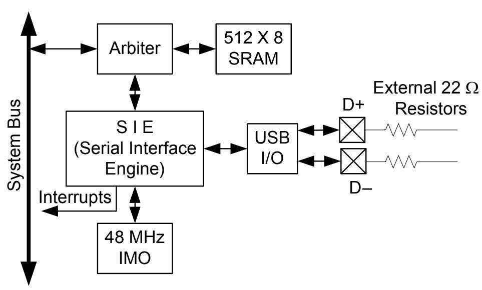
7.5 USB

PSoC includes a dedicated Full-Speed (12 Mbps) USB 2.0 transceiver supporting all four USB transfer types: control, interrupt, bulk, and isochronous. PSoC Creator provides full configuration support. USB interfaces to hosts through two dedicated USBIO pins, which are detailed in the "I/O System and Routing" section on page 37.

USB includes the following features:

- Eight unidirectional data endpoints
- One bidirectional control endpoint 0 (EP0)
- Shared 512-byte buffer for the eight data endpoints
- Dedicated 8-byte buffer for EP0
- Three memory modes
  - Manual Memory Management with No DMA Access
  - Manual Memory Management with Manual DMA Access
  - Automatic Memory Management with Automatic DMA Access
- Internal 3.3 V regulator for transceiver
- Internal 48 MHz main oscillator mode that auto locks to USB bus clock, requiring no external crystal for USB (USB equipped parts only)
- Interrupts on bus and each endpoint event, with device wakeup
- USB Reset, Suspend, and Resume operations
- Bus powered and self powered modes

Figure 7-14. USB



7.6 Timers, Counters, and PWMs

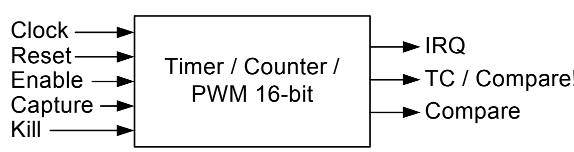
The Timer/Counter/PWM peripheral is a 16-bit dedicated peripheral providing three of the most common embedded peripheral features. As almost all embedded systems use some combination of timers, counters, and PWMs. Four of them have been included on this PSoC device family. Additional and more advanced functionality timers, counters, and PWMs can also be instantiated in Universal Digital Blocks (UDBs) as required. PSoC Creator allows you to choose the timer, counter, and PWM features that they require. The tool set utilizes the most optimal resources available.

The Timer/Counter/PWM peripheral can select from multiple clock sources, with input and output signals connected through the DSI routing. DSI routing allows input and output connections to any device pin and any internal digital signal accessible through the DSI. Each of the four instances has a compare output, terminal count output (optional complementary compare output), and programmable interrupt request line. The Timer/Counter/PWMs are configurable as free running, one shot, or Enable input controlled. The peripheral has timer reset and capture inputs, and a kill input for control of the comparator outputs. The peripheral supports full 16-bit capture.

Timer/Counter/PWM features include:

- 16-bit Timer/Counter/PWM (down count only)
- Selectable clock source
- PWM comparator (configurable for LT, LTE, EQ, GTE, GT)
- Period reload on start, reset, and terminal count
- Interrupt on terminal count, compare true, or capture
- Dynamic counter reads
- Timer capture mode
- Count while enable signal is asserted mode
- Free run mode
- One Shot mode (stop at end of period)
- Complementary PWM outputs with deadband
- PWM output kill

Figure 7-15. Timer/Counter/PWM

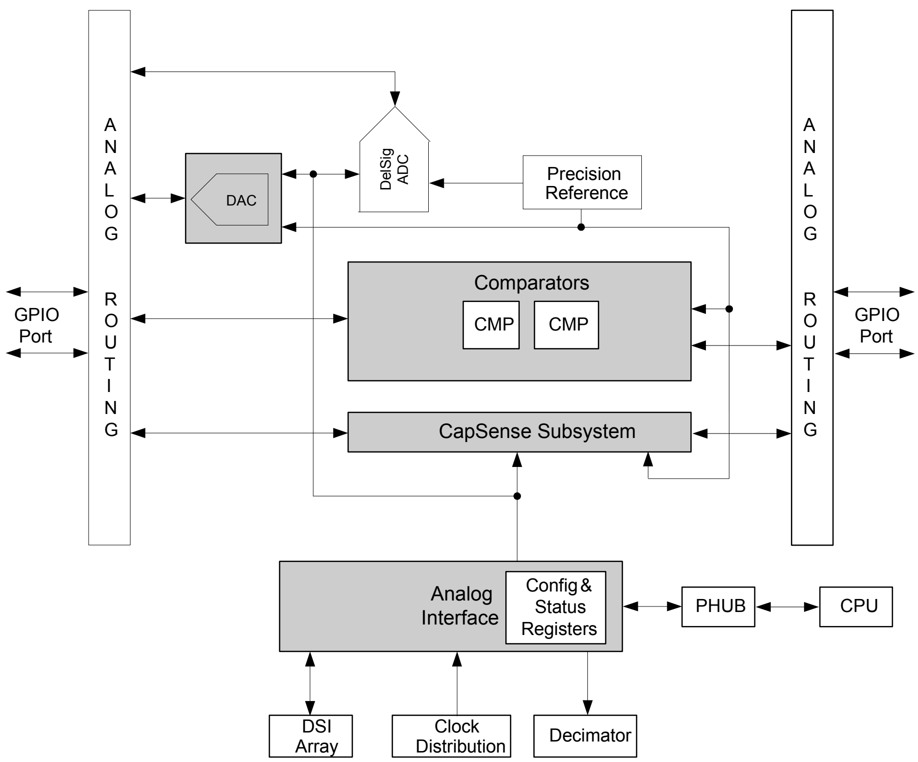


8. Analog Subsystem

The analog programmable system creates application specific combinations of both standard and advanced analog signal processing blocks. These blocks are then interconnected to each other and also to any pin on the device, providing a high level of design flexibility and IP security. The features of the analog subsystem are outlined here to provide an overview of capabilities and architecture.

- Flexible, configurable analog routing architecture provided by analog globals, analog mux bus, and analog local buses.
- High resolution delta-sigma ADC.
- One 8-bit DAC that provides either voltage or current output.
- Two comparators with optional connection to configurable LUT outputs.
- CapSense subsystem to enable capacitive touch sensing.
- Precision reference for generating an accurate analog voltage for internal analog blocks.

Figure 8-1. Analog Subsystem Block Diagram



The PSoC Creator software program provides a user friendly interface to configure the analog connections between the GPIO and various analog resources and connections from one analog resource to another. PSoC Creator also provides component libraries that allow you to configure the various analog blocks to perform application specific functions. The tool also generates API interface libraries that allow you to write firmware that allows the communication between the analog peripheral and CPU/Memory.

Figure 11-11. Efficiency vs V_{BAT}, L_{BOOST} = 4.7 µH [35]

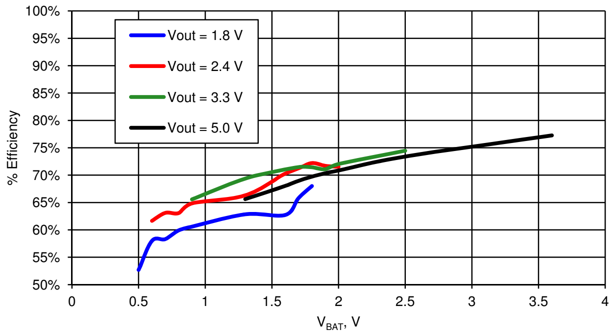


Figure 11-12. Efficiency vs V_{BAT}, L_{BOOST} = 10 µH [35]

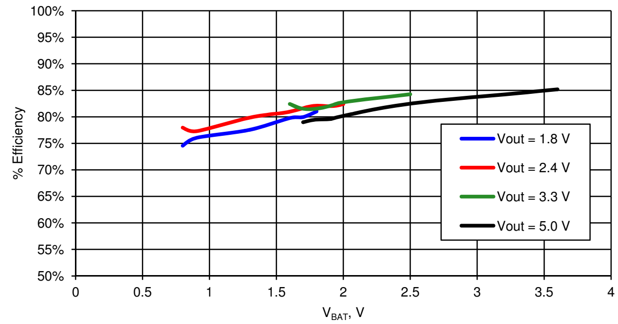


Figure 11-13. Efficiency vs V_{BAT}, L_{BOOST} = 22 µH [35]

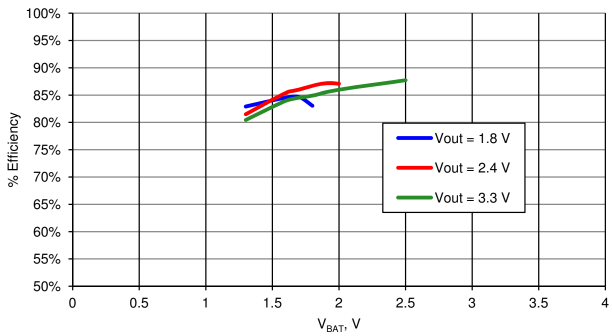
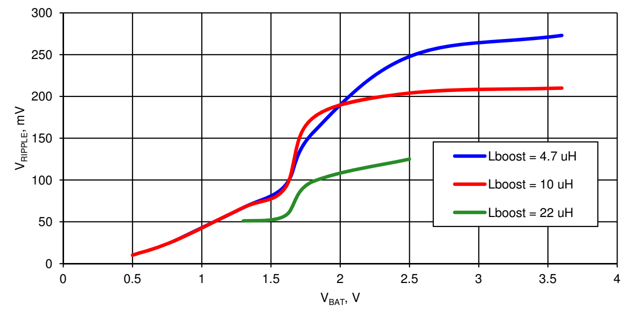


Figure 11-14. V_{RIPPLE} vs V_{BAT} [35]



Note

35. Typical example. Actual values may vary depending on external component selection, PCB layout, and other design parameters.

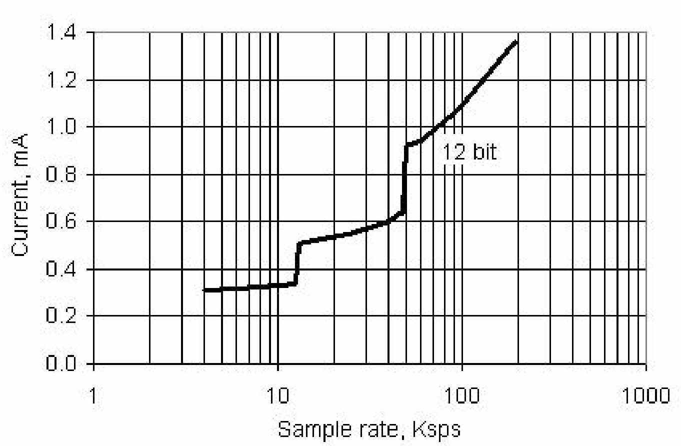
Table 11-20. Delta-sigma ADC AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Startup time		–	–	4	Samples
THD	Total harmonic distortion[48]	Buffer gain = 1, 12-bit, Range = ±1.024 V	–	–	0.0032	%
12-Bit Resolution Mode						
SR12	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	4	–	192	ksps
BW12	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	44	–	kHz
SINAD12int	Signal to noise ratio, 12-bit, internal reference[48]	Range = ±1.024 V, unbuffered	66	–	–	dB
8-Bit Resolution Mode						
SR8	Sample rate, continuous, high power[48]	Range = ±1.024 V, unbuffered	8	–	384	ksps
BW8	Input bandwidth at max sample rate[48]	Range = ±1.024 V, unbuffered	–	88	–	kHz
SINAD8int	Signal to noise ratio, 8-bit, internal reference[48]	Range = ±1.024 V, unbuffered	43	–	–	dB

Table 11-21. Delta-sigma ADC Sample Rates, Range = ±1.024 V

Resolution, Bits	Continuous		Multi-Sample	
	Min	Max	Min	Max
8	8000	384000	1911	91701
9	6400	307200	1543	74024
10	5566	267130	1348	64673
11	4741	227555	1154	55351
12	4000	192000	978	46900

Figure 11-25. Delta-sigma ADC IDD vs sps, Range = ±1.024 V, Continuous Sample Mode, Input Buffer Bypassed



Note
48. Based on device characterization (Not production tested).

11.5.2 Voltage Reference

Table 11-22. Voltage Reference Specifications

See also ADC external reference specifications in *Section 11.5.1*.

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{REF}	Precision reference voltage	Initial trimming, 25 °C	1.014 (–1%)	1.024	1.034 (+1%)	V

11.5.3 Analog Globals

Table 11-23. Analog Globals Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Rppag	Resistance pin-to-pin through P2[4], AGL0, DSM INP, AGL1, P2[5][49]	V_{DDA} = 3 V	–	1472	2200	Ω
Rppmuxbus	Resistance pin-to-pin through P2[3], amuxbusL, P2[4][49]	V_{DDA} = 3 V	–	706	1100	Ω

11.5.4 Comparator

Table 11-24. Comparator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OS}	Input offset voltage in fast mode	Factory trim, V_{DDA} > 2.7 V, $V_{IN} \geq 0.5$ V	–		10	mV
	Input offset voltage in slow mode	Factory trim, $V_{IN} \geq 0.5$ V	–		9	mV
	Input offset voltage in fast mode[50]	Custom trim	–	–	4	mV
	Input offset voltage in slow mode[50]	Custom trim	–	–	4	mV
	Input offset voltage in ultra low-power mode	$V_{DDA} \leq 4.6$ V	–	±12	–	mV
V_{HYST}	Hysteresis	Hysteresis enable mode	–	10	32	mV
V_{ICM}	Input common mode voltage	High current / fast mode	V_{SSA}	–	V_{DDA}	V
		Low current / slow mode	V_{SSA}	–	V_{DDA}	V
		Ultra low power mode $V_{DDA} \leq 4.6$ V	V_{SSA}	–	V_{DDA} – 1.15	
CMRR	Common mode rejection ratio		–	50	–	dB
I_{CMP}	High current mode/fast mode[51]		–	–	400	µA
	Low current mode/slow mode[51]		–	–	100	µA
	Ultra low-power mode[51]	$V_{DDA} \leq 4.6$ V	–	6	–	µA

Table 11-25. Comparator AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Tresp	Response time, high current mode[51]	50 mV overdrive, measured pin-to-pin	–	75	110	ns
	Response time, low current mode[51]	50 mV overdrive, measured pin-to-pin	–	155	200	ns
	Response time, ultra low-power mode[51]	50 mV overdrive, measured pin-to-pin, $V_{DDA} \leq 4.6$ V	–	55	–	µs

Notes

49. The resistance of the analog global and analog mux bus is high if $V_{DDA} \leq 2.7$ V, and the chip is in either sleep or hibernate mode. Use of analog global and analog mux bus under these conditions is not recommended
50. The recommended procedure for using a custom trim value for the on-chip comparators can be found in the TRM.
51. Based on device characterization (Not production tested).

Table 11-26. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Source Mode

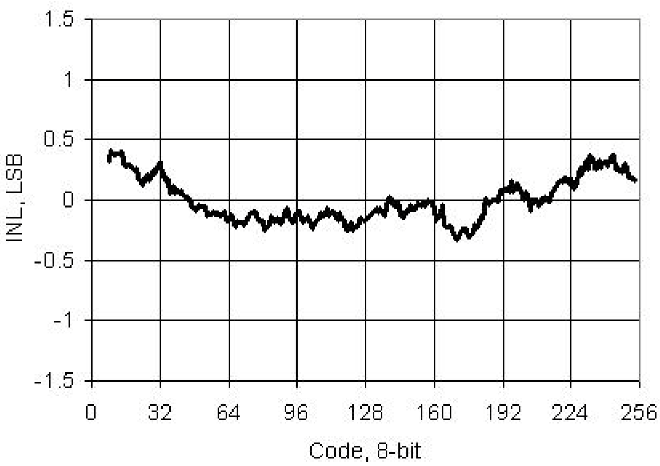
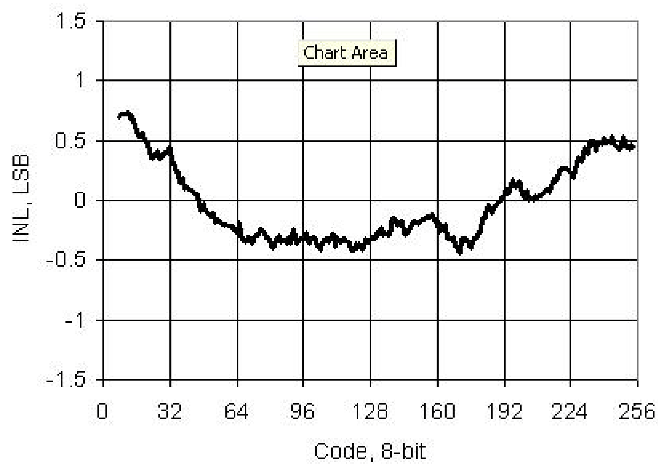


Figure 11-27. IDAC INL vs Input Code, Range = 255 µA, Sink Mode



11.5.6 Voltage Digital to Analog Converter (VDAC)

See the VDAC component datasheet in PSoC Creator for full electrical specifications and APIs.

Unless otherwise specified, all charts and graphs show typical values.

Table 11-28. VDAC DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Resolution		–	8	–	bits
INL1	Integral nonlinearity	1 V scale	–	±2.1	±2.5	LSB
INL4	Integral nonlinearity[52]	4 V scale	–	±2.1	±2.5	LSB
DNL1	Differential nonlinearity	1 V scale	–	±0.3	±1	LSB
DNL4	Differential nonlinearity[52]	4 V scale	–	±0.3	±1	LSB
Rout	Output resistance	1 V scale	–	4	–	kΩ
		4 V scale	–	16	–	kΩ
V_{OUT}	Output voltage range, code = 255	1 V scale	–	1.02	–	V
		4 V scale, V_{DDA} = 5 V	–	4.08	–	V
	Monotonicity		–	–	Yes	–
V_{OS}	Zero scale error		–	0	±0.9	LSB
Eg	Gain error	1 V scale	–	–	±2.5	%
		4 V scale	–	–	±2.5	%
TC_Eg	Temperature coefficient, gain error	1 V scale	–	–	0.03	%FSR / °C
		4 V scale	–	–	0.03	%FSR / °C
I_{DD}	Operating current	Low speed mode	–	–	100	µA
		High speed mode	–	–	500	µA

Figure 11-40. VDAC INL vs Input Code, 1 V Mode

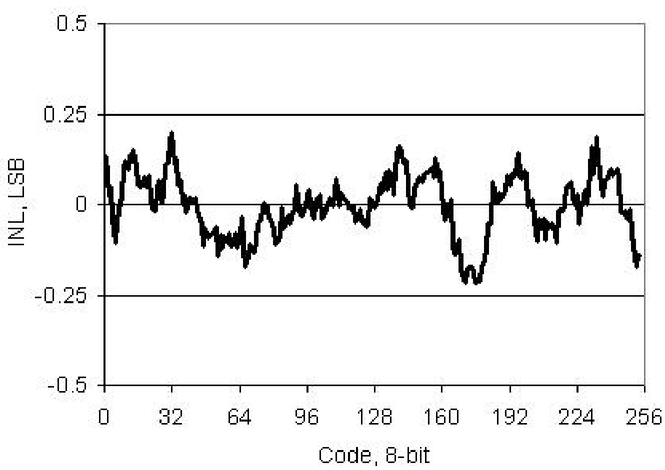
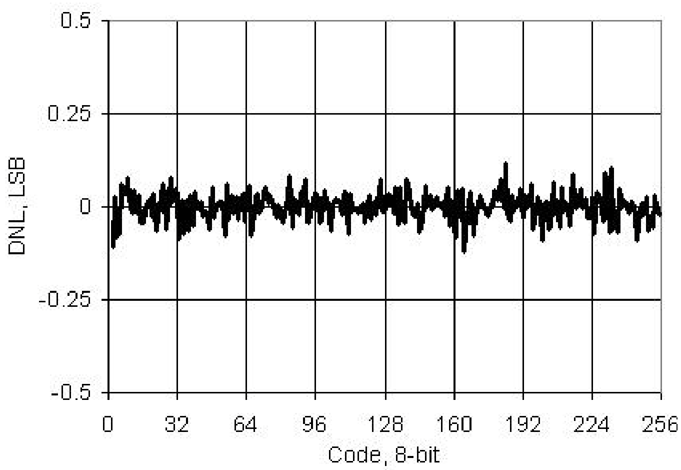


Figure 11-41. VDAC DNL vs Input Code, 1 V Mode



Note

52. Based on device characterization (Not production tested).

Table 11-29. VDAC AC Specifications t

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{DAC}	Update rate	1 V scale	–	–	1000	ksps
		4 V scale	–	–	250	ksps
TsettleP	Settling time to 0.1%, step 25% to 75%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.8	3.2	µs
TsettleN	Settling time to 0.1%, step 75% to 25%	1 V scale, Cload = 15 pF	–	0.45	1	µs
		4 V scale, Cload = 15 pF	–	0.7	3	µs
	Voltage noise	Range = 1 V, High speed mode, V_{DDA} = 5 V, 10 kHz	–	750	–	nV/sqrtHz

Figure 11-48. VDAC Step Response, Codes 0x40 - 0xC0, 1 V Mode, High speed mode, V_{DDA} = 5 V

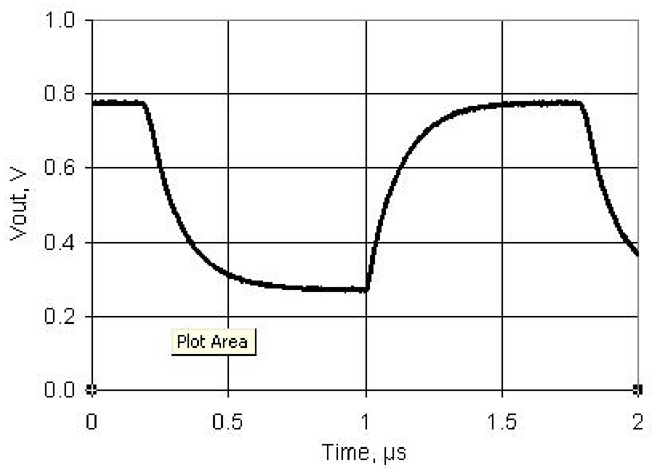


Figure 11-49. VDAC Glitch Response, Codes 0x7F - 0x80, 1 V Mode, High speed mode, V_{DDA} = 5 V

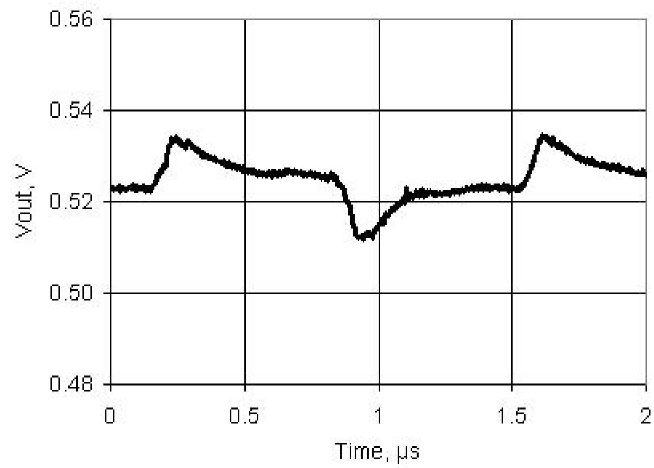


Figure 11-50. VDAC PSRR vs Frequency

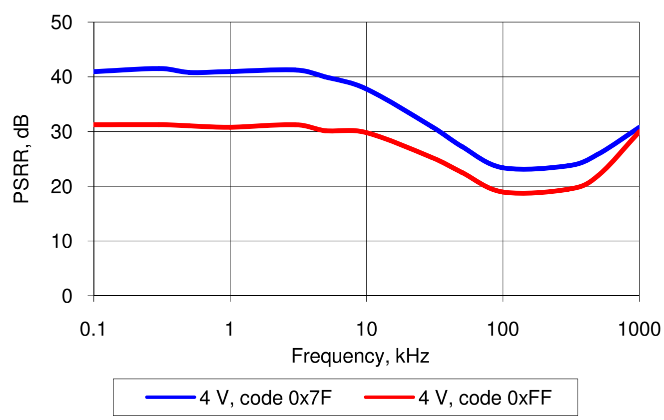
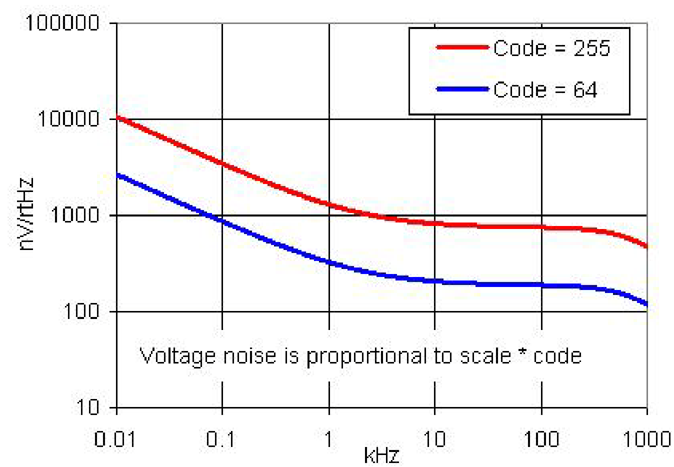


Figure 11-51. VDAC Voltage Noise, 1 V Mode, High speed mode, V_{DDA} = 5 V



11.6 Digital Peripherals

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.6.1 Timer

The following specifications apply to the Timer/Counter/PWM peripheral in timer mode. Timers can also be implemented in UDBs; for more information, see the Timer component datasheet in PSoC Creator.

Table 11-33. Timer DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit timer, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-34. Timer AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	50.01	MHz
	Capture pulse width (Internal)		21	–	–	ns
	Capture pulse width (external)		42	–	–	ns
	Timer resolution		21	–	–	ns
	Enable pulse width		21	–	–	ns
	Enable pulse width (external)		42	–	–	ns
	Reset pulse width		21	–	–	ns
	Reset pulse width (external)		42	–	–	ns

11.6.2 Counter

The following specifications apply to the Timer/Counter/PWM peripheral, in counter mode. Counters can also be implemented in UDBs; for more information, see the Counter component datasheet in PSoC Creator.

Table 11-35. Counter DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Block current consumption	16-bit counter, at listed input clock frequency	–	–	–	µA
	3 MHz		–	15	–	µA
	12 MHz		–	60	–	µA
	50 MHz		–	260	–	µA

Table 11-36. Counter AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
	Operating frequency		DC	–	50.01	MHz
	Capture pulse		21	–	–	ns
	Resolution		21	–	–	ns
	Pulse width		21	–	–	ns
	Pulse width (external)		42	–	–	ns
	Enable pulse width		21	–	–	ns
	Enable pulse width (external)		42	–	–	ns
	Reset pulse width		21	–	–	ns
	Reset pulse width (external)		42	–	–	ns

Figure 11-55. Synchronous Read Cycle Timing

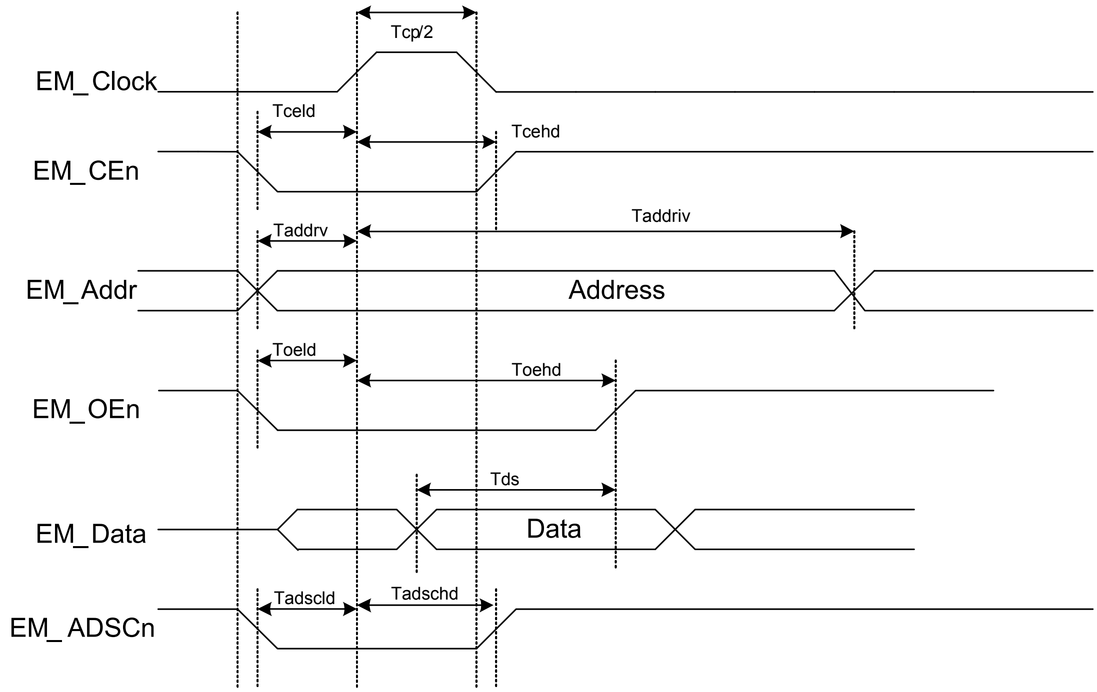


Table 11-55. Synchronous Read Cycle Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
T	EMIF clock period[62]	$V_{DDA} \geq 3.3$ V	30.3	–	–	ns
Tcp/2	EM_Clock pulse high		T/2	–	–	ns
Tceld	EM_CEn low to EM_Clock high		5	–	–	ns
Tcehd	EM_Clock high to EM_CEn high		T/2 – 5	–	–	ns
Taddrv	EM_Addr valid to EM_Clock high		5	–	–	ns
Taddriv	EM_Clock high to EM_Addr invalid		T/2 – 5	–	–	ns
Toeld	EM_OEn low to EM_Clock high		5	–	–	ns
Toehd	EM_Clock high to EM_OEn high		T	–	–	ns
Tds	Data valid before EM_OEn high		T + 15	–	–	ns
Tadscld	EM_ADSCn low to EM_Clock high		5	–	–	ns
Tadschd	EM_Clock high to EM_ADSCn high		T/2 – 5	–	–	ns

Note
62. Limited by GPIO output frequency, see Table 11-10 on page 77.

Figure 11-59. IMO Current vs. Frequency

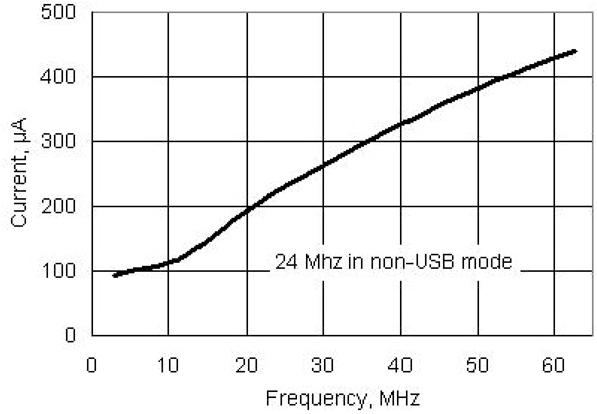


Table 11-66. IMO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F_{IMO}	IMO frequency stability (with factory trim)					
	24 MHz – Non USB mode		–4	–	4	%
	24 MHz – USB mode	With oscillator locking to USB bus	–0.25	–	0.25	%
	12 MHz		–3	–	3	%
	6 MHz		–2	–	2	%
	3 MHz		–2	–	2	%
	Startup time[69]	From enable (during normal system operation)	–	–	13	µs
Jp-p	Jitter (peak to peak)[69]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	1.6	–	ns
Jperiod	Jitter (long term)[69]					
	F = 24 MHz		–	0.9	–	ns
	F = 3 MHz		–	12	–	ns

Figure 11-60. IMO Frequency Variation vs. Temperature

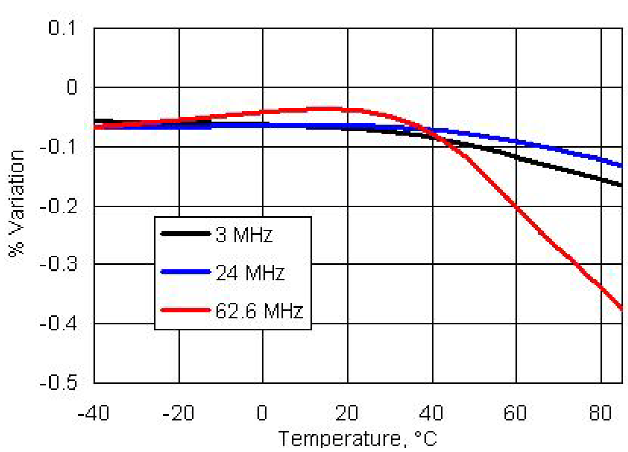
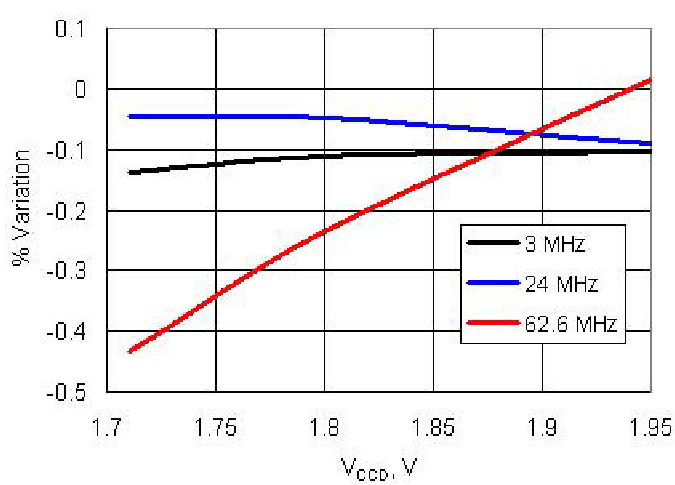


Figure 11-61. IMO Frequency Variation vs. V_{CC}



Note
69. Based on device characterization (Not production tested).

12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 2: CY8C32 family
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- c: Speed grade
  - 4: 50 MHz
  - 6: 67 MHz
- d: Flash capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
  - FN: CSP
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters.

Example CY8C 3 2 4 6 P V I - x x x

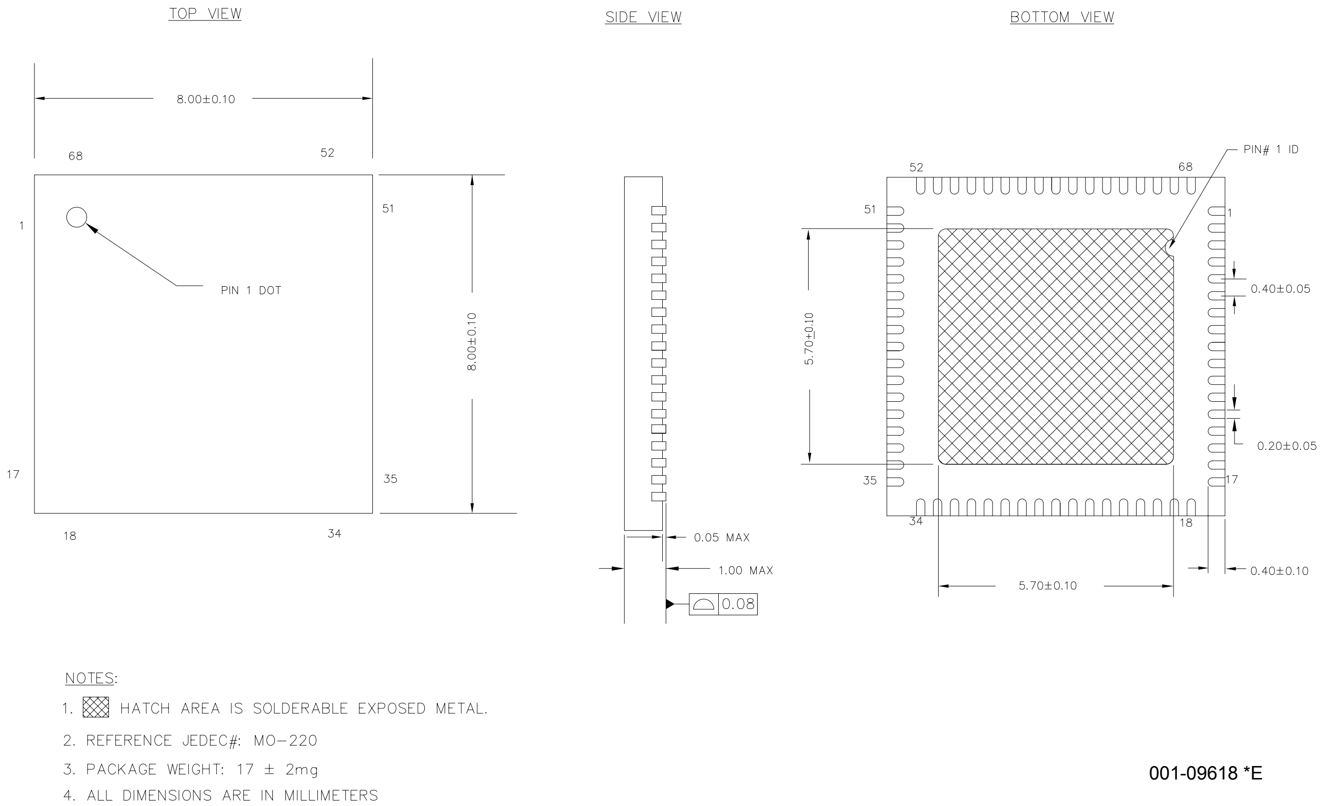
	Cypress Prefix	CY8C
3: PSoC 3	**Architecture**	3
2: CY8C32 Family	**Family Group within Architecture**	2
4: 50 MHz	**Speed Grade**	4
6: 64 KB	**Flash Capacity**	6
PV: SSOP	**Package Code**	P V
I: Industrial	**Temperature Range**	I
	Peripheral Set	x x x

Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C32 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

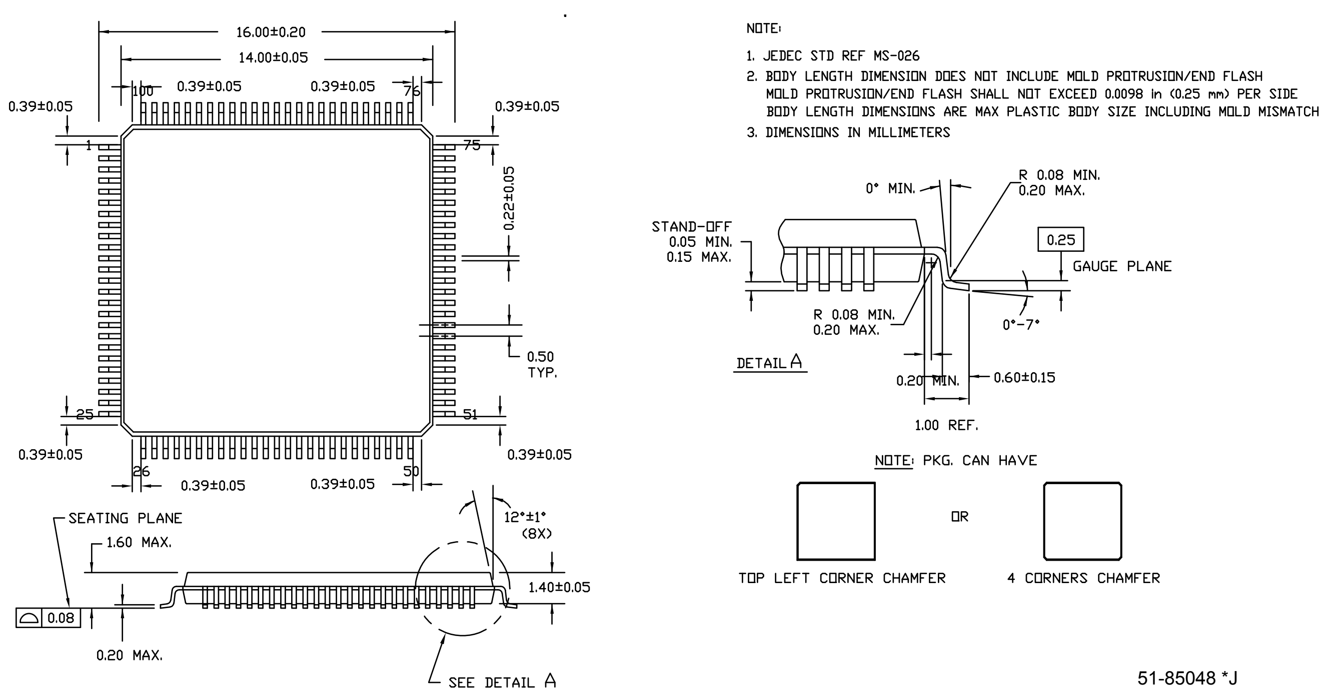
A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other "end of life" requirements.

Figure 13-3. 68-pin QFN 8×8 with 0.4 mm Pitch Package Outline (Sawn Version)



001-09618 *E

Figure 13-4. 100-pin TQFP (14 × 14 × 1.4 mm) Package Outline



51-85048 *J

17. Revision History

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	2796903	11/04/09	MKEA	New datasheet
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11- 7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V_{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V_{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*B	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V_{BIAS} specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I_{OUT} typical and maximum values. Changed Temperature Sensor range to –40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*M	3645908	06/14/2012	MKEA	Added paragraph clarifying that to achieve low hibernate current, you must limit the frequency of IO input signals. Revised description of IPOR and clarified PRES term. Changed footnote to state that all GPIO input voltages - not just analog voltages - must be less than Vddio. Updated 100-TQFP package drawing Clarified description of opamp Iout spec Changed “compliant with I2C” to “compatible with I2C” Updated 48-QFN package drawing Changed reset status register description text to clarify that not all reset sources are in the register Updated example PCB layout figure Removed text stating that FTW is a wakeup source Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Added “based on char” footnote to voltage monitors response time spec Changed analog global spec descriptions and values Added spec for ESDhbm for when Vssa and Vssd are separate Added a statement about support for JTAG programmers and file formats Changed comparator specs and conditions Added text describing flash cache, and updated related text Changed text and added figures describing Vddio source and sink Added a statement about support for JTAG programmers and file formats. Changed comparator specs and conditions Added text on adjustability of buzz frequency Updated terminology for “master” and “system” clock Deleted the text “debug operations are possible while the device is reset” Deleted and updated text regarding SIO performance under certain power ramp conditions Removed from boost mention of 22 µH inductors. This included deleting some graph figures. Changed DAC high and low speed/power mode descriptions and conditions Changed IMO startup time spec Added text on XRES and PRES re-arm times Added text about usage in externally regulated mode Updated package diagram spec 001-45616 to *D revision. Changed supply ramp rate spec from 1 V/ns to 0.066 V/µs Changed text describing SIO modes for overvoltage tolerance Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Added chip Idd specs for active and low-power modes, for multiple voltage, temperature and usage conditions Updated del-sig ADC spec tables, to replace three the instances of “16 bit” with “12 bit”
*N	3648803	06/18/2012	WKA/ MKEA	No changes. EROS update.

18. Sales, Solutions, and Legal Information

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