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Applications of "<u>Embedded -</u> <u>Microcontrollers</u>"

Details

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Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-VFQFN Exposed Pad
Supplier Device Package	48-QFN (7x7)
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246lti-162t

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong





This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a $1-\mu$ A sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 31 of this datasheet.

PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for "printf" style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 62 of this datasheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.



4.3 Instruction Set

The 8051 instruction set is highly optimized for 8-bit handling and Boolean operations. The types of instructions supported include:

- Arithmetic instructions
- Logical instructions
- Data transfer instructions
- Boolean instructions
- Program branching instructions

Table 4-1. Arithmetic Instructions

4.3.1 Instruction Set Summary

4.3.1.1 Arithmetic Instructions

Arithmetic instructions support the direct, indirect, register, immediate constant, and register-specific instructions. Arithmetic modes are used for addition, subtraction, multiplication, division, increment, and decrement operations. Table 4-1 lists the different arithmetic instructions.

Mnemonic	Description	Bytes	Cycles
ADD A,Rn	Add register to accumulator	1	1
ADD A,Direct	Add direct byte to accumulator	2	2
ADD A,@Ri	Add indirect RAM to accumulator	1	2
ADD A,#data	Add immediate data to accumulator	2	2
ADDC A,Rn	Add register to accumulator with carry	1	1
ADDC A, Direct	Add direct byte to accumulator with carry	2	2
ADDC A,@Ri	Add indirect RAM to accumulator with carry	1	2
ADDC A,#data	Add immediate data to accumulator with carry	2	2
SUBB A,Rn	Subtract register from accumulator with borrow	1	1
SUBB A, Direct	Subtract direct byte from accumulator with borrow	2	2
SUBB A,@Ri	Subtract indirect RAM from accumulator with borrow	1	2
SUBB A,#data	Subtract immediate data from accumulator with borrow	2	2
INC A	Increment accumulator	1	1
INC Rn	Increment register	1	2
INC Direct	Increment direct byte	2	3
INC @Ri	Increment indirect RAM	1	3
DEC A	Decrement accumulator	1	1
DEC Rn	Decrement register	1	2
DEC Direct	Decrement direct byte	2	3
DEC @Ri	Decrement indirect RAM	1	3
INC DPTR	Increment data pointer	1	1
MUL	Multiply accumulator and B	1	2
DIV	Divide accumulator by B	1	6
DAA	Decimal adjust accumulator	1	3





4.4.2 DMA Features

- 24 DMA channels
- Each channel has one or more transaction descriptors (TDs) to configure channel behavior. Up to 128 total TDs can be defined
- TDs can be dynamically updated
- Eight levels of priority per channel
- Any digitally routable signal, the CPU, or another DMA channel, can trigger a transaction
- Each channel can generate up to two interrupts per transfer
- Transactions can be stalled or canceled
- Supports transaction size of infinite or 1 to 64k bytes
- TDs may be nested and/or chained for complex transactions

4.4.3 Priority Levels

The CPU always has higher priority than the DMA controller when their accesses require the same bus resources. Due to the system architecture, the CPU can never starve the DMA. DMA channels of higher priority (lower priority number) may interrupt current DMA transfers. In the case of an interrupt, the current transfer is allowed to complete its current transaction. To ensure latency limits when multiple DMA accesses are requested simultaneously, a fairness algorithm guarantees an interleaved minimum percentage of bus bandwidth for priority levels 2 through 7. Priority levels 0 and 1 do not take part in the fairness algorithm and may use 100 percent of the bus bandwidth. If a tie occurs on two DMA requests of the same priority level, a simple round robin method is used to evenly share the allocated bandwidth. The round robin allocation can be disabled for each DMA channel, allowing it to always be at the head of the line. Priority levels 2 to 7 are guaranteed the minimum bus bandwidth shown in Table 4-7 after the CPU and DMA priority levels 0 and 1 have satisfied their requirements.



4.4.4.2 Auto Repeat DMA

Auto repeat DMA is typically used when a static pattern is repetitively read from system memory and written to a peripheral. This is done with a single TD that chains to itself.

4.4.4.3 Ping Pong DMA

A ping pong DMA case uses double buffering to allow one buffer to be filled by one client while another client is consuming the

Table 4-7. Priority Levels

Priority Level	% Bus Bandwidth
0	100.0
1	100.0
2	50.0
3	25.0
4	12.5
5	6.2
6	3.1
7	1.5

When the fairness algorithm is disabled, DMA access is granted based solely on the priority level; no bus bandwidth guarantees are made.

4.4.4 Transaction Modes Supported

The flexible configuration of each DMA channel and the ability to chain multiple channels allow the creation of both simple and complex use cases. General use cases include, but are not limited to:

4.4.4.1 Simple DMA

In a simple DMA case, a single TD transfers data between a source and sink (peripherals or memory location). The basic timing diagrams of DMA read and write cycles are shown in Figure 4-1. For more description on other transfer modes, refer to the Technical Reference Manual.

Figure 4-1. DMA Timing Diagram



data previously received in the other buffer. In its simplest form, this is done by chaining two TDs together so that each TD calls the opposite TD when complete.

4.4.4.4 Circular DMA

Circular DMA is similar to ping pong DMA except it contains more than two buffers. In this case there are multiple TDs; after the last TD is complete it chains back to the first TD.



Figure 6-3. 32kHzECO Block Diagram



It is recommended that the external 32.768-kHz watch crystal have a load capacitance (CL) of 6 pF or 12.5 pF. Check the crystal manufacturer's datasheet. The two external capacitors, CL1 and CL2, are typically of the same value, and their total capacitance, CL1CL2 / (CL1 + CL2), including pin and trace capacitance, should equal the crystal CL value. For more information, refer to application note AN54439: PSoC 3 and PSoC 5 External Oscillators. See also pin capacitance specifications in the "GPIO" section on page 76.

6.1.2.3 Digital System Interconnect

The DSI provides routing for clocks taken from external clock oscillators connected to I/O. The oscillators can also be generated within the device in the digital system and Universal Digital Blocks.

While the primary DSI clock input provides access to all clocking resources, up to eight other DSI clocks (internally or externally generated) may be routed directly to the eight digital clock dividers. This is only possible if there are multiple precision clock sources.

6.1.3 Clock Distribution

All seven clock sources are inputs to the central clock distribution system. The distribution system is designed to create multiple high precision clocks. These clocks are customized for the design's requirements and eliminate the common problems found with limited resolution prescalers attached to peripherals. The clock distribution system generates several types of clock trees.

The master clock is used to select and supply the fastest clock in the system for general clock requirements and clock synchronization of the PSoC device.

- Bus Clock 16-bit divider uses the master clock to generate the bus clock used for data transfers. Bus clock is the source clock for the CPU clock divider.
- Eight fully programmable 16-bit clock dividers generate digital system clocks for general use in the digital system, as configured by the design's requirements. Digital system clocks can generate custom clocks derived from any of the seven clock sources for any purpose. Examples include baud rate generators, accurate PWM periods, and timer clocks, and many others. If more than eight digital clock dividers are required, the Universal Digital Blocks (UDBs) and fixed function Timer/Counter/PWMs can also generate clocks.
- Four 16-bit clock dividers generate clocks for the analog system components that require clocking, such as ADC. The analog clock dividers include skew control to ensure that critical analog events do not occur simultaneously with digital switching events. This is done to reduce analog system noise.

Each clock divider consists of an 8-input multiplexer, a 16-bit clock divider (divide by 2 and higher) that generates ~50 percent duty cycle clocks, master clock resynchronization logic, and deglitch logic. The outputs from each digital clock tree can be routed into the digital system interconnect and then brought back into the clock system as an input, allowing clock chaining of up to 32 bits.

6.1.4 USB Clock Domain

The USB clock domain is unique in that it operates largely asynchronously from the main clock network. The USB logic contains a synchronous bus interface to the chip, while running on an asynchronous clock to process USB data. The USB logic requires a 48 MHz frequency. This frequency can be generated from different sources, including DSI clock at 48 MHz or doubled value of 24 MHz from internal oscillator, DSI signal, or crystal oscillator.

6.2 Power System

The power system consists of separate analog, digital, and I/O supply pins, labeled VDDA, VDDD, and VDDIOX, respectively. It also includes two internal 1.8 V regulators that provide the digital (VCCD) and analog (VCCA) supplies for the internal core logic. The output pins of the regulators (VCCD and VCCA) and the VDDIO pins must have capacitors connected as shown in Figure 6-4. The two VCCD pins must be shorted together, with as short a trace as possible, and connected to a 1- μ F ±10-percent X5R capacitor. The power system also contains a sleep regulator, an I²C regulator, and a hibernate regulator.



Figure 6-5. Power Mode Transitions



6.2.1.1 Active Mode

Active mode is the primary operating mode of the device. When in active mode, the active configuration template bits control which available resources are enabled or disabled. When a resource is disabled, the digital clocks are gated, analog bias currents are disabled, and leakage currents are reduced as appropriate. User firmware can dynamically control subsystem power by setting and clearing bits in the active configuration template. The CPU can disable itself, in which case the CPU is automatically reenabled at the next wakeup event.

When a wakeup event occurs, the global mode is always returned to active, and the CPU is automatically enabled, regardless of its template settings. Active mode is the default global power mode upon boot.

6.2.1.2 Alternate Active Mode

Alternate Active mode is very similar to Active mode. In alternate active mode, fewer subsystems are enabled, to reduce power consumption. One possible configuration is to turn off the CPU and flash, and run peripherals at full speed.

6.2.1.3 Sleep Mode

Sleep mode reduces power consumption when a resume time of 15 μ s is acceptable. The wake time is used to ensure that the regulator outputs are stable enough to directly enter active mode.

6.2.1.4 Hibernate Mode

In hibernate mode nearly all of the internal functions are disabled. Internal voltages are reduced to the minimal level to keep vital systems alive. Configuration state is preserved in hibernate mode and SRAM memory is retained. GPIOs configured as digital outputs maintain their previous values and external GPIO pin interrupt settings are preserved. The device can only return from hibernate mode in response to an external I/O interrupt. The resume time from hibernate mode is less than 100 µs.

To achieve an extremely low current, the hibernate regulator has limited capacity. This limits the frequency of any signal present on the input pins - no GPIO should toggle at a rate greater than 10 kHz while in hibernate mode. If pins must be toggled at a high rate while in a low power mode, use sleep mode instead.

6.2.1.5 Wakeup Events

Wakeup events are configurable and can come from an interrupt or device reset. A wakeup event restores the system to active mode. Firmware enabled interrupt sources include internally generated interrupts, power supervisor, central timewheel, and I/O interrupts. Internal interrupt sources can come from a variety of peripherals, such as analog comparators and UDBs. The central timewheel provides periodic interrupts to allow the system to wake up, poll peripherals, or perform real-time functions. Reset event sources include the external reset I/O pin (XRES), WDT, and Precision Reset (PRES).

6.2.2 Boost Converter

Applications that use a supply voltage of less than 1.71 V, such as solar panels or single cell battery supplies, may use the on-chip boost converter to generate a minimum of 1.8 V supply voltage. The boost converter may also be used in any system that requires a higher operating voltage than the supply provides such as driving 5.0 V LCD glass in a 3.3 V system. With the addition of an inductor, Schottky diode, and capacitors, it produces a selectable output voltage sourcing enough current to operate the PSoC and other on-board components.

The boost converter accepts an input voltage V_{BAT} from 0.5 V to 3.6 V, and can start up with V_{BAT} as low as 0.5 V. The converter provides a user configurable output voltage of 1.8 to 5.0 V (V_{OUT}) in 100 mV increments. V_{BAT} is typically less than V_{OUT}; if V_{BAT} is greater than or equal to V_{OUT}, then V_{OUT} will be slightly less than V_{BAT} due to resistive losses in the boost converter. The block can deliver up to 50 mA (I_{BOOST}) depending on configuration to both the PSoC device and external components. The sum of all current sinks in the design including the PSoC device, PSoC I/O pin loads, and external component loads must be less than the I_{BOOST} specified maximum current.

Four pins are associated with the boost converter: VBAT, VSSB, VBOOST, and IND. The boosted output voltage is sensed at the VBOOST pin and must be connected directly to the chip's supply inputs, VDDA, VDDD, and VDDIO, if used to power the PSoC device.

The boost converter requires four components in addition to those required in a non-boost design, as shown in Figure 6-6 on page 35. A 22-µF capacitor (CBAT) is required close to the VBAT pin to provide local bulk storage of the battery voltage and provide regulator stability. A diode between the battery and VBAT pin should not be used for reverse polarity protection because the diodes forward voltage drop reduces the $\ensuremath{\mathsf{V}_{\mathsf{BAT}}}$ voltage. Between the VBAT and IND pins, an inductor of 4.7 µH, 10 µH, or 22 µH is required. The inductor value can be optimized to increase the boost converter efficiency based on input voltage, output voltage, temperature, and current. Inductor size is determined by following the design guidance in this section and the electrical specifications. The inductor must be placed within 1 cm of the VBAT and IND pins and have a minimum saturation current of 750 mA. Between the IND and VBOOST pins, place a Schottky diode within 1 cm of the pins. This diode shall have a forward current rating of at least 1.0 A and a reverse voltage of at least 20 V. Connect a 22-µF bulk capacitor (CBOOST) close to VBOOST to provide regulator output stability. It is important to sum the total capacitance connected to the VBOOST pin and ensure the maximum CBOOST specification is not exceeded. All capacitors must be rated for a minimum of 10 V to minimize capacitive losses due to voltage de-rating.



7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I²C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



Routing Channel

The main component blocks of the UDB are:

- PLD blocks There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.

- Status and Control Module The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.



Figure 7-17. Connection of Devices to the I²C Bus



For most designs, the default values in Table 7-2 will provide excellent performance without any calculations. The default values were chosen to use standard resistor values between the minimum and maximum limits. The values in Table 7-2 work for designs with 1.8 V to 5.0V V_{DD}, less than 200-pF bus capacitance (C_B), up to 25 μ A of total input leakage (I_{IL}), up to 0.4 V output voltage level (V_{OL}), and a max V_{IH} of 0.7 * V_{DD}. Standard Mode and Fast Mode can use either GPIO or SIO PSoC pins. Fast Mode Plus requires use of SIO pins to meet the V_{OL} spec at 20 mA. Calculation of custom pull-up resistor values is required; if your design does not meet the default assumptions, you use series resistor value for low power consumption.

Table 7-2. Recommended default Pull-up Resistor Values

	R _P	Units
Standard Mode – 100 kbps	4.7 k, 5%	Ω
Fast Mode – 400 kbps	1.74 k, 1%	Ω
Fast Mode Plus – 1 Mbps	620, 5%	Ω

Calculation of the ideal pull-up resistor value involves finding a value between the limits set by three equations detailed in the NXP I^2C specification. These equations are:

Equation 1:

$$R_{PMIN} = (V_{DD}(max) - V_{OL}(max))/(I_{OL}(min))$$

Equation 2:

$$R_{PMAX} = T_R(max)/0.8473 \times C_R(max)$$

Equation 3:

 $R_{PMAX} = V_{DD}(min) - V_{IH}(min) + V_{NH}(min) / I_{IH}(max)$

Equation parameters:

 V_{DD} = Nominal supply voltage for I²C bus

V_{OL} = Maximum output low voltage of bus devices.

 I_{OI} = Low-level output current from I²C specification

 T_R = Rise Time of bus from I²C specification

C_B = Capacitance of each bus line including pins and PCB traces

V_{IH} = Minimum high-level input voltage of all bus devices

 V_{NH} = Minimum high-level input noise margin from I^2C specification

I_{IH} = Total input leakage current of all devices on the bus

The supply voltage (V_{DD}) limits the minimum pull-up resistor value due to bus devices maximum low output voltage (V_{DL}) specifications. Lower pull-up resistance increases current through the pins and can, therefore, exceed the spec conditions of V_{OL}. Equation 1 is derived using Ohm's law to determine the minimum resistance that will still meet the V_{OL} specification at 3 mA for standard and fast modes, and 20 mA for fast mode plus at the given V_{DD}.

Equation 2 determines the maximum pull-up resistance due to bus capacitance. Total bus capacitance is comprised of all pin, wire, and trace capacitance on the bus. The higher the bus capacitance, the lower the pull-up resistance required to meet the specified bus speeds rise time due to RC delays. Choosing a pull-up resistance higher than allowed can result in failing timing requirements resulting in communication errors. Most designs with five or less I^2C devices and up to 20 centimeters of bus trace length have less than 100 pF of bus capacitance.

A secondary effect that limits the maximum pull-up resistor value is total bus leakage calculated in Equation 3. The primary source of leakage is I/O pins connected to the bus. If leakage is too high, the pull-ups will have difficulty maintaining an acceptable V_{IH} level causing communication errors. Most designs with five or less I²C devices on the bus have less than 10 µA of total leakage current.



Analog local buses (abus) are routing resources located within the analog subsystem and are used to route signals between different analog blocks. There are eight abus routes in CY8C32, four in the left half (abusl [0:3]) and four in the right half (abusr [0:3]) as shown in Figure 8-2. Using the abus saves the analog globals and analog mux buses from being used for interconnecting the analog blocks.

Multiplexers and switches exist on the various buses to direct signals into and out of the analog blocks. A multiplexer can have only one connection on at a time, whereas a switch can have multiple connections on simultaneously. In Figure 8-2, multiplexers are indicated by grayed ovals and switches are indicated by transparent ovals.

8.2 Delta-sigma ADC

The CY8C32 device contains one delta-sigma ADC. This ADC offers differential input, high resolution and excellent linearity, making it a good ADC choice for measurement applications. The converter can be configured to output 12-bit resolution at data rates of up to 192 ksps. At a fixed clock rate, resolution can be traded for faster data rates as shown in Table 8-1 and Figure 8-3.

Table 8-1.	Delta-sigma	ADC Performa	nce
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Bits	Maximum Sample Rate (sps)	SINAD (dB)
12	192 k	66
8	384 k	43

Figure 8-3. Delta-sigma ADC Sample Rates, Range = ±1.024 V



8.2.1 Functional Description

The ADC connects and configures three basic components, input buffer, delta-sigma modulator, and decimator. The basic block diagram is shown in Figure 8-4. The signal from the input muxes is delivered to the delta-sigma modulator either directly or through the input buffer. The delta-sigma modulator performs the actual analog to digital conversion. The modulator over-samples the input and generates a serial data stream output. This high

speed data stream is not useful for most applications without some type of post processing, and so is passed to the decimator through the Analog Interface block. The decimator converts the high speed serial data stream into parallel ADC results. The modulator/decimator frequency response is $[(\sin x)/x]^4$.

Figure 8-4. Delta-sigma ADC Block Diagram



Resolution and sample rate are controlled by the Decimator. Data is pipelined in the decimator; the output is a function of the last four samples. When the input multiplexer is switched, the output data is not valid until after the fourth sample after the switch.

8.2.2 Operational Modes

The ADC can be configured by the user to operate in one of four modes: Single Sample, Multi Sample, Continuous, or Multi Sample (Turbo). All four modes are started by either a write to the start bit in a control register or an assertion of the Start of Conversion (SoC) signal. When the conversion is complete, a status bit is set and the output signal End of Conversion (EoC) asserts high and remains high until the value is read by either the DMA controller or the CPU.

8.2.2.1 Single Sample

In Single Sample mode, the ADC performs one sample conversion on a trigger. In this mode, the ADC stays in standby state waiting for the SoC signal to be asserted. When SoC is signaled the ADC performs four successive conversions. The first three conversions prime the decimator. The ADC result is valid and available after the fourth conversion, at which time the EoC signal is generated. To detect the end of conversion, the system may poll a control register for status or configure the external EoC signal to generate an interrupt or invoke a DMA request. When the transfer is done the ADC reenters the standby state where it stays until another SoC event.

8.2.2.2 Continuous

Continuous sample mode is used to take multiple successive samples of a single input signal. Multiplexing multiple inputs should not be done with this mode. There is a latency of three conversion times before the first conversion result is available. This is the time required to prime the decimator. After the first result, successive conversions are available at the selected sample rate.

8.2.2.3 Multi Sample

Multi sample mode is similar to continuous mode except that the ADC is reset between samples. This mode is useful when the input is switched between multiple signals. The decimator is re-primed between each sample so that previous samples do not affect the current conversion. Upon completion of a sample, the next sample is automatically initiated. The results can be transferred using either firmware polling, interrupt, or DMA.



11.2 Device Level Specifications

Specifications are valid for –40 $^{\circ}C \le T_A \le 85 ~^{\circ}C$ and $T_J \le 100 ~^{\circ}C$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions		Min	Typ ^[22]	Max	Units	
V _{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulato	r enabled	1.8	_	5.5	V	
V _{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulato	r disabled	1.71	1.8	1.89	V	
V	ameterDescriptionConditionsAnalog supply voltage and input to analog core regulatorAnalog core regulator enabledAnalog supply voltage, analog regulator bypassedAnalog core regulator disabledDigital supply voltage relative to V_{SSD} Digital core regulator enabledDigital supply voltage relative to V_{SSD} Digital core regulator enabledDigital supply voltage, digital regulator bypassedDigital core regulator disabledDigital supply voltage relative to V_{SSD} Digital core regulator disabledDigital core voltage relative to V_{SSIO} Digital core regulator disabledDirect analog core voltage input (Analog 	enabled	1.8	-	V _{DDA} ^[18]	V		
Parameter VDDA A VDDA A VDDA B VDDD E VDDD E VDDD E VDDIO ^[19] I/ VCCA Fr VCCD Fr IDD E IDD I	Digital supply voltage relative to v _{SSD}		enableu	-	-	V _{DDA} + 0.1 ^[24]	v	
V _{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator	disabled	1.71	1.8	1.89	V	
V[19]	^[19] I/O supply voltage relative to Vacua		1.71	-	V _{DDA} ^[18]	V		
ADDIO.		-		-	_	V _{DDA} + 0.1 ^[24]		
V _{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulato	r disabled	1.71	1.8	1.89	V	
V _{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled			1.8	1.89	V	
	Active Mode							
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	$V_{DDX} = 2.7 V - 5.5 V; F_{CPU} = 6 MHz^{[23]} T = 25 °C T = 85 °C T =$	T = -40 °C	-	1.2	2.9		
			T = 25 °C	_	1.2	3.1		
			-	4.9	7.7			
		$V_{DDX} = 2.7 V - 5.5 V; F_{CPU} = 3 MHz^{[23]} T = 25 °C T = 85 °C T =$	T = -40 °C	-	1.3	2.9		
			T = 25 °C	I	1.6	3.2		
			T = 85 °C	I	4.8	7.5		
		$V_{DDX} = 2.7 V - 5.5 V; F_{CPU} = 6 MHz T = 25 °C T = 85 °C $	T = -40 °C	-	2.1	3.7		
			T = 25 °C	-	2.3	3.9		
I _{DD} ^[20, 21]			I	5.6	8.5	mΔ		
	IMO enabled, bus clock and CPU clock	$V_{DDX} = 2.7 V - 5.5 V;$	T = -40 °C	-	3.5	5.2		
	enabled. CPU executing program from	$F_{CPU} = 12 \text{ MHz}^{(23)}$	T = 25 °C	_	3.8	5.5		
	flash.		T = 85 °C	_	7.1	9.8		
		$V_{DDX} = 2.7 V - 5.5 V;$	T = -40 °C	_	6.3	8.1		
		F _{CPU} = 24 MHz ^[23]	T = 25 °C	-	6.6	8.3		
			T = 85 °C	-	10	13		
		$V_{DDX} = 2.7 V - 5.5 V;$	T = -40 °C	-	11.5	13.5		
		F _{CPU} = 48 MHz ^[23]	T = 25 °C	-	12	14		
		T = 85 °C		-	15.5	18.5		

Notes

18. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies. 19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin $\leq V_{DDIO} \leq V_{DDA}$. 20. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.

21. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.

22. V_{DDX} = 3.3 V. 23. Based on device characterizations (Not production tested).

24. Guaranteed by design, not production tested.



Figure 11-15. GPIO Output High Voltage and Current





Table 11-10. GPIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
TriseF	Rise time in Fast Strong Mode ^[38]	3.3 V V _{DDIO} Cload = 25 pF	_	-	6	ns
TfallF	Fall time in Fast Strong Mode ^[38]	3.3 V V _{DDIO} Cload = 25 pF	_	-	6	ns
TriseS	Rise time in Slow Strong Mode ^[38]	3.3 V V _{DDIO} Cload = 25 pF	-	_	60	ns
TfallS	Fall time in Slow Strong Mode ^[38]	3.3 V V _{DDIO} Cload = 25 pF	_	-	60	ns
	GPIO output operating frequency					
	2.7 V \leq V _{DDIO} \leq 5.5 V, fast strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	33	MHz
Fgpioout	1.71 V \leq V _{DDIO} < 2.7 V, fast strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	20	MHz
	$3.3 \text{ V} \leq \text{V}_{\text{DDIO}} \leq 5.5 \text{ V}$, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	7	MHz
	1.71 V \leq V _{DDIO} < 3.3 V, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	_	3.5	MHz
Egnioin	GPIO input operating frequency					
' gpiolit	$1.71 \text{ V} \le \text{V}_{\text{DDIO}} \le 5.5 \text{ V}$	90/10% V _{DDIO}	-	-	33	MHz

^{38.} Based on device characterization (Not production tested).



Table 11-12. SIO AC Specifications (continued)

Parameter	Description	Conditions	Min	Тур	Max	Units
	SIO output operating frequency					
	2.7 V < V _{DDIO} < 5.5 V, Unregu- lated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	33	MHz
	1.71 V < V _{DDIO} < 2.7 V, Unregu- lated output (GPIO) mode, fast strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	16	MHz
	3.3 V < V _{DDIO} < 5.5 V, Unregu- lated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	-	-	5	MHz
Fsioout	1.71 V < V _{DDIO} < 3.3 V, Unregu- lated output (GPIO) mode, slow strong drive mode	90/10% V _{DDIO} into 25 pF	_	-	4	MHz
	$2.7 V < V_{DDIO} < 5.5 V$, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	_	-	20	MHz
	1.71 V < V _{DDIO} < 2.7 V, Regulated output mode, fast strong drive mode	Output continuously switching into 25 pF	-	-	10	MHz
	1.71 V < V _{DDIO} < 5.5 V, Regulated output mode, slow strong drive mode	Output continuously switching into 25 pF	_	-	2.5	MHz
Esioin	SIO input operating frequency					
Fsioout Fsioin	$1.71 \text{ V} \le \text{V}_{\text{DDIO}} \le 5.5 \text{ V}$	90/10% V _{DDIO}	_	-	33	MHz

Figure 11-20. SIO Output Rise and Fall Times, Fast Strong Mode, V_{DDIO} = 3.3 V, 25 pF Load



Figure 11-21. SIO Output Rise and Fall Times, Slow Strong Mode, $V_{\mbox{DDIO}}$ = 3.3 V, 25 pF Load





Figure 11-22. USBIO Output High Voltage and Current, GPIO Mode







Table 11-15. USBIO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Tdrate	Full-speed data rate average bit rate		12 – 0.25%	12	12 + 0.25%	MHz
Tjr1	Receiver data jitter tolerance to next transition		-8	-	8	ns
Tjr2	Receiver data jitter tolerance to pair transition		-5	_	5	ns
Tdj1	Driver differential jitter to next transition		-3.5	-	3.5	ns
Tdj2	Driver differential jitter to pair transition		-4	-	4	ns
Tfdeop	Source jitter for differential transition to SE0 transition		-2	-	5	ns
Tfeopt	Source SE0 interval of EOP		160	-	175	ns
Tfeopr	Receiver SE0 interval of EOP		82	_	_	ns
Tfst	Width of SE0 interval during differ- ential transition		-	-	14	ns
Fgpio_out	GPIO mode output operating	$3 \text{ V} \leq \text{V}_{\text{DDD}} \leq 5.5 \text{ V}$	-	_	20	MHz
	frequency	V _{DDD} = 1.71 V	-	_	6	MHz
Tr_gpio	Rise time, GPIO mode, 10%/90%	V _{DDD} > 3 V, 25 pF load	_	-	12	ns
	V _{DDD}	V _{DDD} = 1.71 V, 25 pF load	_	-	40	ns
Tf_gpio	Fall time, GPIO mode, 90%/10% V _{DDD}	V _{DDD} > 3 V, 25 pF load	_	_	12	ns
		V _{DDD} = 1.71 V, 25 pF load	_	_	40	ns

Figure 11-24. USBIO Output Rise and Fall Times, GPIO Mode,







Figure 11-34. IDAC Operating Current vs Temperature, Range = 255μ A, Code = 0, Source Mode



Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255μ A, Sink Mode



Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 μ A, Code = 0, Sink Mode





11.6.6 USB

Table 11-43. USB DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
V _{USB_5}	Device supply (V _{DDD}) for USB operation	USB configured, USB regulator enabled	4.35	-	5.25	V
V _{USB_3.3}		USB configured, USB regulator bypassed	3.15	-	3.6	V
V _{USB_3}		USB configured, USB regulator bypassed ^[54]	2.85	-	3.6	V
IUSB_Configured	Device supply current in device active	V _{DDD} = 5 V, F _{CPU} = 1.5 MHz	_	10	-	mA
	mode, bus clock and IMO = 24 MHz	V _{DDD} = 3.3 V, F _{CPU} = 1.5 MHz	_	8	-	mA
IUSB_Suspended	Device supply current in device sleep mode	V _{DDD} = 5 V, connected to USB host, PICU configured to wake on USB resume signal	_	0.5	-	mA
		V _{DDD} = 5 V, disconnected from USB host	_	0.3	-	mA
		V _{DDD} = 3.3 V, connected to USB host, PICU configured to wake on USB resume signal	-	0.5	-	mA
		V _{DDD} = 3.3 V, disconnected from USB host	_	0.3	-	mA

11.6.7 Universal Digital Blocks (UDBs)

PSoC Creator provides a library of pre-built and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. See the component datasheets in PSoC Creator for full AC/DC specifications, APIs, and example code.

Table 11-44. UDB AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Datapath Per	formance					
F _{MAX_TIMER}	Maximum frequency of 16-bit timer in a UDB pair		-	_	50.01	MHz
F _{MAX_ADDER}	Maximum frequency of 16-bit adder in a UDB pair		-	_	50.01	MHz
F _{MAX_CRC}	Maximum frequency of 16-bit CRC/PRS in a UDB pair		-	_	50.01	MHz
PLD Perform	ance					
F _{MAX_PLD}	Maximum frequency of a two-pass PLD function in a UDB pair		-	_	50.01	MHz
Clock to Outp	but Performance					
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-52 on page 99.	25 °C, $V_{DDD} \ge 2.7 V$	-	20	25	ns
t _{CLK_OUT}	Propagation delay for clock in to data out, see Figure 11-52 on page 99.	Worst-case placement, routing, and pin selection	-	-	55	ns

Note 54. Rise/fall time matching (TR) not guaranteed, see USB Driver AC Specifications on page 83.



11.8 PSoC System Resources

Specifications are valid for –40 °C \leq T_A \leq 85 °C and T_J \leq 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.8.1 POR with Brown Out

For brown out detect in regulated mode, V_{DDD} and V_{DDA} must be \geq 2.0 V. Brown out detect is not available in externally regulated mode.

Table 11-57. Precise Low-Voltage Reset (PRES) with Brown Out DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
PRESR	Rising trip voltage	Factory trim	1.64	_	1.68	V
PRESF	Falling trip voltage		1.62	_	1.66	V

Table 11-58. Power-on Reset (POR) with Brown Out AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
PRES_TR	Response time		-	-	0.5	μs
	V _{DDD} /V _{DDA} droop rate	Sleep mode	-	5	-	V/sec

11.8.2 Voltage Monitors

Table 11-59. Voltage Monitors DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
LVI	Trip voltage					
	LVI_A/D_SEL[3:0] = 0000b		1.68	1.73	1.77	V
	LVI_A/D_SEL[3:0] = 0001b		1.89	1.95	2.01	V
	LVI_A/D_SEL[3:0] = 0010b		2.14	2.20	2.27	V
	LVI_A/D_SEL[3:0] = 0011b		2.38	2.45	2.53	V
	LVI_A/D_SEL[3:0] = 0100b		2.62	2.71	2.79	V
	LVI_A/D_SEL[3:0] = 0101b		2.87	2.95	3.04	V
	LVI_A/D_SEL[3:0] = 0110b		3.11	3.21	3.31	V
	LVI_A/D_SEL[3:0] = 0111b		3.35	3.46	3.56	V
	LVI_A/D_SEL[3:0] = 1000b		3.59	3.70	3.81	V
	LVI_A/D_SEL[3:0] = 1001b		3.84	3.95	4.07	V
	LVI_A/D_SEL[3:0] = 1010b		4.08	4.20	4.33	V
	LVI_A/D_SEL[3:0] = 1011b		4.32	4.45	4.59	V
	LVI_A/D_SEL[3:0] = 1100b		4.56	4.70	4.84	V
	LVI_A/D_SEL[3:0] = 1101b		4.83	4.98	5.13	V
	LVI_A/D_SEL[3:0] = 1110b		5.05	5.21	5.37	V
	LVI_A/D_SEL[3:0] = 1111b		5.30	5.47	5.63	V
HVI	Trip voltage		5.57	5.75	5.92	V

Table 11-60. Voltage Monitors AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Response time ^[64]		-	-	1	μs



11.8.3 Interrupt Controller

Table 11-61. Interrupt Controller AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
	Delay from interrupt signal input to ISR code execution from ISR code	Includes worse case completion of longest instruction DIV with 6 cycles	-	-	25	Tcy CPU

11.8.4 JTAG Interface





|--|

Parameter	Description	Conditions	Min	Тур	Max	Units
f_TCK	TCK frequency	$3.3 \text{ V} \leq \text{V}_{DDD} \leq 5 \text{ V}$	-	-	14 ^[66]	MHz
		$1.71 \text{ V} \le \text{V}_{\text{DDD}} < 3.3 \text{ V}$	-	-	7 ^[66]	MHz
T_TDI_setup	TDI setup before TCK high		(T/10)-5	-	-	ns
T_TMS_setup	TMS setup before TCK high		T/4	_	-	
T_TDI_hold	TDI, TMS hold after TCK high	T = 1/f_TCK max	T/4	_	-	
T_TDO_valid	TCK low to TDO valid	T = 1/f_TCK max	-	-	2T/5	
T_TDO_hold	TDO hold after TCK high	T = 1/f_TCK max	T/4	-	_	

Notes

65. Based on device characterization (Not production tested).
 66. f_TCK must also be no more than 1/3 CPU clock frequency.



11.9.4 kHz External Crystal Oscillator

Table 11-71. kHzECO DC Specifications^[72]

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{CC}	Operating current	Low-power mode; CL = 6 pF	-	0.25	1.0	μA
DL	Drive level		_	_	1	μW

Table 11-72. kHzECO AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
F	Frequency		-	32.768	_	kHz
T _{ON}	Startup time	High power mode	-	1	_	S

11.9.5 External Clock Reference

Table 11-73. External Clock Reference AC Specifications^[72]

Parameter	Description	Conditions	Min	Тур	Max	Units
	External frequency range		0	-	33	MHz
	Input duty cycle range	Measured at V _{DDIO} /2	30	50	70	%
	Input edge rate	V _{IL} to V _{IH}	0.5	_	_	V/ns

11.9.6 Phase–Locked Loop

Table 11-74. PLL DC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
I _{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	_	200	_	μA

Table 11-75. PLL AC Specifications

Parameter	Description	Conditions	Min	Тур	Max	Units
Fpllin	PLL input frequency ^[73]		1	_	48	MHz
	PLL intermediate frequency ^[74]	Output of prescaler	1	-	3	MHz
Fpllout	PLL output frequency ^[73]		24	-	50	MHz
	Lock time at startup		-	_	250	μs
Jperiod-rms	Jitter (rms) ^[72]		_	_	250	ps

Notes

72. Based on device characterization (Not production tested).
73. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
74. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.





Figure 13-1. 48-pin (300 mil) SSOP Package Outline

Figure 13-2. 48-pin QFN Package Outline



- 2. REFERENCE JEDEC#: MO-220
- 3. PACKAGE WEIGHT: REFER TO PMDD SPEC.
- 4. ALL DIMENSIONS ARE IN MM [MIN/MAX]
- 5. PACKAGE CODE

PART #	DESCRIPTION
LT48D	LEAD FREE

001-45616 *E



16. Document Conventions

16.1 Units of Measure

Table 16-1. Units of Measure

Symbol	Unit of Measure		
°C	degrees Celsius		
dB	decibels		
fF	femtofarads		
Hz	hertz		
KB	1024 bytes		
kbps	kilobits per second		
Khr	kilohours		
kHz	kilohertz		
kΩ	kilohms		
ksps	kilosamples per second		
LSB	least significant bit		
Mbps	megabits per second		
MHz	megahertz		
MΩ	megaohms		
Msps	megasamples per second		
μA	microamperes		

Symbol	Unit of Measure			
μF	microfarads			
μH	microhenrys			
μs	microseconds			
μV	microvolts			
μW	microwatts			
mA	milliamperes			
ms	milliseconds			
mV	millivolts			
nA	nanoamperes			
ns	nanoseconds			
nV	nanovolts			
Ω	ohms			
pF	picofarads			
ppm	parts per million			
ps	picoseconds			
S	seconds			
sps	samples per second			
sqrtHz	square root of hertz			
V	volts			

Table 16-1. Units of Measure (continued)



17. Revision History

Description Title: PSoC [®] 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC [®]) Document Number: 001-56955					
Revision	ECN	Submission Date	Orig. of Change	Description of Change	
**	2796903	11/04/09	MKEA	New datasheet	
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V _{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpioout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V _{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.	
*В	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V _{BIAS} specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I _{OUT} typical and maximum values. Changed Temperature Sensor range to -40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details	