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What is "[Embedded - Microcontrollers](#)"?

"[Embedded - Microcontrollers](#)" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "[Embedded - Microcontrollers](#)"

Details

Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I ² C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246pvi-122

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1. Architectural Overview

Introducing the CY8C32 family of ultra low-power, flash Programmable System-on-Chip (PSoC®) devices, part of a scalable 8-bit PSoC 3 and 32-bit PSoC 5 platform. The CY8C32 family provides configurable blocks of analog, digital, and interconnect circuitry around a CPU subsystem. The combination of a CPU with a flexible analog subsystem, digital subsystem, routing, and I/O enables a high level of integration in a wide variety of consumer, industrial, and medical applications.

Figure 1-1. Simplified Block Diagram

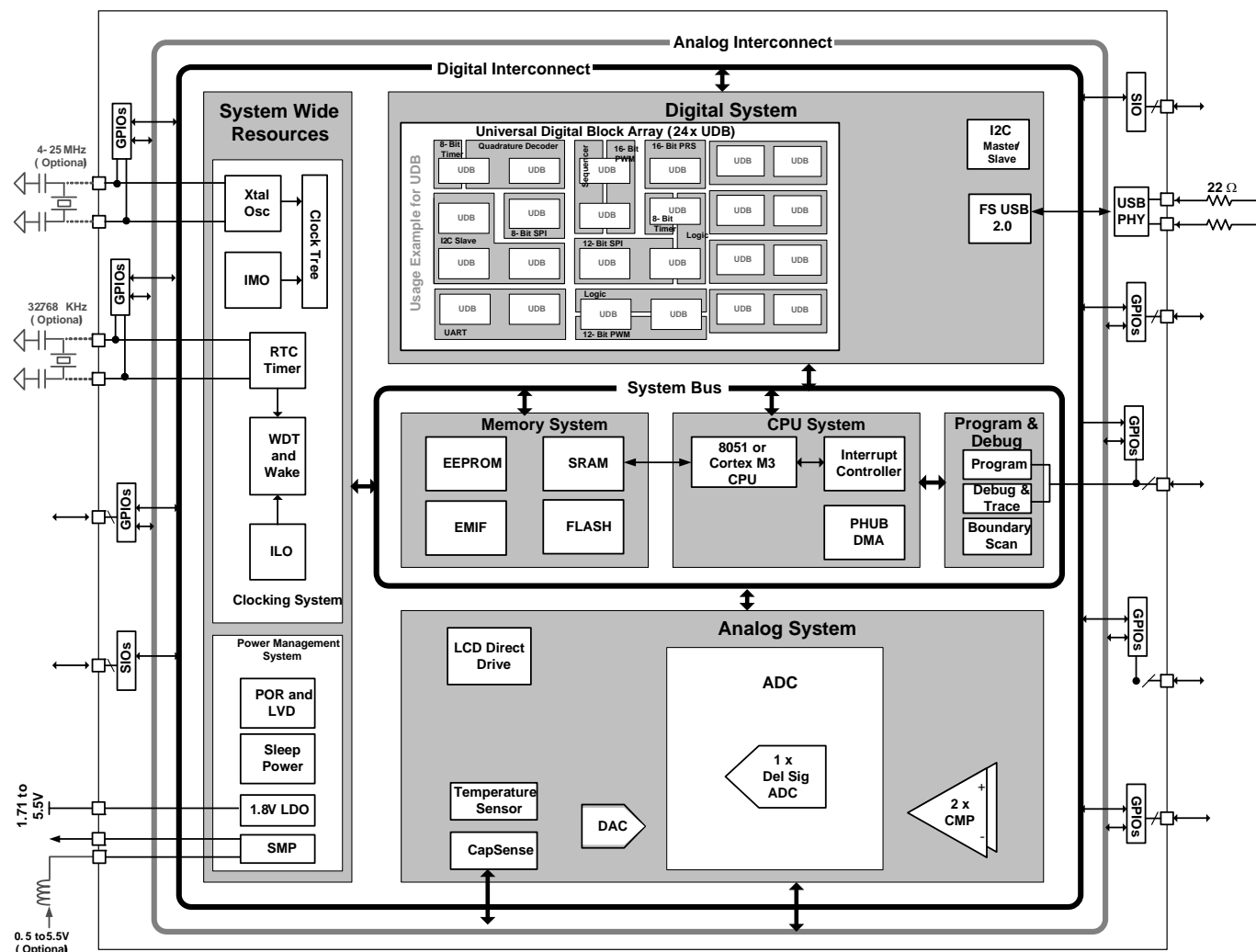


Figure 1-1 illustrates the major components of the CY8C32 family. They are:

- 8051 CPU subsystem
- Nonvolatile subsystem
- Programming, debug, and test subsystem
- Inputs and outputs
- Clocking
- Power
- Digital subsystem
- Analog subsystem

PSoC's digital subsystem provides half of its unique configurability. It connects a digital signal from any peripheral to any pin through the Digital System Interconnect (DSI). It also provides functional flexibility through an array of small, fast, low-power UDBs. PSoC Creator provides a library of prebuilt and tested standard digital peripherals (UART, SPI, LIN, PRS, CRC, timer, counter, PWM, AND, OR, and so on) that are mapped to the UDB array. You can also easily create a digital circuit using boolean primitives by means of graphical design entry. Each UDB contains programmable array logic (PAL)/programmable logic device (PLD) functionality, together with a small state machine engine to support a wide variety of peripherals.

This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1- μ A sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the “Power System” section on page 31 of this datasheet.

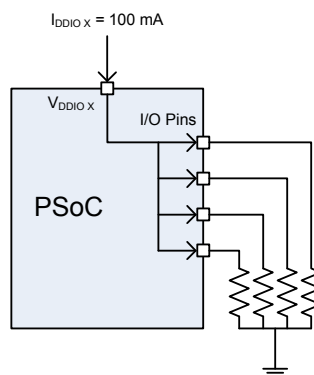
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for “printf” style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data cache memory for debug. Details of the programming, test, and debugging interfaces are discussed in the “Programming, Debug Interfaces, Resources” section on page 62 of this datasheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

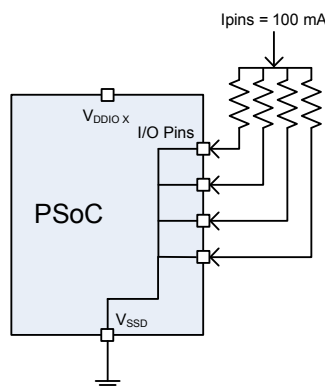
Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



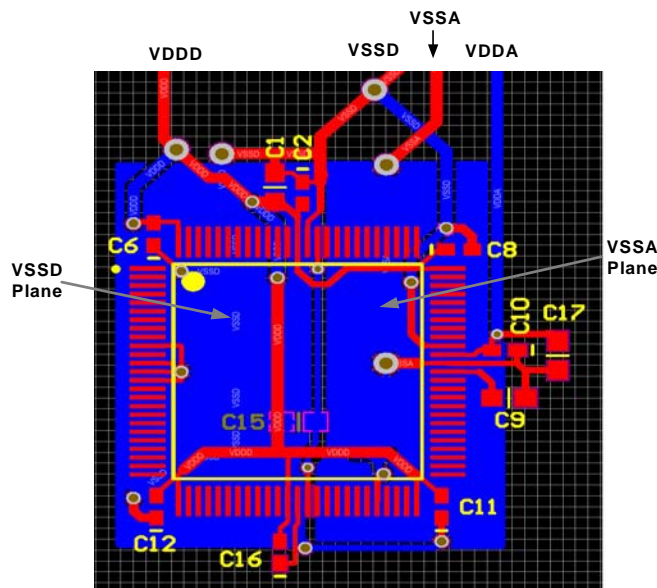
Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

Figure 2-8. Example PCB Layout for 100-pin TQFP Part for Optimal Analog Performance



3. Pin Descriptions

IDAC0

Low resistance output pin for high current DAC (IDAC).

Extref0, Extref1

External reference input to the analog system.

GPIO

General purpose I/O pin provides interfaces to the CPU, digital peripherals, analog peripherals, interrupts, LCD segment drive, and CapSense.

I2C0: SCL, I2C1: SCL

I²C SCL line providing wake from sleep on an address match. Any I/O pin can be used for I²C SCL if wake from sleep is not required.

I2C0: SDA, I2C1: SDA

I²C SDA line providing wake from sleep on an address match. Any I/O pin can be used for I²C SDA if wake from sleep is not required.

Ind

Inductor connection to boost pump.

kHz XTAL: Xo, kHz XTAL: Xi

32.768-kHz crystal oscillator pin.

MHz XTAL: Xo, MHz XTAL: Xi

4- to 25- MHz crystal oscillator pin.

nTRST

Optional JTAG test reset programming and debug port connection to reset the JTAG connection.

SIO

Special I/O provides interfaces to the CPU, digital peripherals and interrupts with a programmable high threshold voltage, analog comparator, high sink current, and high impedance state when the device is unpowered.

SWDCK

Serial wire debug clock programming and debug port connection.

SWDIO

Serial wire debug input and output programming and debug port connection.

SWV.

Single wire viewer debug output.

TCK

JTAG test clock programming and debug port connection.

TDI

JTAG test data in programming and debug port connection.

TDO

JTAG test data out programming and debug port connection.

TMS

JTAG test mode select programming and debug port connection.

4.3.1.2 Logical Instructions

The logical instructions perform Boolean operations such as AND, OR, XOR on bytes, rotate of accumulator contents, and swap of nibbles in an accumulator. The Boolean operations on the bytes are performed on the bit-by-bit basis. [Table 4-2](#) on page 15 shows the list of logical instructions and their description.

Table 4-2. Logical Instructions

Mnemonic	Description	Bytes	Cycles
ANL A,Rn	AND register to accumulator	1	1
ANL A,Direct	AND direct byte to accumulator	2	2
ANL A,@Ri	AND indirect RAM to accumulator	1	2
ANL A,#data	AND immediate data to accumulator	2	2
ANL Direct, A	AND accumulator to direct byte	2	3
ANL Direct, #data	AND immediate data to direct byte	3	3
ORL A,Rn	OR register to accumulator	1	1
ORL A,Direct	OR direct byte to accumulator	2	2
ORL A,@Ri	OR indirect RAM to accumulator	1	2
ORL A,#data	OR immediate data to accumulator	2	2
ORL Direct, A	OR accumulator to direct byte	2	3
ORL Direct, #data	OR immediate data to direct byte	3	3
XRL A,Rn	XOR register to accumulator	1	1
XRL A,Direct	XOR direct byte to accumulator	2	2
XRL A,@Ri	XOR indirect RAM to accumulator	1	2
XRL A,#data	XOR immediate data to accumulator	2	2
XRL Direct, A	XOR accumulator to direct byte	2	3
XRL Direct, #data	XOR immediate data to direct byte	3	3
CLR A	Clear accumulator	1	1
CPL A	Complement accumulator	1	1
RL A	Rotate accumulator left	1	1
RLC A	Rotate accumulator left through carry	1	1
RR A	Rotate accumulator right	1	1
RRC A	Rotate accumulator right though carry	1	1
SWAP A	Swap nibbles within accumulator	1	1

I/O ports are linked to the CPU through the PHUB and are also available in the SFRs. Using the SFRs allows faster access to a limited set of I/O port registers, while using the PHUB allows boot configuration and access to all I/O port registers.

Each SFR supported I/O port provides three SFRs:

- SFRPRTxDR sets the output data state of the port (where x is port number and includes ports 0 – 6, 12 and 15).
- The SFRPRTxSEL selects whether the PHUB PRTxDR register or the SFRPRTxDR controls each pin's output buffer within the port. If a SFRPRTxSEL[y] bit is high, the corresponding SFRPRTxDR[y] bit sets the output state for that pin. If a SFRPRTxSEL[y] bit is low, the corresponding PRTxDR[y] bit sets the output state of the pin (where y varies from 0 to 7).
- The SFRPRTxPS is a read only register that contains pin state values of the port pins.

5.7.4 xdata Space

The 8051 xdata space is 24-bit, or 16 MB in size. The majority of this space is not “external”—it is used by on-chip components. See [Table 5-5](#). External, that is, off-chip, memory can be accessed using the EMIF. See [External Memory Interface](#) on page 26.

Table 5-5. XDATA Data Address Map

Address Range	Purpose
0x00 0000 – 0x00 1FFF	SRAM
0x00 4000 – 0x00 42FF	Clocking, PLLs, and oscillators
0x00 4300 – 0x00 43FF	Power management
0x00 4400 – 0x00 44FF	Interrupt controller
0x00 4500 – 0x00 45FF	Ports interrupt control
0x00 4700 – 0x00 47FF	Flash programming interface
0x00 4800 – 0x00 48FF	Cache controller
0x00 4900 – 0x00 49FF	I ² C controller
0x00 4E00 – 0x00 4EFF	Decimator
0x00 4F00 – 0x00 4FFF	Fixed timer/counter/PWMs
0x00 5000 – 0x00 51FF	I/O ports control
0x00 5400 – 0x00 54FF	External Memory Interface (EMIF) control registers
0x00 5800 – 0x00 5FFF	Analog Subsystem interface
0x00 6000 – 0x00 60FF	USB controller
0x00 6400 – 0x00 6FFF	UDB Working Registers
0x00 7000 – 0x00 7FFF	PHUB configuration
0x00 8000 – 0x00 8FFF	EEPROM
0x01 0000 – 0x01 FFFF	Digital Interconnect configuration
0x05 0220 – 0x05 02F0	Debug controller
0x08 0000 – 0x08 1FFF	Flash ECC bytes
0x80 0000 – 0xFF FFFF	External Memory Interface

6. System Integration

6.1 Clocking System

The clocking system generates, divides, and distributes clocks throughout the PSoC system. For the majority of systems, no external crystal is required. The IMO and PLL together can generate up to a 50 MHz clock, accurate to ± 2 percent over voltage and temperature. Additional internal and external clock sources allow each design to optimize accuracy, power, and cost. Any of the clock sources can be used to generate other clock frequencies in the 16-bit clock dividers and UDBs for anything the user wants, for example a UART baud rate generator.

Clock generation and distribution is automatically configured through the PSoC Creator IDE graphical interface. This is based on the complete system's requirements. It greatly speeds the design process. PSoC Creator allows you to build clocking systems with minimal input. You can specify desired clock frequencies and accuracies, and the software locates or builds a clock that meets the required specifications. This is possible because of the programmability inherent in PSoC.

Key features of the clocking system include:

- Seven general purpose clock sources
 - 3- to 24-MHz IMO, ± 2 percent at 3 MHz
 - 4- to 25-MHz external crystal oscillator (MHzECO)
 - Clock doubler provides a doubled clock frequency output for the USB block, see [USB Clock Domain](#) on page 31
 - DSI signal from an external I/O pin or other logic
 - 24- to 50- MHz fractional PLL sourced from IMO, MHzECO, or DSI
 - 1-kHz, 33-kHz, 100-kHz ILO for watchdog timer (WDT) and sleep timer
 - 32.768-kHz external crystal oscillator (kHzECO) for RTC
- IMO has a USB mode that auto locks to the USB bus clock requiring no external crystal for USB. (USB equipped parts only)
- Independently sourced clock in all clock dividers
- Eight 16-bit clock dividers for the digital system
- Four 16-bit clock dividers for the analog system
- Dedicated 16-bit divider for the bus clock
- Dedicated 4-bit divider for the CPU clock
- Automatic clock configuration in PSoC Creator

6.2.1 Power Modes

PSoC 3 devices have four different power modes, as shown in [Table 6-2](#) and [Table 6-3](#). The power modes allow a design to easily provide required functionality and processing power while simultaneously minimizing power consumption and maximizing battery life in low-power and portable devices.

PSoC 3 power modes, in order of decreasing power consumption are:

- Active
- Alternate Active
- Sleep
- Hibernate

Active is the main processing mode. Its functionality is configurable. Each power controllable subsystem is enabled or disabled by using separate power configuration template registers. In alternate active mode, fewer subsystems are enabled, reducing power. In sleep mode most resources are disabled regardless of the template settings. Sleep mode is optimized to provide timed sleep intervals and RTC functionality. The lowest power mode is hibernate, which retains register and SRAM state, but no clocks, and allows wakeup only from I/O pins. [Figure 6-5](#) illustrates the allowable transitions between power modes. Sleep and hibernate modes should not be entered until all VDDIO supplies are at valid voltage levels.

Table 6-2. Power Modes

Power Modes	Description	Entry Condition	Wakeup Source	Active Clocks	Regulator
Active	Primary mode of operation, all peripherals available (programmable)	Wakeup, reset, manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Alternate Active	Similar to Active mode, and is typically configured to have fewer peripherals active to reduce power. One possible configuration is to use the UDBs for processing, with the CPU turned off	Manual register entry	Any interrupt	Any (programmable)	All regulators available. Digital and analog regulators can be disabled if external regulation used.
Sleep	All subsystems automatically disabled	Manual register entry	Comparator, PICU, I ² C, RTC, CTW, LVD	ILO/kHzECO	Both digital and analog regulators buzzed. Digital and analog regulators can be disabled if external regulation used.
Hibernate	All subsystems automatically disabled Lowest power consuming mode with all peripherals and internal regulators disabled, except hibernate regulator is enabled Configuration and memory contents retained	Manual register entry	PICU		Only hibernate regulator active.

Table 6-3. Power Modes Wakeup Time and Power Consumption

Sleep Modes	Wakeup Time	Current (typ)	Code Execution	Digital Resources	Analog Resources	Clock Sources Available	Wakeup Sources	Reset Sources
Active	–	1.2 mA ^[11]	Yes	All	All	All	–	All
Alternate Active	–	–	User defined	All	All	All	–	All
Sleep	<15 µs	1 µA	No	I ² C	Comparator	ILO/kHzECO	Comparator, PICU, I ² C, RTC, CTW, LVD	XRES, LVD, WDR
Hibernate	<100 µs	200 nA	No	None	None	None	PICU	XRES

Note

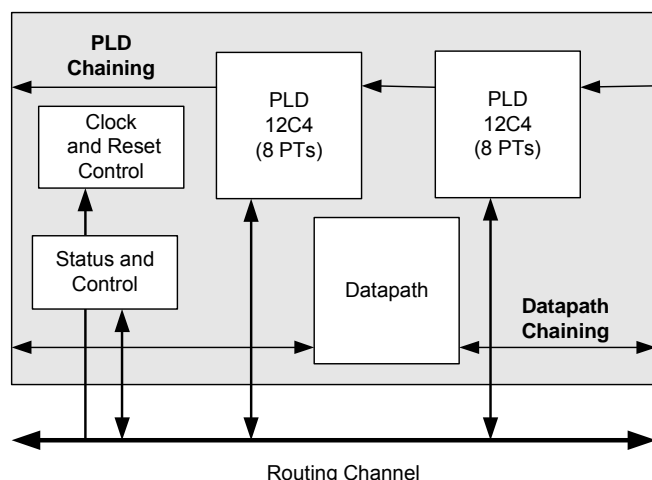
11. Bus clock off. Execute from cache at 6 MHz. See [Table 11-2](#) on page 68.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I²C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



The main component blocks of the UDB are:

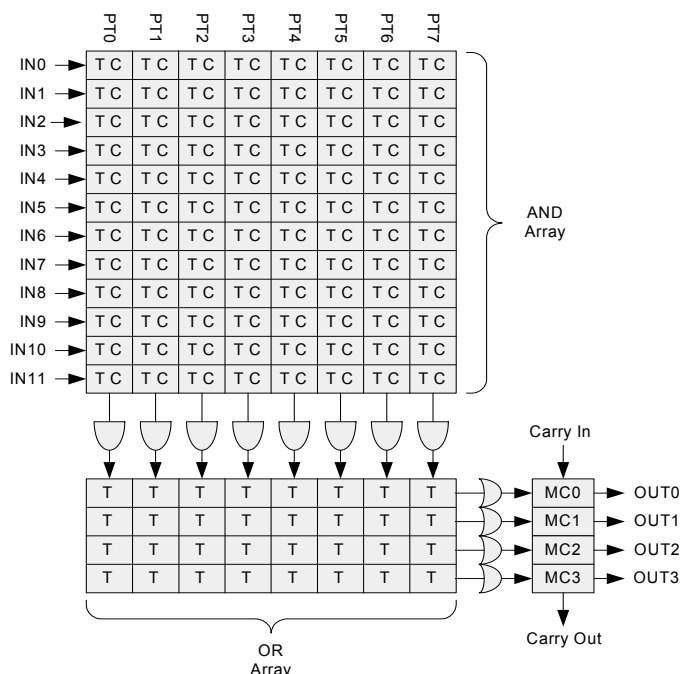
- **PLD blocks** – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- **Datapath Module** – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.

- **Status and Control Module** – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- **Clock and Reset Module** – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

More information on output formats is provided in the Technical Reference Manual.

8.2.3 Start of Conversion Input

The SoC signal is used to start an ADC conversion. A digital clock or UDB output can be used to drive this input. It can be used when the sampling period must be longer than the ADC conversion time or when the ADC must be synchronized to other hardware. This signal is optional and does not need to be connected if ADC is running in a continuous mode.

8.2.4 End of Conversion Output

The EoC signal goes high at the end of each ADC conversion. This signal may be used to trigger either an interrupt or DMA request.

8.3 Comparators

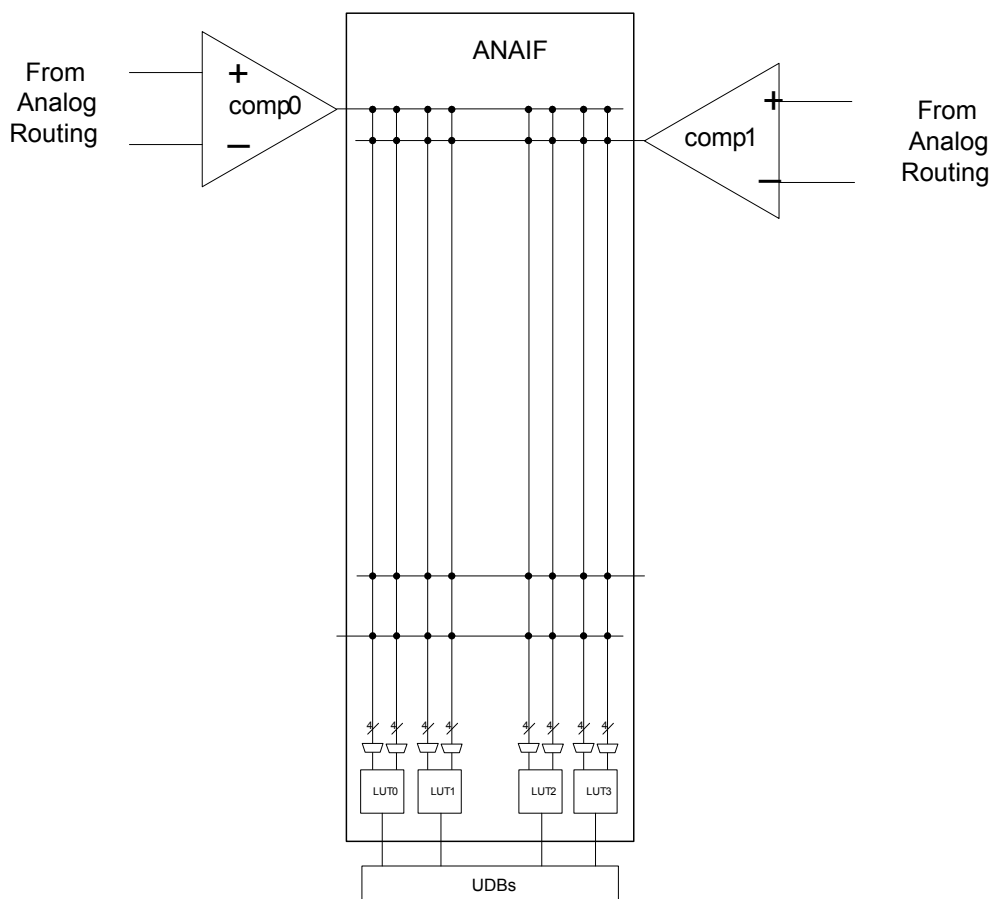
The CY8C32 family of devices contains two comparators in a device. Comparators have these features:

- Input offset factory trimmed to less than 5 mV
- Rail-to-rail common mode input range (VSSA to VDDA)
- Speed and power can be traded off by using one of three modes: fast, slow, or ultra low-power
- Comparator outputs can be routed to lookup tables to perform simple logic functions and then can also be routed to digital blocks
- The positive input of the comparators may be optionally passed through a low pass filter. Two filters are provided
- Comparator inputs can be connections to GPIO or DAC output

8.3.1 Input and Output Interface

The positive and negative inputs to the comparators come from the analog global buses, the analog mux line, the analog local bus and precision reference through multiplexers. The output from each comparator could be routed to any of the two input LUTs. The output of that LUT is routed to the UDB Digital System Interface.

Figure 8-5. Analog Comparator



8.3.2 LUT

The CY8C32 family of devices contains four LUTs. The LUT is a two input, one output lookup table that is driven by any one or two of the comparators in the chip. The output of any LUT is routed to the digital system interface of the UDB array. From the digital system interface of the UDB array, these signals can be connected to UDBs, DMA controller, I/O, or the interrupt controller.

The LUT control word written to a register sets the logic function on the output. The available LUT functions and the associated control word is shown in Table 8-2.

Table 8-2. LUT Function vs. Program Word and Inputs

Control Word	Output (A and B are LUT inputs)
0000b	FALSE ('0')
0001b	A AND B
0010b	A AND (NOT B)
0011b	A
0100b	(NOT A) AND B
0101b	B
0110b	A XOR B
0111b	A OR B
1000b	A NOR B
1001b	A XNOR B
1010b	NOT B
1011b	A OR (NOT B)
1100b	NOT A
1101b	(NOT A) OR B
1110b	A NAND B
1111b	TRUE ('1')

8.4 LCD Direct Drive

The PSoC Liquid Crystal Display (LCD) driver system is a highly configurable peripheral designed to allow PSoC to directly drive a broad range of LCD glass. All voltages are generated on chip, eliminating the need for external components. With a high multiplex ratio of up to 1/16, the CY8C32 family LCD driver system can drive a maximum of 736 segments. The PSoC LCD driver module was also designed with the conservative power budget of portable devices in mind, enabling different LCD drive modes and power down modes to conserve power.

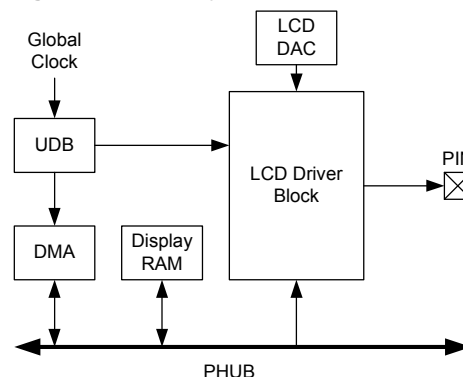
PSoC Creator provides an LCD segment drive component. The component wizard provides easy and flexible configuration of LCD resources. You can specify pins for segments and commons along with other options. The software configures the device to meet the required specifications. This is possible because of the programmability inherent to PSoC devices.

Key features of the PSoC LCD segment system are:

- LCD panel direct driving
- Type A (standard) and Type B (low-power) waveform support
- Wide operating voltage range support (2 V to 5 V) for LCD panels

- Static, 1/2, 1/3, 1/4, 1/5 bias voltage levels
- Internal bias voltage generation through internal resistor ladder
- Up to 62 total common and segment outputs
- Up to 1/16 multiplex for a maximum of 16 backplane/common outputs
- Up to 62 front plane/segment outputs for direct drive
- Drives up to 736 total segments (16 backplane × 46 front plane)
- Up to 64 levels of software controlled contrast
- Ability to move display data from memory buffer to LCD driver through DMA (without CPU intervention)
- Adjustable LCD refresh rate from 10 Hz to 150 Hz
- Ability to invert LCD display for negative image
- Three LCD driver drive modes, allowing power optimization

Figure 8-6. LCD System



8.4.1 LCD Segment Pin Driver

Each GPIO pin contains an LCD driver circuit. The LCD driver buffers the appropriate output of the LCD DAC to directly drive the glass of the LCD. A register setting determines whether the pin is a common or segment. The pin's LCD driver then selects one of the six bias voltages to drive the I/O pin, as appropriate for the display data.

8.4.2 Display Data Flow

The LCD segment driver system reads display data and generates the proper output voltages to the LCD glass to produce the desired image. Display data resides in a memory buffer in the system SRAM. Each time you need to change the common and segment driver voltages, the next set of pixel data moves from the memory buffer into the Port Data Registers via DMA.

8.4.3 UDB and LCD Segment Control

A UDB is configured to generate the global LCD control signals and clocking. This set of signals is routed to each LCD pin driver through a set of dedicated LCD global routing channels. In addition to generating the global LCD control signals, the UDB also produces a DMA request to initiate the transfer of the next frame of LCD data.

9.3 Debug Features

Using the JTAG or SWD interface, the CY8C32 supports the following debug features:

- Halt and single-step the CPU
- View and change CPU and peripheral registers, and RAM addresses
- Eight program address breakpoints
- One memory access breakpoint—break on reading or writing any memory address and data value
- Break on a sequence of breakpoints (non recursive)
- Debugging at the full speed of the CPU
- Compatible with PSoC Creator and MiniProg3 programmer and debugger
- Standard JTAG programming and debugging interfaces make CY8C32 compatible with other popular third-party tools (for example, ARM / Keil)

9.4 Trace Features

The CY8C32 supports the following trace features when using JTAG or SWD:

- Trace the 8051 program counter (PC), accumulator register (ACC), and one SFR / 8051 core RAM register
- Trace depth up to 1000 instructions if all registers are traced, or 2000 instructions if only the PC is traced (on devices that include trace memory)
- Program address trigger to start tracing
- Trace windowing, that is, only trace when the PC is within a given range
- Two modes for handling trace buffer full: continuous (overwriting the oldest trace data) or break when trace buffer is full

9.5 Single Wire Viewer Interface

The SWV interface is closely associated with SWD but can also be used independently. SWV data is output on the JTAG interface's TDO pin. If using SWV, you must configure the device for SWD, not JTAG. SWV is not supported with the JTAG interface.

SWV is ideal for application debug where it is helpful for the firmware to output data similar to 'printf' debugging on PCs. The SWV is ideal for data monitoring, because it requires only a single pin and can output data in standard UART format or Manchester encoded format. For example, it can be used to tune a PID control loop in which the output and graphing of the three error terms greatly simplifies coefficient tuning.

The following features are supported in SWV:

- 32 virtual channels, each 32 bits long
- Simple, efficient packing and serializing protocol
- Supports standard UART format (N81)

9.6 Programming Features

The JTAG and SWD interfaces provide full programming support. The entire device can be erased, programmed, and verified. You can increase flash protection levels to protect firmware IP. Flash protection can only be reset after a full device

erase. Individual flash blocks can be erased, programmed, and verified, if block security settings permit.

9.7 Device Security

PSoC 3 offers an advanced security feature called device security, which permanently disables all test, programming, and debug ports, protecting your application from external access. The device security is activated by programming a 32-bit key (0x50536F43) to a Write Once Latch (WOL).

The Write Once Latch is a type of nonvolatile latch (NVL). The cell itself is an NVL with additional logic wrapped around it. Each WOL device contains four bytes (32 bits) of data. The wrapper outputs a '1' if a super-majority (28 of 32) of its bits match a pre-determined pattern (0x50536F43); it outputs a '0' if this majority is not reached. When the output is 1, the Write Once NV latch locks the part out of Debug and Test modes; it also permanently gates off the ability to erase or alter the contents of the latch. Matching all bits is intentionally not required, so that single (or few) bit failures do not deassert the WOL output. The state of the NVL bits after wafer processing is truly random with no tendency toward 1 or 0.

The WOL only locks the part after the correct 32-bit key (0x50536F43) is loaded into the NVL's volatile memory, programmed into the NVL's nonvolatile cells, and the part is reset. The output of the WOL is only sampled on reset and used to disable the access. This precaution prevents anyone from reading, erasing, or altering the contents of the internal memory.

The user can write the key into the WOL to lock out external access only if no flash protection is set (see "Flash Security" on page 24). However, after setting the values in the WOL, a user still has access to the part until it is reset. Therefore, a user can write the key into the WOL, program the flash protection data, and then reset the part to lock it.

If the device is protected with a WOL setting, Cypress cannot perform failure analysis and, therefore, cannot accept RMAs from customers. The WOL can be read out via SWD port to electrically identify protected parts. The user can write the key in WOL to lock out external access only if no flash protection is set. For more information on how to take full advantage of the security features in PSoC see the PSoC 3 TRM.

Disclaimer

Note the following details of the flash code protection features on Cypress devices.

Cypress products meet the specifications contained in their particular Cypress datasheets. Cypress believes that its family of products is one of the most secure families of its kind on the market today, regardless of how they are used. There may be methods, unknown to Cypress, that can breach the code protection features. Any of these methods, to our knowledge, would be dishonest and possibly illegal. Neither Cypress nor any other semiconductor manufacturer can guarantee the security of their code. Code protection does not mean that we are guaranteeing the product as "unbreakable."

Cypress is willing to work with the customer who is concerned about the integrity of their code. Code protection is constantly evolving. We at Cypress are committed to continuously improving the code protection features of our products.

11.2 Device Level Specifications

Specifications are valid for $-40\text{ }^{\circ}\text{C} \leq T_A \leq 85\text{ }^{\circ}\text{C}$ and $T_J \leq 100\text{ }^{\circ}\text{C}$, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted.

11.2.1 Device Level Specifications

Table 11-2. DC Specifications

Parameter	Description	Conditions	Min	Typ ^[22]	Max	Units	
V _{DDA}	Analog supply voltage and input to analog core regulator	Analog core regulator enabled	1.8	–	5.5	V	
V _{DDA}	Analog supply voltage, analog regulator bypassed	Analog core regulator disabled	1.71	1.8	1.89	V	
V _{DDD}	Digital supply voltage relative to V _{SSD}	Digital core regulator enabled	1.8	–	V _{DDA} ^[18]	V	
			–	–	V _{DDA} + 0.1 ^[24]		
V _{DDD}	Digital supply voltage, digital regulator bypassed	Digital core regulator disabled	1.71	1.8	1.89	V	
V _{DDIO} ^[19]	I/O supply voltage relative to V _{SSIO}		1.71	–	V _{DDA} ^[18]	V	
			–	–	V _{DDA} + 0.1 ^[24]		
V _{CCA}	Direct analog core voltage input (Analog regulator bypass)	Analog core regulator disabled	1.71	1.8	1.89	V	
V _{CCD}	Direct digital core voltage input (Digital regulator bypass)	Digital core regulator disabled	1.71	1.8	1.89	V	
I _{DD} ^[20, 21]	Active Mode						
	Only IMO and CPU clock enabled. CPU executing simple loop from instruction buffer.	V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 6 MHz ^[23]	T = –40 °C	–	1.2	2.9	mA
			T = 25 °C	–	1.2	3.1	
			T = 85 °C	–	4.9	7.7	
	IMO enabled, bus clock and CPU clock enabled. CPU executing program from flash.	V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 3 MHz ^[23]	T = –40 °C	–	1.3	2.9	
			T = 25 °C	–	1.6	3.2	
			T = 85 °C	–	4.8	7.5	
		V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 6 MHz	T = –40 °C	–	2.1	3.7	
			T = 25 °C	–	2.3	3.9	
			T = 85 °C	–	5.6	8.5	
		V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 12 MHz ^[23]	T = –40 °C	–	3.5	5.2	
			T = 25 °C	–	3.8	5.5	
			T = 85 °C	–	7.1	9.8	
		V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 24 MHz ^[23]	T = –40 °C	–	6.3	8.1	
			T = 25 °C	–	6.6	8.3	
			T = 85 °C	–	10	13	
		V _{DDX} = 2.7 V – 5.5 V; F _{CPU} = 48 MHz ^[23]	T = –40 °C	–	11.5	13.5	
			T = 25 °C	–	12	14	
T = 85 °C			–	15.5	18.5		

Notes

18. The power supplies can be brought up in any sequence however once stable V_{DDA} must be greater than or equal to all other supplies.

19. The V_{DDIO} supply voltage must be greater than the maximum voltage on the associated GPIO pins. Maximum voltage on GPIO pin $\leq V_{DDIO} \leq V_{DDA}$.

20. Total current for all power domains: digital (I_{DDD}), analog (I_{DDA}), and I/Os ($I_{DDIO0, 1, 2, 3}$). Boost not included. All I/Os floating.

21. The current consumption of additional peripherals that are implemented only in programmed logic blocks can be found in their respective datasheets, available in PSoC Creator, the integrated design environment. To estimate total current, find the CPU current at the frequency of interest and add peripheral currents for your particular system from the device datasheet and component datasheets.

22. $V_{DDX} = 3.3\text{ V}$.

23. Based on device characterizations (Not production tested).

24. Guaranteed by design, not production tested.

Figure 11-1. Active Mode Current vs F_{CPU} , $V_{DD} = 3.3$ V, Temperature = 25 °C

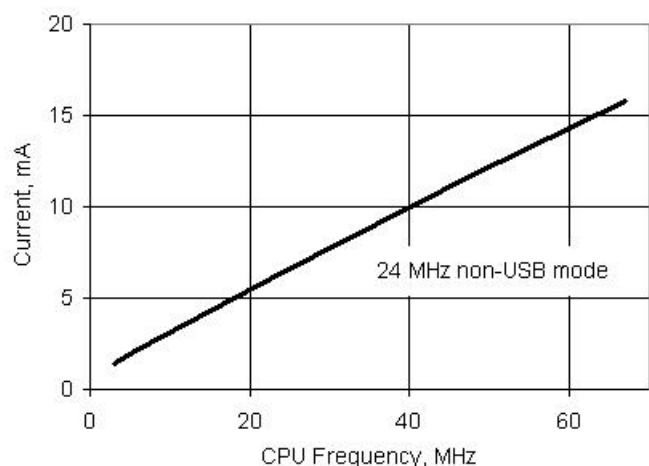


Figure 11-2. Active Mode Current vs Temperature and F_{CPU} , $V_{DD} = 3.3$ V

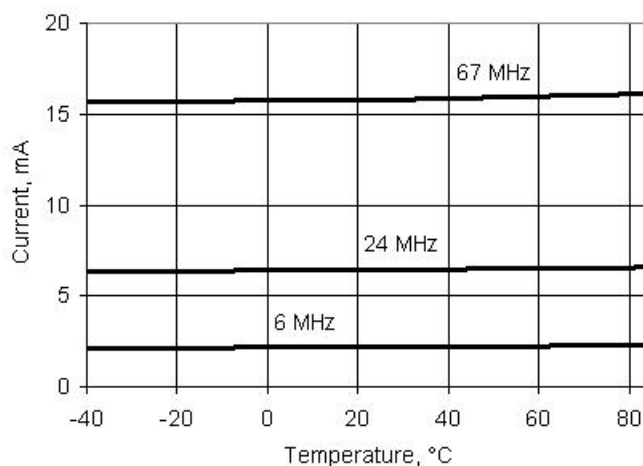
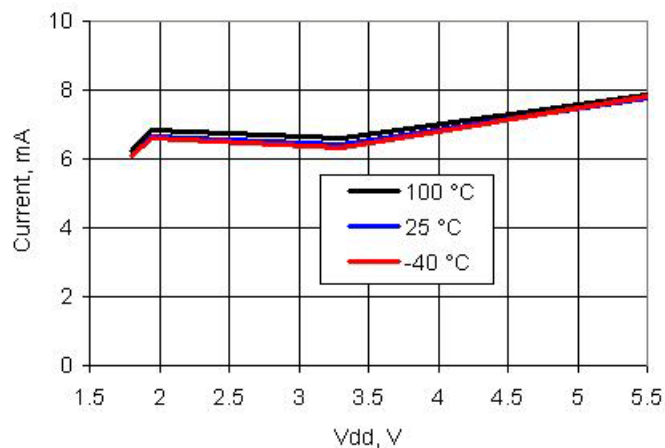


Figure 11-3. Active Mode Current vs V_{DD} and Temperature, $F_{CPU} = 24$ MHz



Notes

25. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
26. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
27. Externally regulated mode.
28. Based on device characterization (not production tested).
29. Based on device characterization (not production tested). USBIO pins tied to ground (V_{SSD}).

11.3.3 Inductive Boost Regulator

Unless otherwise specified, operating conditions are: $V_{BAT} = 0.5\text{ V} - 3.6\text{ V}$, $V_{OUT} = 1.8\text{ V} - 5.0\text{ V}$, $I_{OUT} = 0\text{ mA} - 50\text{ mA}$, $L_{BOOST} = 4.7\text{ }\mu\text{H} - 22\text{ }\mu\text{H}$, $C_{BOOST} = 22\text{ }\mu\text{F} \parallel 3 \times 1.0\text{ }\mu\text{F} \parallel 3 \times 0.1\text{ }\mu\text{F}$, $C_{BAT} = 22\text{ }\mu\text{F}$, $I_F = 1.0\text{ A}$. Unless otherwise specified, all charts and graphs show typical values.

Table 11-6. Inductive Boost Regulator DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{OUT}	Boost output voltage ^[31]	$v_{sel} = 1.8\text{ V}$ in register BOOST_CR0	1.71	1.8	1.89	V
		$v_{sel} = 1.9\text{ V}$ in register BOOST_CR0	1.81	1.90	2.00	V
		$v_{sel} = 2.0\text{ V}$ in register BOOST_CR0	1.90	2.00	2.10	V
		$v_{sel} = 2.4\text{ V}$ in register BOOST_CR0	2.16	2.40	2.64	V
		$v_{sel} = 2.7\text{ V}$ in register BOOST_CR0	2.43	2.70	2.97	V
		$v_{sel} = 3.0\text{ V}$ in register BOOST_CR0	2.70	3.00	3.30	V
		$v_{sel} = 3.3\text{ V}$ in register BOOST_CR0	2.97	3.30	3.63	V
		$v_{sel} = 3.6\text{ V}$ in register BOOST_CR0	3.24	3.60	3.96	V
		$v_{sel} = 5.0\text{ V}$ in register BOOST_CR0	4.50	5.00	5.50	V
V_{BAT}	Input voltage to boost ^[32]	$I_{OUT} = 0\text{ mA} - 5\text{ mA}$ $v_{sel} = 1.8\text{ V} - 2.0\text{ V}$, $T_A = 0\text{ }^\circ\text{C} - 70\text{ }^\circ\text{C}$	0.5	—	0.8	V
		$I_{OUT} = 0\text{ mA} - 15\text{ mA}$ $v_{sel} = 1.8\text{ V} - 5.0\text{ V}$ ^[33] , $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	1.6	—	3.6	V
		$I_{OUT} = 0\text{ mA} - 25\text{ mA}$ $v_{sel} = 1.8\text{ V} - 2.7\text{ V}$, $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	0.8	—	1.6	V
		$I_{OUT} = 0\text{ mA} - 50\text{ mA}$ $v_{sel} = 1.8\text{ V} - 3.3\text{ V}$ ^[33] , $T_A = -40\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	1.8	—	2.5	V
			1.3	—	2.5	V
			2.5	—	3.6	V
		$v_{sel} = 2.5\text{ V} - 5.0\text{ V}$ ^[33] , $T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$	—	—	—	—
I_{OUT}	Output current	$T_A = 0\text{ }^\circ\text{C} - 70\text{ }^\circ\text{C}$ $V_{BAT} = 0.5\text{ V} - 0.8\text{ V}$	0	—	5	mA
		$T_A = -10\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$ $V_{BAT} = 1.6\text{ V} - 3.6\text{ V}$ $V_{BAT} = 0.8\text{ V} - 1.6\text{ V}$ $V_{BAT} = 1.3\text{ V} - 2.5\text{ V}$ $V_{BAT} = 2.5\text{ V} - 3.6\text{ V}$	0	—	15	mA
			0	—	25	mA
			0	—	50	mA
			0	—	50	mA
		$T_A = -40\text{ }^\circ\text{C} - 85\text{ }^\circ\text{C}$ $V_{BAT} = 1.8\text{ V} - 2.5\text{ V}$	0	—	50	mA
I_{LPK}	Inductor peak current		—	—	700	mA
I_Q	Quiescent current	Boost active mode	—	250	—	μA
		Boost sleep mode, $I_{OUT} < 1\text{ }\mu\text{A}$	—	25	—	μA
Reg_{LOAD}	Load regulation		—	—	10	%
Reg_{LINE}	Line regulation		—	—	10	%

Notes

31. Listed v_{sel} options are characterized. Additional v_{sel} options are valid and guaranteed by design.

32. The boost will start at all valid V_{BAT} conditions including down to $V_{BAT} = 0.5\text{ V}$.

33. If V_{BAT} is greater than or equal to V_{OUT} boost setting, then V_{OUT} will be less than V_{BAT} due to resistive losses in the boost circuit.

12. Ordering Information

In addition to the features listed in [Table 12-1](#), every CY8C32 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C32 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C32 Family with Single Cycle 8051

Part Number	MCU Core				LCD Segment Drive	Analog							Digital				I/O ^[76]				Package	JTAG ID ^[77]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)		ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs ^[75]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3244AXI-153	50	16	2	0.5	✓	12-bit Del-Sig	1	2	0	0	–	✓	16	4	–	–	70	62	8	0	100-pin TQFP	0×1E099069
CY8C3244LTI-130	50	16	2	0.5	✓	12-bit Del-Sig	1	2	0	0	–	✓	16	4	–	–	46	38	8	0	68-pin QFN	0×1E082069
CY8C3244LTI-123	50	16	2	0.5	✓	12-bit Del-Sig	1	2	0	0	–	✓	16	4	–	–	29	25	4	0	48-pin QFN	0×1E07B069
CY8C3244PVI-133	50	16	2	0.5	✓	12-bit Del-Sig	1	2	0	0	–	✓	16	4	–	–	29	25	4	0	48-pin SSOP	0×1E085069
32 KB Flash																						
CY8C3245AXI-158	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	–	–	70	62	8	0	100-pin TQFP	0×1E09E069
CY8C3245LTI-163	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	–	–	46	38	8	0	68-pin QFN	0×1E0A3069
CY8C3245LTI-139	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	–	–	29	25	4	0	48-pin QFN	0×1E08B069
CY8C3245PVI-134	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	–	–	29	25	4	0	48-pin SSOP	0×1E086069
CY8C3245AXI-166	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	✓	–	72	62	8	2	100-pin TQFP	0×1E0A6069
CY8C3245LTI-144	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	✓	–	31	25	4	2	48-pin QFN	0×1E090069
CY8C3245PVI-150	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	✓	–	31	25	4	2	48-pin SSOP	0×1E096069
CY8C3245FNI-212	50	32	4	1	✓	12-bit Del-Sig	1	2	0	0	–	✓	20	4	–	–	46	38	8	0	72-pin WLCSP	0x1E0D4069
64 KB Flash																						
CY8C3246LTI-149	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	–	–	46	38	8	0	68-pin QFN	0×1E095069
CY8C3246PVI-147	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	✓	–	31	25	4	2	48-pin SSOP	0×1E093069
CY8C3246AXI-131	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	–	–	70	62	8	0	100-pin TQFP	0×1E083069
CY8C3246LTI-162	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	–	–	29	25	4	0	48-pin QFN	0×1E0A2069
CY8C3246PVI-122	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	–	–	29	25	4	0	48-pin SSOP	0×1E07A069
CY8C3246AXI-138	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	✓	–	72	62	8	2	100-pin TQFP	0×1E08A069
CY8C3246LTI-128	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	✓	–	48	38	8	2	68-pin QFN	0×1E080069
CY8C3246LTI-125	50	64	8	2	✓	12-bit Del-Sig	1	2	0	0	–	✓	24	4	✓	–	31	25	4	2	48-pin QFN	0×1E07D069
CY8C3246FNI-213	50	64	8	2	✓	12-bit Del-Sig	1	2	–	–	–	✓	24	4	–	–	46	38	8	–	72-pin WLCSP	0x1E0D5069

Notes

75. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the [Example Peripherals](#) on page 45 for more information on how UDBs can be used.

76. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the [I/O System and Routing](#) on page 37 for details on the functionality of each of these types of I/O.

77. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.



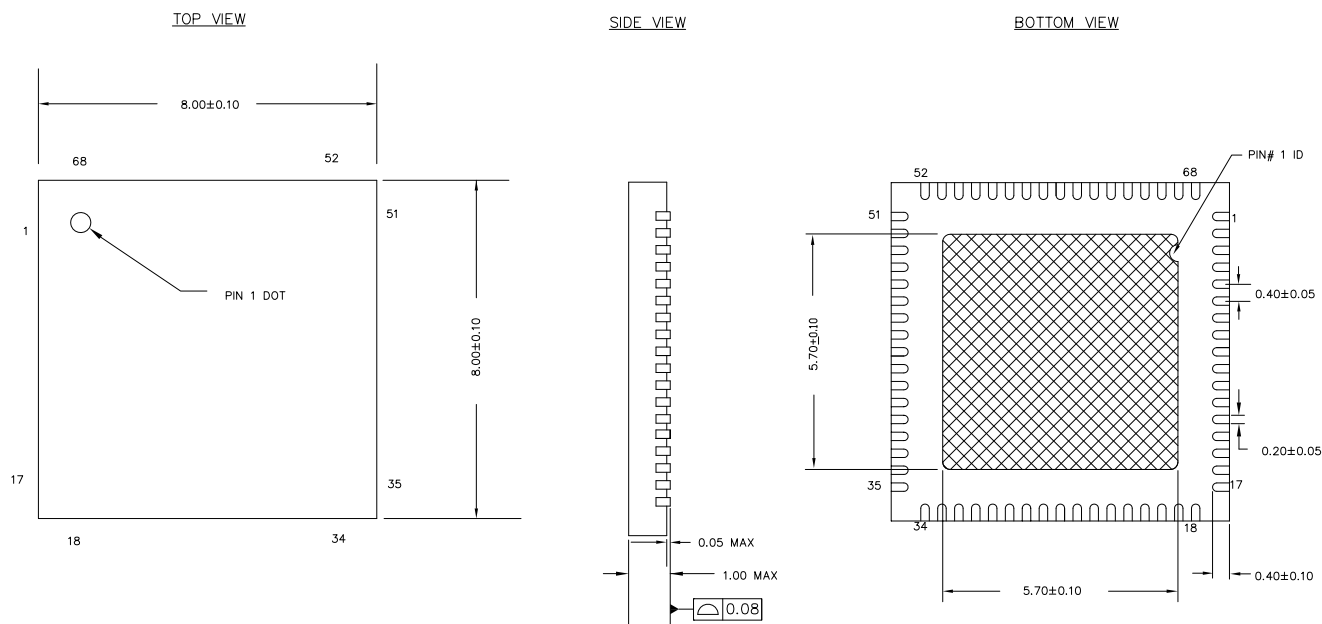
CY8Cabcdefg-xxx

- a: Architecture
 - 3: PSoC 3
 - 5: PSoC 5
- b: Family group within architecture
 - 2: CY8C32 family
 - 4: CY8C34 family
 - 6: CY8C36 family
 - 8: CY8C38 family
- c: Speed grade
 - 4: 50 MHz
 - 6: 67 MHz
- d: Flash capacity
 - 4: 16 KB
 - 5: 32 KB
 - 6: 64 KB
- ef: Package code
 - Two character alphanumeric
 - AX: TQFP
 - LT: QFN
 - PV: SSOP
 - FN: CSP
- g: Temperature range
 - C: commercial
 - I: industrial
 - A: automotive
- xxx: Peripheral set
 - Three character numeric
 - No meaning is associated with these three characters.

[illegible]

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

Figure 13-3. 68-pin QFN 8x8 with 0.4 mm Pitch Package Outline (Sawn Version)

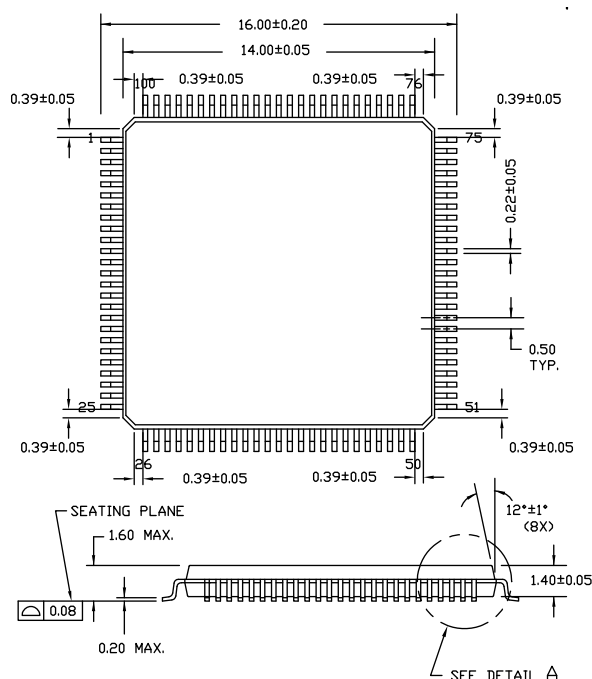


NOTES:

1. HATCH AREA IS SOLDERABLE EXPOSED METAL.
2. REFERENCE JEDEC#: MO-220
3. PACKAGE WEIGHT: 17 ± 2mg
4. ALL DIMENSIONS ARE IN MILLIMETERS

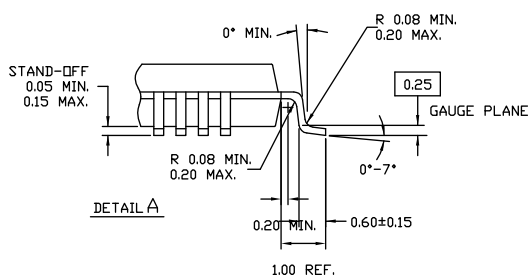
001-09618 *E

Figure 13-4. 100-pin TQFP (14 x 14 x 1.4 mm) Package Outline

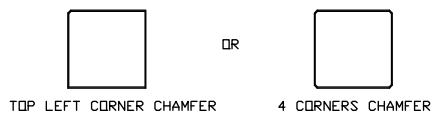


NOTE:

1. JEDEC STD REF MS-026
2. BODY LENGTH DIMENSION DOES NOT INCLUDE MOLD PROTRUSION/END FLASH
MOLD PROTRUSION/END FLASH SHALL NOT EXCEED 0.0098 in (0.25 mm) PER SIDE
BODY LENGTH DIMENSIONS ARE MAX PLASTIC BODY SIZE INCLUDING MOLD MISMATCH
3. DIMENSIONS IN MILLIMETERS



NOTE: PKG. CAN HAVE



51-85048 *J

17. Revision History

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) Document Number: 001-56955				
Revision	ECN	Submission Date	Orig. of Change	Description of Change
**	2796903	11/04/09	MKEA	New datasheet
*A	2824546	12/09/09	MKEA	Updated I2C section to reflect 1 Mbps. Updated Table 11-6 and 11-7 (Boost AC and DC specs); also added Shottky Diode specs. Changed current for sleep/hibernate mode to include SIO; Added footnote to analog global specs. Updated Figures 1-1, 6-2, 7-14, and 8-1. Updated Table 6-2 and Table 6-3 (Hibernate and Sleep rows) and Power Modes section. Updated GPIO and SIO AC specifications. Updated Gain error in IDAC and VDAC specifications. Updated description of V _{DDA} spec in Table 11-1 and removed GPIO Clamp Current parameter. Updated number of UDBs on page 1. Moved FILO from ILO DC to AC table. Added PCB Layout and PCB Schematic diagrams. Updated Fgpiout spec (Table 11-9). Added duty cycle frequency in PLL AC spec table. Added note for Sleep and Hibernate modes and Active Mode specs in Table 11-2. Linked URL in Section 10.3 to PSoC Creator site. Updated Ja and Jc values in Table 13-1. Updated Single Sample Mode and Fast FIR Mode sections. Updated Input Resistance specification in Del-Sig ADC table. Added Tio_init parameter. Updated PGA and UGB AC Specs. Removed SPC ADC. Updated Boost Converter section. Added section 'SIO as Comparator'; updated Hysteresis spec (differential mode) in Table 11-10. Updated V _{BAT} condition and deleted Vstart parameter in Table 11-6. Added 'Bytes' column for Tables 4-1 to 4-5.
*B	2873322	02/04/10	MKEA	Changed maximum value of PPOR_TR to '1'. Updated V _{BIAS} specification. Updated PCB Schematic. Updated Figure 8-1 and Figure 6-3. Updated Interrupt Vector table, Updated Sales links. Updated JTAG and SWD specifications. Removed Jp-p and Jperiod from ECO AC Spec table. Added note on sleep timer in Table 11-2. Updated ILO AC and DC specifications. Added Resolution parameter in VDAC and IDAC tables. Updated I _{OUT} typical and maximum values. Changed Temperature Sensor range to -40 °C to +85 °C. Removed Latchup specification from Table 11-1. Updated DAC details

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) (continued)
Document Number: 001-56955

Revision	ECN	Submission Date	Orig. of Change	Description of Change
*D	2938381	05/27/10	MKEA	<p>Replaced V_{DDIO} with V_{DDD} in USBIO diagram and specification tables, added text in USBIO section of Electrical Specifications.</p> <p>Added Table 13-2 (Package MSL)</p> <p>Modified Tstorag condition and changed max spec to 100</p> <p>Added bullet (Pass) under ALU (section 7.2.2.2)</p> <p>Added figures for kHzECO and MHzECO in the External Oscillator section</p> <p>Updated Figure 6-1(Clocking Subsystem diagram)</p> <p>Removed CPUCLK_DIV in table 5-2, Deleted Clock Divider SFR subsection</p> <p>Updated PSoC Creator Framework image</p> <p>Updated SIO DC Specifications (V_{IH} and V_{IL} parameters)</p> <p>Updated bullets in Clocking System and Clocking Distribution sections</p> <p>Updated Figure 8-2</p> <p>Updated Table 11-10</p> <p>Updated PCB Layout and Schematic, updated as per MTRB review comments</p> <p>Updated Table 6-3 (power changed to current)</p> <p>In 32kHz EC DC Specifications table, changed I_{CC} Max to 0.25</p> <p>In IMO DC Specifications table, updated Supply Current values</p> <p>Updated GPIO DC Specs table</p> <p>Modified to support a maximum 50MHz CPU speed</p>
*E	2958674	06/22/10	SHEA	Minor ECN to post datasheet to external website
*F	2989685	08/04/10	MKEA	<p>Added USBIO 22 ohm DP and DM resistors to Simplified Block Diagram</p> <p>Added to Table 6-6 a footnote and references to same.</p> <p>Added sentences to the resistive pull-up and pull-down description bullets.</p> <p>Added sentence to Section 6.4.11, Adjustable Output Level.</p> <p>Updated section 5.5 External Memory Interface</p> <p>Updated Table 11-73 JTAG Interface AC Specifications</p> <p>Updated Table 11-74 SWD Interface AC Specifications</p>
*G	3078568	11/04/10	MKEA	<p>Updated "Current Digital-to-analog Converter (IDAC)" on page 87</p> <p>Updated "Voltage Digital to Analog Converter (VDAC)" on page 92</p> <p>Updated Table 11-2, "DC Specifications," on page 68</p>
*H	3107314	12/10/2010	MKEA	<p>Updated delta-sigma tables and graphs.</p> <p>Updated Flash AC specs</p> <p>Formatted table 11.2.</p> <p>Updated interrupt controller table</p> <p>Updated transimpedance amplifier section</p> <p>Updated SIO DC specs table</p> <p>Updated Voltage Monitors DC Specifications table</p> <p>Updated LCD Direct Drive DC specs table</p> <p>Updated ESD_{HBM} value.</p> <p>Updated IDAC and VDAC sections</p> <p>Removed ESO parts from ordering information</p> <p>Changed USBIO pins from NC to DNU and removed redundant USBIO pin description notes</p> <p>Updated POR with brown out DC and AC specs</p> <p>Updated 32 kHz External Crystal DC Specifications</p> <p>Updated XRES IO specs</p> <p>Updated Inductive boost regulator section</p> <p>Delta sigma ADC spec updates</p> <p>Updated comparator section</p> <p>Removed buzz mode from Power Mode Transition diagram</p>
*I	3179219	02/22/2011	MKEA	<p>Updated conditions for flash data retention time.</p> <p>Updated 100-pin TQFP package spec.</p> <p>Updated EEPROM AC specifications.</p>

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*J	3200146	03/28/2011	MKEA	<p>Removed Preliminary status from the data sheet.</p> <p>Updated JTAG ID</p> <p>Deleted Cin_G1, ADC input capacitance from Delta-Sigma ADC DC spec table</p> <p>Updated JTAG Interface AC Specifications and SWD Interface Specifications tables</p> <p>Updated USBIO DC specs</p> <p>Added 0.01 to max speed</p> <p>Updated Features on page 1</p> <p>Added Section 5.5, Nonvolatile Latches</p> <p>Updated Flash AC specs</p> <p>Updated delta-sigma graphs, noise histogram figures and RMS Noise spec tables</p> <p>Add reference to application note AN58304 in section 8.1</p> <p>Updated 100-pin TQFP package spec</p> <p>Added oscillator, I/O, VDAC, regulator graphs</p> <p>Updated JTAG/SWD timing diagrams</p> <p>Updated GPIO and SIO AC specs</p> <p>Updated POR with Brown Out AC spec table</p> <p>Updated IDAC graphs</p> <p>Added DMA timing diagram, interrupt timing and interrupt vector, I2C timing diagrams</p> <p>Added full chip performance graphs</p> <p>Changed MHzECO range.</p> <p>Added "Solder Reflow Peak Temperature" table.</p>
*K	3259185	05/17/2011	MKEA	<p>Added JTAG and SWD interface connection diagrams</p> <p>Updated T_{JA} and T_{JC} values in Table 13-1</p> <p>Changed typ and max values for the TC_{Vos} parameter in Opamp DC specifications table.</p> <p>Updated Clocking subsystem diagram.</p> <p>Changed VSSD to VSSB in the PSoC Power System diagram</p> <p>Updated Ordering information.</p>