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What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	8051
Core Size	8-Bit
Speed	50MHz
Connectivity	EBI/EMI, I²C, LINbus, SPI, UART/USART
Peripherals	CapSense, DMA, LCD, POR, PWM, WDT
Number of I/O	25
Program Memory Size	64KB (64K x 8)
Program Memory Type	FLASH
EEPROM Size	2K x 8
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	1.71V ~ 5.5V
Data Converters	A/D 16x12b; D/A 1x8b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	48-BSSOP (0.295", 7.50mm Width)
Supplier Device Package	48-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/infineon-technologies/cy8c3246pvi-122t

Contents

In addition to the flexibility of the UDB array, PSoC also provides configurable digital blocks targeted at specific functions. For the CY8C32 family these blocks can include four 16-bit timers, counters, and PWM blocks; I^2C slave, master, and multimaster; and FS USB.

For more details on the peripherals see the "Example Peripherals" section on page 45 of this datasheet. For information on UDBs, DSI, and other digital blocks, see the "Digital Subsystem" section on page 45 of this datasheet.

PSoC's analog subsystem is the second half of its unique configurability. All analog performance is based on a highly accurate absolute voltage reference with less than 1-percent error over temperature and voltage. The configurable analog subsystem includes:

- Analog muxes
- Comparators
- Voltage references
- ADC
- DAC

All GPIO pins can route analog signals into and out of the device using the internal analog bus. This allows the device to interface up to 62 discrete analog signals. The heart of the analog subsystem is a fast, accurate, configurable delta-sigma ADC with these features:

- Less than 100 µV offset
- A gain error of 0.2 percent
- INL less than ±1 LSB
- DNL less than ±1 LSB
- SINAD better than 66 dB

This converter addresses a wide variety of precision analog applications, including some of the most demanding sensors.

A high-speed voltage or current DAC supports 8-bit output signals at an update rate of 8 Msps in current DAC (IDAC) and 1 Msps in voltage DAC (VDAC). It can be routed out of any GPIO pin. You can create higher resolution voltage PWM DAC outputs using the UDB array. This can be used to create a pulse width modulated (PWM) DAC of up to 10 bits, at up to 48 kHz. The digital DACs in each UDB support PWM, PRS, or delta-sigma algorithms with programmable widths.

In addition to the ADC and DAC, the analog subsystem provides multiple comparators.

See the "Analog Subsystem" section on page 55 of this datasheet for more details.

PSoC's 8051 CPU subsystem is built around a single cycle pipelined 8051 8-bit processor running at up to 50 MHz. The CPU subsystem includes a programmable nested vector interrupt controller, DMA controller, and RAM. PSoC's nested vector interrupt controller provides low latency by allowing the CPU to vector directly to the first address of the interrupt service routine, bypassing the jump instruction required by other architectures. The DMA controller enables peripherals to exchange data without CPU involvement. This allows the CPU to run slower (saving power) or use those CPU cycles to improve the performance of firmware algorithms. The single cycle 8051 CPU runs ten times faster than a standard 8051 processor. The processor speed itself is configurable, allowing you to tune active power consumption for specific applications.

PSoC's nonvolatile subsystem consists of flash, byte-writeable EEPROM, and nonvolatile configuration options. It provides up to 64 KB of on-chip flash. The CPU can reprogram individual blocks of flash, enabling bootloaders. You can enable an ECC for high reliability applications. A powerful and flexible protection model secures the user's sensitive information, allowing selective memory block locking for read and write protection. Up to 2 KB of byte-writeable EEPROM is available on-chip to store application data. Additionally, selected configuration options such as boot speed and pin drive mode are stored in nonvolatile memory. This allows settings to activate immediately after POR.

The three types of PSoC I/O are extremely flexible. All I/Os have many drive modes that are set at POR. PSoC also provides up to four I/O voltage domains through the VDDIO pins. Every GPIO has analog I/O, LCD drive[3], CapSense[4], flexible interrupt generation, slew rate control, and digital I/O capability. The SIOs on PSoC allow Voh to be set independently of VDDIO when used as outputs. When SIOs are in input mode they are high impedance. This is true even when the device is not powered or when the pin voltage goes above the supply voltage. This makes the SIO ideally suited for use on an I^2C bus where the PSoC may not be powered when other devices on the bus are. The SIO pins also have high current sink capability for applications such as LED drives. The programmable input threshold feature of the SIO can be used to make the SIO function as a general purpose analog comparator. For devices with FS USB the USB physical interface is also provided (USBIO). When not using USB these pins may also be used for limited digital functionality and device programming. All of the features of the PSoC I/Os are covered in detail in the "I/O System and Routing" section on page 37 of this datasheet.

The PSoC device incorporates flexible internal clock generators, designed for high stability and factory trimmed for high accuracy. The Internal Main Oscillator (IMO) is the clock base for the system, and has 2-percent accuracy at 3 MHz. The IMO can be configured to run from 3 MHz up to 24 MHz. Multiple clock derivatives can be generated from the main clock frequency to meet application needs. The device provides a PLL to generate clock frequencies up to 50 MHz from the IMO, external crystal, or external reference clock. It also contains a separate, very low-power Internal Low-Speed Oscillator (ILO) for the sleep and watchdog timers. A 32.768-kHz external watch crystal is also supported for use in RTC applications. The clocks, together with programmable clock dividers, provide the flexibility to integrate most timing requirements.

The CY8C32 family supports a wide supply operating range from 1.71 V to 5.5 V. This allows operation from regulated supplies such as 1.8 ± 5 percent, 2.5 V ±10 percent, 3.3 V ± 10 percent, or 5.0 V ± 10 percent, or directly from a wide range of battery types. In addition, it provides an integrated high efficiency synchronous boost converter that can power the device from supply voltages as low as 0.5 V.

Notes
3. This feature on select devices only. See Ordering Information on page 111 for details.
4. GPIOs with opamp outputs are not recommended for use with CapSense.

This enables the device to be powered directly from a single battery or solar cell. In addition, you can use the boost converter to generate other voltages required by the device, such as a 3.3-V supply for LCD glass drive. The boost's output is available on the V_{BOOST} pin, allowing other devices in the application to be powered from the PSoC.

PSoC supports a wide range of low-power modes. These include a 200-nA hibernate mode with RAM retention and a 1-µA sleep mode with RTC. In the second mode the optional 32.768-kHz watch crystal runs continuously and maintains an accurate RTC.

Power to all major functional blocks, including the programmable digital and analog peripherals, can be controlled independently by firmware. This allows low-power background processing when some peripherals are not in use. This, in turn, provides a total device current of only 1.2 mA when the CPU is running at 6 MHz, or 0.8 mA running at 3 MHz.

The details of the PSoC power modes are covered in the "Power System" section on page 31 of this datasheet.

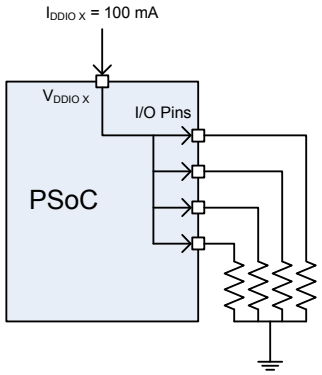
PSoC uses JTAG (4-wire) or SWD (2-wire) interfaces for programming, debug, and test. The 1-wire SWV may also be used for "printf" style debugging. By combining SWD and SWV, you can implement a full debugging interface with just three pins. Using these standard interfaces enables you to debug or program the PSoC with a variety of hardware solutions from Cypress or third party vendors. PSoC supports on-chip break points and 4-KB instruction and data race memory for debug. Details of the programming, test, and debugging interfaces are discussed in the "Programming, Debug Interfaces, Resources" section on page 62 of this datasheet.

2. Pinouts

Each VDDIO pin powers a specific set of I/O pins. (The USBIOs are powered from VDDD.) Using the VDDIO pins, a single PSoC can support multiple voltage levels, reducing the need for off-chip level shifters. The black lines drawn on the pinout diagrams in Figure 2-3 through Figure 2-6, as well as Table 2-1, show the pins that are powered by each VDDIO.

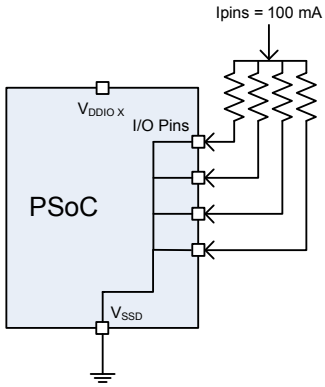
Each VDDIO may source up to 100 mA total to its associated I/O pins, as shown in Figure 2-1.

Figure 2-1. VDDIO Current Limit



Conversely, for the 100-pin and 68-pin devices, the set of I/O pins associated with any VDDIO may sink up to 100 mA total, as shown in Figure 2-2.

Figure 2-2. I/O Pins Current Limit



For the 48-pin devices, the set of I/O pins associated with VDDIO0 plus VDDIO2 may sink up to 100 mA total. The set of I/O pins associated with VDDIO1 plus VDDIO3 may sink up to a total of 100 mA.

4.3.1.3 Data Transfer Instructions

The data transfer instructions are of three types: the core RAM, xdata RAM, and the lookup tables. The core RAM transfer includes transfer between any two core RAM locations or SFRs. These instructions can use direct, indirect, register, and immediate addressing. The xdata RAM transfer includes only the transfer between the accumulator and the xdata RAM location. It can use only indirect addressing. The lookup tables involve nothing but the read of program memory using the Indexed addressing mode. Table 4-3 lists the various data transfer instructions available.

4.3.1.4 Boolean Instructions

The 8051 core has a separate bit-addressable memory location. It has 128 bits of bit addressable RAM and a set of SFRs that are bit addressable. The instruction set includes the whole menu of bit operations such as move, set, clear, toggle, OR, and AND instructions and the conditional jump instructions. Table 4-4 on page 17Table 4-4 lists the available Boolean instructions.

Table 4-3. Data Transfer Instructions

Mnemonic	Description	Bytes	Cycles
MOV A,Rn	Move register to accumulator	1	1
MOV A,Direct	Move direct byte to accumulator	2	2
MOV A,@Ri	Move indirect RAM to accumulator	1	2
MOV A,#data	Move immediate data to accumulator	2	2
MOV Rn,A	Move accumulator to register	1	1
MOV Rn,Direct	Move direct byte to register	2	3
MOV Rn, #data	Move immediate data to register	2	2
MOV Direct, A	Move accumulator to direct byte	2	2
MOV Direct, Rn	Move register to direct byte	2	2
MOV Direct, Direct	Move direct byte to direct byte	3	3
MOV Direct, @Ri	Move indirect RAM to direct byte	2	3
MOV Direct, #data	Move immediate data to direct byte	3	3
MOV @Ri, A	Move accumulator to indirect RAM	1	2
MOV @Ri, Direct	Move direct byte to indirect RAM	2	3
MOV @Ri, #data	Move immediate data to indirect RAM	2	2
MOV DPTR, #data16	Load data pointer with 16-bit constant	3	3
MOVC A, @A+DPTR	Move code byte relative to DPTR to accumulator	1	5
MOVC A, @A + PC	Move code byte relative to PC to accumulator	1	4
MOVX A,@Ri	Move external RAM (8-bit) to accumulator	1	4
MOVX A, @DPTR	Move external RAM (16-bit) to accumulator	1	3
MOVX @Ri, A	Move accumulator to external RAM (8-bit)	1	5
MOVX @DPTR, A	Move accumulator to external RAM (16-bit)	1	4
PUSH Direct	Push direct byte onto stack	2	3
POP Direct	Pop direct byte from stack	2	2
XCH A, Rn	Exchange register with accumulator	1	2
XCH A, Direct	Exchange direct byte with accumulator	2	3
XCH A, @Ri	Exchange indirect RAM with accumulator	1	3
XCHD A, @Ri	Exchange low order indirect digit RAM with accumulator	1	3

The term **device reset** indicates that the processor as well as analog and digital peripherals and registers are reset.

A reset status register shows some of the resets or power voltage monitoring interrupts. The program may examine this register to detect and report certain exception conditions. This register is cleared after a power-on reset. For details see the Technical Reference Manual.

6.3.1 Reset Sources

6.3.1.1 Power Voltage Level Monitors

- IPOR – Initial Power-on Reset

  At initial power on, IPOR monitors the power voltages VDDD, VDDA, VCCD, and VCCA. The trip level is not precise. It is set to approximately 1 volt, which is below the lowest specified operating voltage but high enough for the internal circuits to be reset and to hold their reset state. The monitor generates a reset pulse that is at least 150 ns wide. It may be much wider if one or more of the voltages ramps up slowly.

  After boot, the IPOR circuit is disabled and voltage supervision is handed off to the precise low-voltage reset (PRES) circuit.

- PRES – Precise Low Voltage Reset

  This circuit monitors the outputs of the analog and digital internal regulators after power up. The regulator outputs are compared to a precise reference voltage. The response to a PRES trip is identical to an IPOR reset.

  In normal operating mode, the program cannot disable the digital PRES circuit. The analog regulator can be disabled, which also disables the analog portion of the PRES. The PRES circuit is disabled automatically during sleep and hibernate modes, with one exception: During sleep mode the regulators are periodically activated (buzzed) to provide supervisory services and to reduce wakeup time. At these times the PRES circuit is also buzzed to allow periodic voltage monitoring.

- ALVI, DLVI, AHVI – Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

  Interrupt circuits are available to detect when VDDA and VDDD go outside a voltage range. For AHVI, VDDA is compared to a fixed trip level. For ALVI and DLVI, VDDA and VDDD are compared to trip levels that are programmable, as listed in Table 6-5. ALVI and DLVI can also be configured to generate a device reset instead of an interrupt.

Table 6-5. Analog/Digital Low Voltage Interrupt, Analog High Voltage Interrupt

Interrupt	Supply	Normal Voltage Range	Available Trip Settings
DLVI	VDDD	1.71 V – 5.5 V	1.70 V – 5.45 V in 250 mV increments
ALVI	VDDA	1.71 V – 5.5 V	1.70 V – 5.45 V in 250 mV increments
AHVI	VDDA	1.71 V – 5.5 V	5.75 V

The monitors are disabled until after IPOR. During sleep mode these circuits are periodically activated (buzzed). If an interrupt occurs during buzzing then the system first enters its wake up sequence. The interrupt is then recognized and may be serviced.

The buzz frequency is adjustable, and should be set to be less than the minimum time that any voltage is expected to be out of range. For details on how to adjust the buzz frequency, see the TRM.

6.3.1.2 Other Reset Sources

- XRES – External Reset

  PSoC 3 has either a single GPIO pin that is configured as an external reset or a dedicated XRES pin. Either the dedicated XRES pin or the GPIO pin, if configured, holds the part in reset while held active (low). The response to an XRES is the same as to an IPOR reset.

  After XRES has been deasserted, at least 10 µs must elapse before it can be reasserted.

  The external reset is active low. It includes an internal pull-up resistor. XRES is active during sleep and hibernate modes.

- SRES – Software Reset

  A reset can be commanded under program control by setting a bit in the software reset register. This is done either directly by the program or indirectly by DMA access. The response to a SRES is the same as after an IPOR reset.

  Another register bit exists to disable this function.

- WRES – Watchdog Timer Reset

  The watchdog reset detects when the software program is no longer being executed correctly. To indicate to the watchdog timer that it is running correctly, the program must periodically reset the timer. If the timer is not reset before a user-specified amount of time, then a reset is generated.

  Note IPOR disables the watchdog function. The program must enable the watchdog function at an appropriate point in the code by setting a register bit. When this bit is set, it cannot be cleared again except by an IPOR power-on reset event.

6.4 I/O System and Routing

PSoC I/Os are extremely flexible. Every GPIO has analog and digital I/O capability. All I/Os have a large number of drive modes, which are set at POR. PSoC also provides up to four individual I/O voltage domains through the VDDIO pins.

There are two types of I/O pins on every device; those with USB provide a third type. Both GPIO and Special I/O (SIO) provide similar digital functionality. The primary differences are their analog capability and drive strength. Devices that include USB also provide two USBIO pins that support specific USB functionality as well as limited GPIO capability.

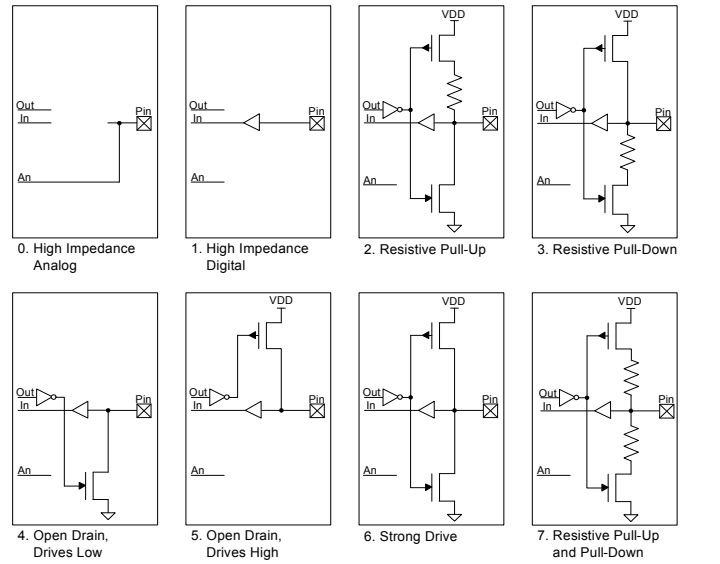
All I/O pins are available for use as digital inputs and outputs for both the CPU and digital peripherals. In addition, all I/O pins can generate an interrupt. The flexible and advanced capabilities of the PSoC I/O, combined with any signal to any pin routability, greatly simplify circuit design and board layout. All GPIO pins can be used for analog input, CapSense, and LCD segment drive, while SIO pins are used for voltages in excess of VDDA and for programmable output voltages.

- Features supported by both GPIO and SIO:
  - User programmable port reset state
  - Separate I/O supplies and voltages for up to four groups of I/O
  - Digital peripherals use DSI to connect the pins

6.4.1 Drive Modes

Each GPIO and SIO pin is individually configurable into one of the eight drive modes listed in Table 6-6. Three configuration bits are used for each pin (DM[2:0]) and set in the PRTxDM[2:0] registers. Figure 6-12 depicts a simplified pin view based on each of the eight drive modes. Table 6-6 shows the I/O pin's drive state based on the port data register value or digital array signal if bypass mode is selected. Note that the actual I/O pin voltage is determined by a combination of the selected drive mode and the load at the pin. For example, if a GPIO pin is configured for resistive pull-up mode and driven high while the pin is floating, the voltage measured at the pin is a high logic state. If the same GPIO pin is externally tied to ground then the voltage unmeasured at the pin is a low logic state.

Figure 6-12. Drive Mode



The 'Out' connection is driven from either the Digital System (when the Digital Output terminal is connected) or the Data Register (when HW connection is disabled).
The 'In' connection drives the Pin State register, and the Digital System if the Digital Input terminal is enabled and connected.
The 'An' connection connects to the Analog System.

Table 6-6. Drive Modes

Diagram	Drive Mode	PRTxDM2	PRTxDM1	PRTxDM0	PRTxDR = 1	PRTxDR = 0
0	High impedence analog	0	0	0	High Z	High Z
1	High Impedance digital	0	0	1	High Z	High Z
2	Resistive pull-up[12]	0	1	0	Res High (5K)	Strong Low
3	Resistive pull-down[12]	0	1	1	Strong High	Res Low (5K)
4	Open drain, drives low	1	0	0	High Z	Strong Low
5	Open drain, drive high	1	0	1	Strong High	High Z
6	Strong drive	1	1	0	Strong High	Strong Low
7	Resistive pull-up and pull-down[12]	1	1	1	Res High (5K)	Res Low (5K)

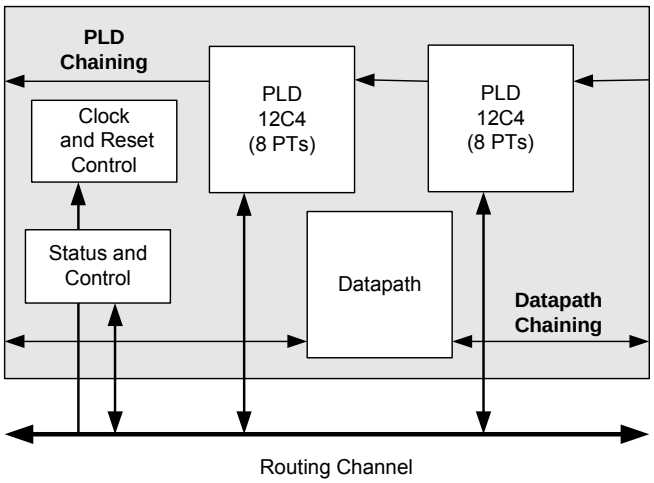
Note
12. Resistive pull-up and pull-down are not available with SIO in regulated output mode.

7.2 Universal Digital Block

The Universal Digital Block (UDB) represents an evolutionary step to the next generation of PSoC embedded digital peripheral functionality. The architecture in first generation PSoC digital blocks provides coarse programmability in which a few fixed functions with a small number of options are available. The new UDB architecture is the optimal balance between configuration granularity and efficient implementation. A cornerstone of this approach is to provide the ability to customize the devices digital operation to match application requirements.

To achieve this, UDBs consist of a combination of uncommitted logic (PLD), structured logic (Datapath), and a flexible routing scheme to provide interconnect between these elements, I/O connections, and other peripherals. UDB functionality ranges from simple self contained functions that are implemented in one UDB, or even a portion of a UDB (unused resources are available for other functions), to more complex functions that require multiple UDBs. Examples of basic functions are timers, counters, CRC generators, PWMs, dead band generators, and communications functions, such as UARTs, SPI, and I^2C. Also, the PLD blocks and connectivity provide full featured general purpose programmable logic within the limits of the available resources.

Figure 7-2. UDB Block Diagram



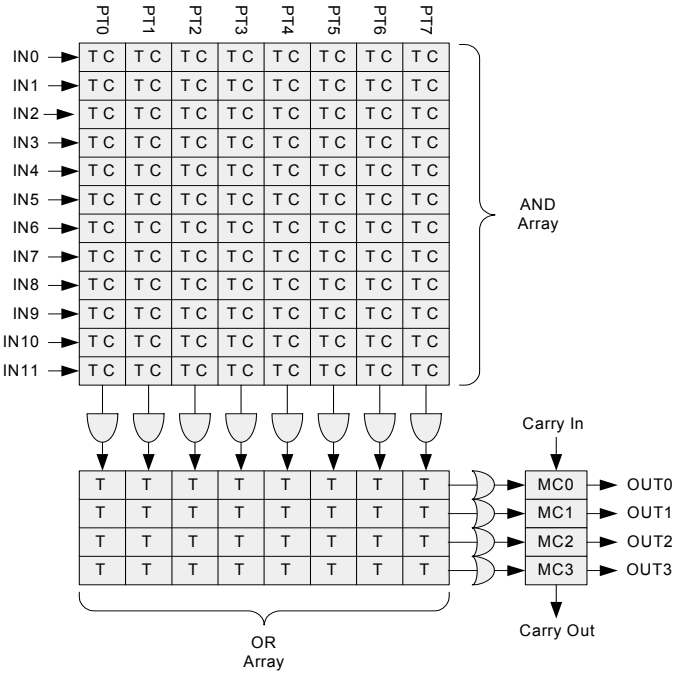
The main component blocks of the UDB are:

- PLD blocks – There are two small PLDs per UDB. These blocks take inputs from the routing array and form registered or combinational sum-of-products logic. PLDs are used to implement state machines, state bits, and combinational logic equations. PLD configuration is automatically generated from graphical primitives.
- Datapath Module – This 8-bit wide datapath contains structured logic to implement a dynamically configurable ALU, a variety of compare configurations and condition generation. This block also contains input/output FIFOs, which are the primary parallel data interface between the CPU/DMA system and the UDB.
- Status and Control Module – The primary role of this block is to provide a way for CPU firmware to interact and synchronize with UDB operation.
- Clock and Reset Module – This block provides the UDB clocks and reset selection and control.

7.2.1 PLD Module

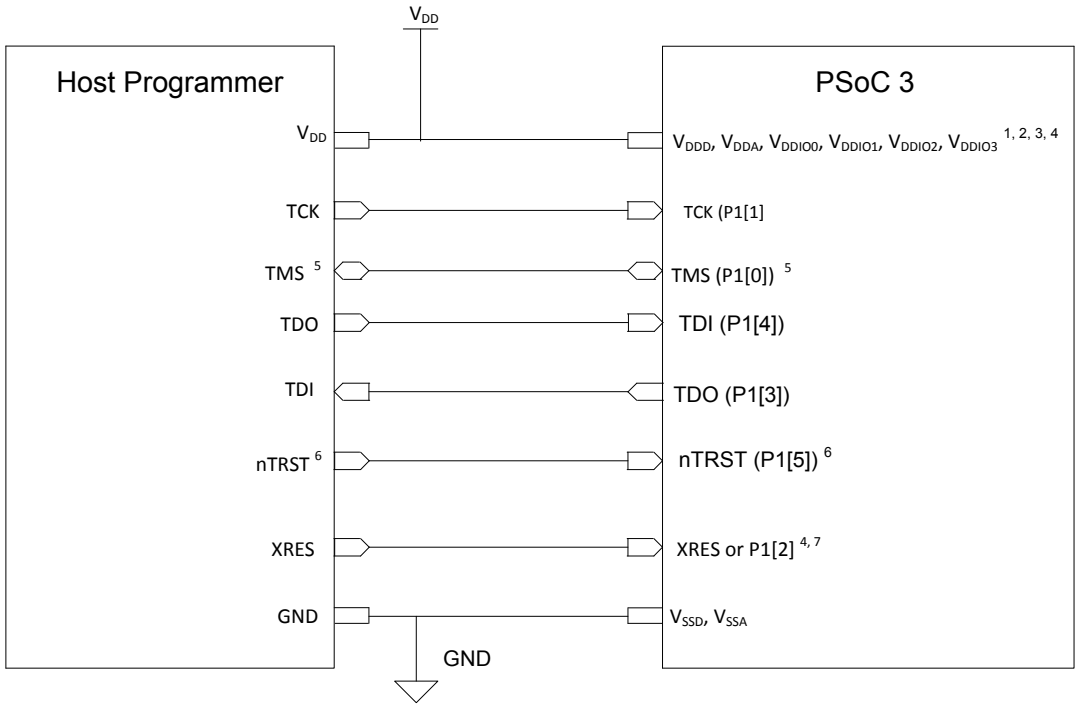
The primary purpose of the PLD blocks is to implement logic expressions, state machines, sequencers, lookup tables, and decoders. In the simplest use model, consider the PLD blocks as a standalone resource onto which general purpose RTL is synthesized and mapped. The more common and efficient use model is to create digital functions from a combination of PLD and datapath blocks, where the PLD implements only the random logic and state portion of the function while the datapath (ALU) implements the more structured elements.

Figure 7-3. PLD 12C4 Structure



One 12C4 PLD block is shown in Figure 7-3. This PLD has 12 inputs, which feed across eight product terms. Each product term (AND function) can be from 1 to 12 inputs wide, and in a given product term, the true (T) or complement (C) of each input can be selected. The product terms are summed (OR function) to create the PLD outputs. A sum can be from 1 to 8 product terms wide. The 'C' in 12C4 indicates that the width of the OR gate (in this case 8) is constant across all outputs (rather than variable as in a 22V10 device). This PLA like structure gives maximum flexibility and insures that all inputs and outputs are permutable for ease of allocation by the software tools. There are two 12C4 PLDs in each UDB.

Figure 9-1. JTAG Interface Connections between PSoC 3 and Programmer



[1] The voltage levels of Host Programmer and the PSoC 3 voltage domains involved in Programming should be same. The Port 1 JTAG pins, XRES pin (XRES_N or P1[2]) are powered by V_{DDIO1}. So, V_{DDIO1} of PSoC 3 should be at same voltage level as host V_{DD}. Rest of PSoC 3 voltage domains (V_{DDD}, V_{DDA}, V_{DDIO0}, V_{DDIO2}, V_{DDIO3}) need not be at the same voltage level as host Programmer.

[2] Vdda must be greater than or equal to all other power supplies (Vddd, Vddio's) in PSoC 3.

[3] For Power cycle mode Programming, XRES pin is not required. But the Host programmer must have the capability to toggle power (Vddd, Vdda, All Vddio's) to PSoC 3. This may typically require external interface circuitry to toggle power which will depend on the programming setup. The power supplies can be brought up in any sequence, however, once stable, VDDA must be greater than or equal to all other supplies.

[4] For JTAG Programming, Device reset can also be done without connecting to the XRES pin or Power cycle mode by using the TMS,TCK,TDI, TDO pins of PSoC 3, and writing to a specific register. But this requires that the DPS setting in NVL is not equal to "Debug Ports Disabled".

[5] By default, PSoC 3 is configured for 4-wire JTAG mode unless user changes the DPS setting. So the TMS pin is unidirectional. But if the DPS setting is changed to non-JTAG mode, the TMS pin in JTAG is bi-directional as the SWD Protocol has to be used for acquiring the PSoC 3 device initially. After switching from SWD to JTAG mode, the TMS pin will be uni-directional. In such a case, unidirectional buffer should not be used on TMS line.

[6] nTRST JTAG pin (P1[5]) cannot be used to reset the JTAG TAP controlller during first time programming of PSoC 3 as the default setting is 4-wire JTAG (nTRST disabled). Use the TMS, TCK pins to do a reset of JTAG TAP controller.

[7] If XRES pin is used by host, P1[2] will be configured as XRES by default only for 48-pin devices (without dedicated XRES pin). For devices with dedicated XRES pin, P1[2] is GPIO pin by default. So use P1[2] as Reset pin only for 48-pin devices, but use dedicated XRES pin for rest of devices.

Figure 11-1. Active Mode Current vs F_{CPU}, V_{DD} = 3.3 V, Temperature = 25 °C

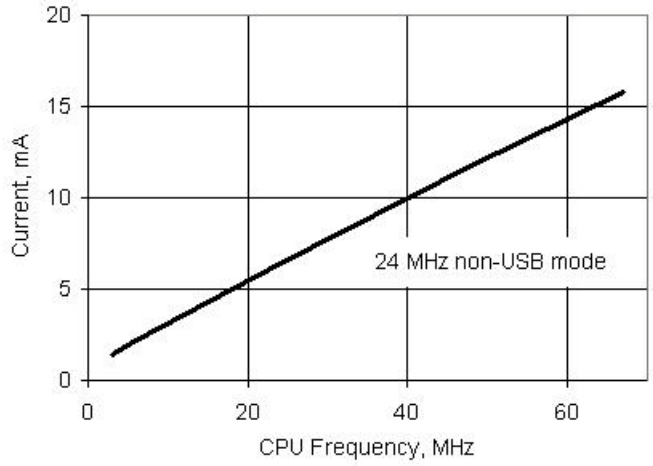


Figure 11-2. Active Mode Current vs Temperature and F_{CPU}, V_{DD} = 3.3 V

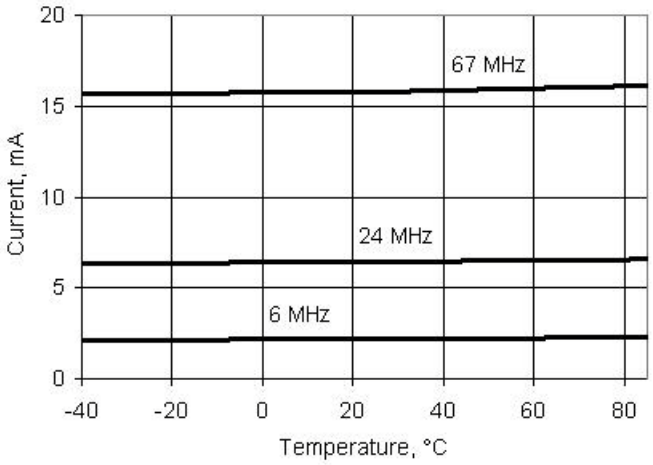
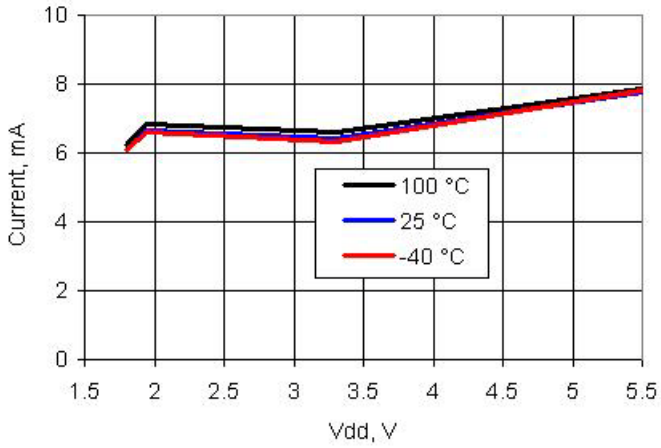


Figure 11-3. Active Mode Current vs V_{DD} and Temperature, F_{CPU} = 24 MHz



Notes
25. If V_{CCD} and V_{CCA} are externally regulated, the voltage difference between V_{CCD} and V_{CCA} must be less than 50 mV.
26. Sleep timer generates periodic interrupts to wake up the CPU. This specification applies only to those times that the CPU is off.
27. Externally regulated mode.
28. Based on device characterization (not production tested).
29. Based on device characterization (not production tested). USBIO pins tied to ground (V_{SSD}).

11.4 Inputs and Outputs

Specifications are valid for –40 °C ≤ T_A ≤ 85 °C and T_J ≤ 100 °C, except where noted. Specifications are valid for 1.71 V to 5.5 V, except where noted. Unless otherwise specified, all charts and graphs show typical values.

When the power supplies ramp up, there are low-impedance connections between each GPIO pin and its V_{DDIO} supply. This causes the pin voltages to track V_{DDIO} until both V_{DDIO} and V_{DDA} reach the IPOR voltage, which can be as high as 1.45 V. At that point, the low-impedance connections no longer exist and the pins change to their normal NVL settings.

11.4.1 GPIO

Table 11-9. GPIO DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input voltage high threshold	CMOS Input, PRT[×]CTL = 0	0.7 × V_{DDIO}	–	–	V
V_{IL}	Input voltage low threshold	CMOS Input, PRT[×]CTL = 0	–	–	0.3 × V_{DDIO}	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} < 2.7 V	0.7 × V_{DDIO}	–	–	V
V_{IH}	Input voltage high threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} ≥ 2.7V	2.0	–	–	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} < 2.7 V	–	–	0.3 × V_{DDIO}	V
V_{IL}	Input voltage low threshold	LVTTL Input, PRT[×]CTL = 1, V_{DDIO} ≥ 2.7V	–	–	0.8	V
V_{OH}	Output voltage high	I_{OH} = 4 mA at 3.3 V_{DDIO}	V_{DDIO} – 0.6	–	–	V
		I_{OH} = 1 mA at 1.8 V_{DDIO}	V_{DDIO} – 0.5	–	–	V
V_{OL}	Output voltage low	I_{OL} = 8 mA at 3.3 V_{DDIO}	–	–	0.6	V
		I_{OL} = 4 mA at 1.8 V_{DDIO}	–	–	0.6	V
		I_{OL} = 3 mA at 3.3 V_{DDIO}	–	–	0.4	V
Rpullup	Pull-up resistor		3.5	5.6	8.5	kΩ
Rpulldown	Pull-down resistor		3.5	5.6	8.5	kΩ
I_{IL}	Input leakage current (absolute value)[36]]	25 °C, V_{DDIO} = 3.0 V	–	–	2	nA
C_{IN}	Input capacitance[36]	GPIOs not shared with opamp outputs, MHz ECO or kHzECO	–	4	7	pF
		GPIOs shared with MHz ECO or kHzECO[37]	–	5	7	pF
		GPIOs shared with opamp outputs	–	–	18	pF
V_H	Input voltage hysteresis (Schmitt-Trigger)[36]		–	40	–	mV
Idiode	Current through protection diode to V_{DDIO} and V_{SSIO}		–	–	100	µA
Rglobal	Resistance pin to analog global bus	25 °C, V_{DDIO} = 3.0 V	–	320	–	Ω
Rmux	Resistance pin to analog mux bus	25 °C, V_{DDIO} = 3.0 V	–	220	–	Ω

Notes
36. Based on device characterization (Not production tested).
37. For information on designing with PSoC oscillators, refer to the application note, AN54439 - PSoC® 3 and PSoC 5 External Oscillator.

Table 11-26. IDAC DC Specifications *(continued)*

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	Operating current, code = 0	Low speed mode, source mode, range = 31.875 µA	–	44	100	µA
		Low speed mode, source mode, range = 255 µA,	–	33	100	µA
		Low speed mode, source mode, range = 2.04 mA	–	33	100	µA
		Low speed mode, sink mode, range = 31.875 µA	–	36	100	µA
		Low speed mode, sink mode, range = 255 µA	–	33	100	µA
		Low speed mode, sink mode, range = 2.04 mA	–	33	100	µA
		High speed mode, source mode, range = 31.875 µA	–	310	500	µA
		High speed mode, source mode, range = 255 µA	–	305	500	µA
		High speed mode, source mode, range = 2.04 mA	–	305	500	µA
		High speed mode, sink mode, range = 31.875 µA	–	310	500	µA
		High speed mode, sink mode, range = 255 µA	–	300	500	µA
		High speed mode, sink mode, range = 2.04 mA	–	300	500	µA

Figure 11-26. IDAC INL vs Input Code, Range = 255 µA, Source Mode

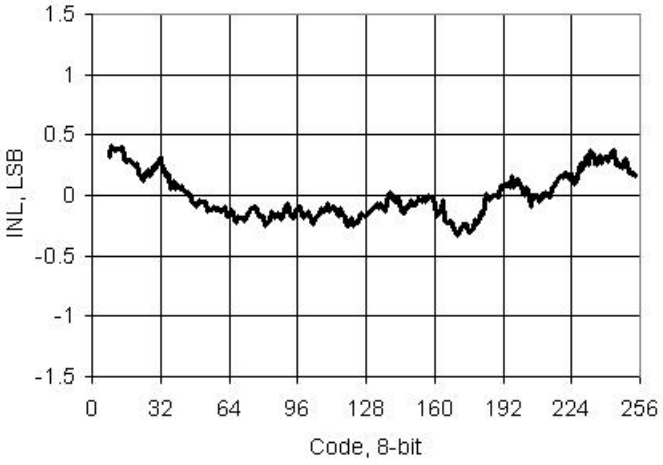


Figure 11-27. IDAC INL vs Input Code, Range = 255 µA, Sink Mode

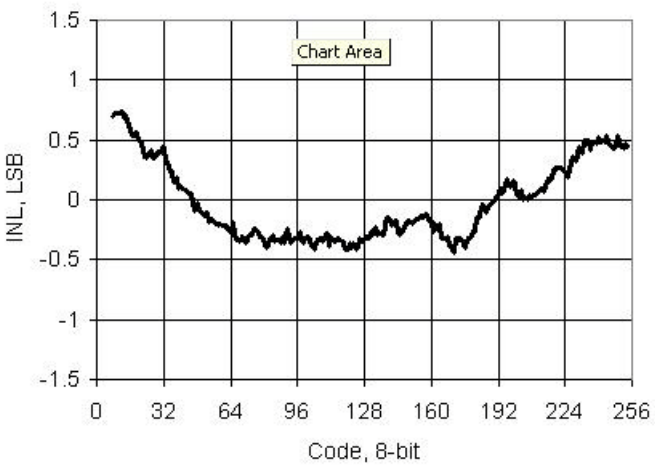


Figure 11-32. IDAC Full Scale Error vs Temperature, Range = 255 µA, Source Mode

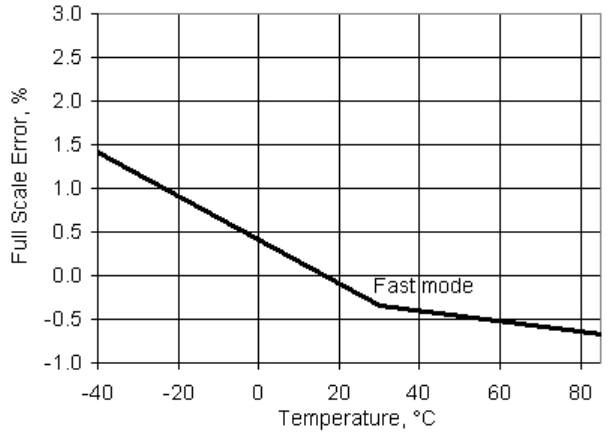


Figure 11-33. IDAC Full Scale Error vs Temperature, Range = 255 µA, Sink Mode

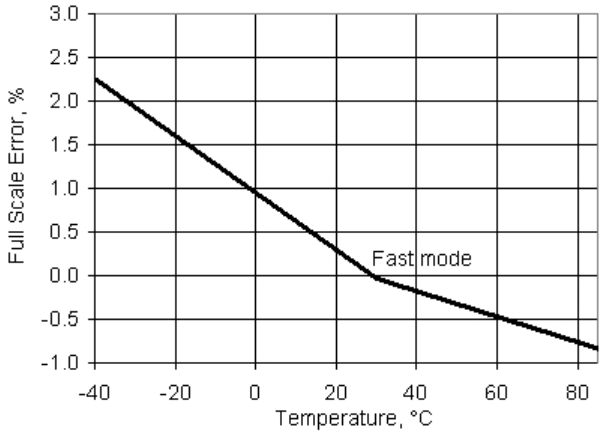


Figure 11-34. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Source Mode

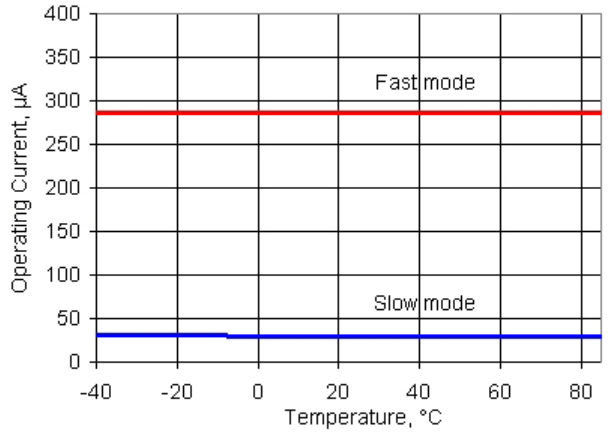


Figure 11-35. IDAC Operating Current vs Temperature, Range = 255 µA, Code = 0, Sink Mode

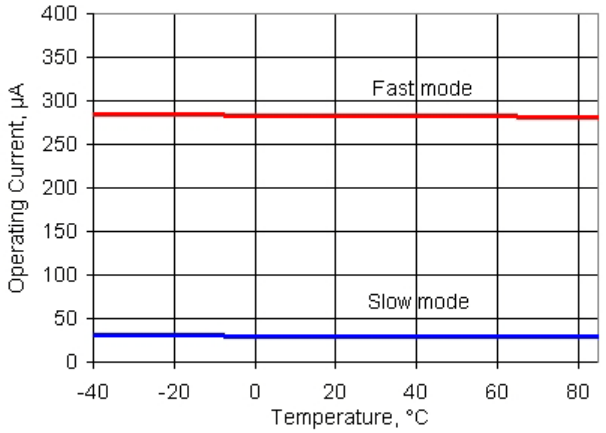


Figure 11-42. VDAC INL vs Temperature, 1 V Mode

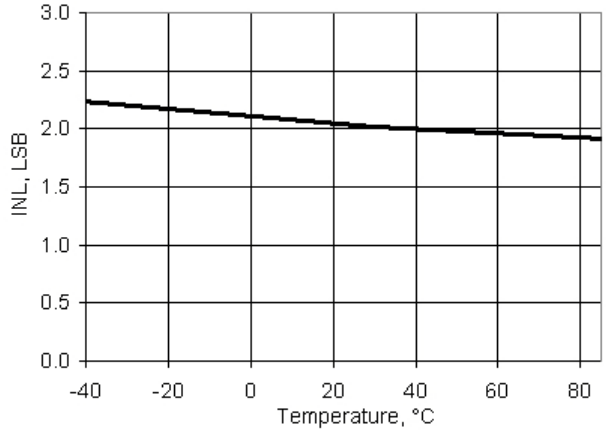


Figure 11-43. VDAC DNL vs Temperature, 1 V Mode

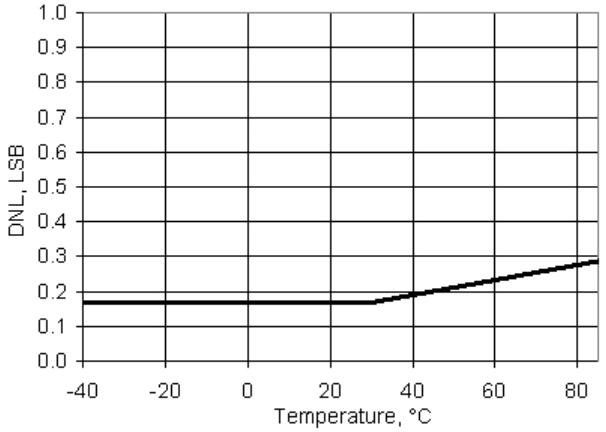


Figure 11-44. VDAC Full Scale Error vs Temperature, 1 V Mode

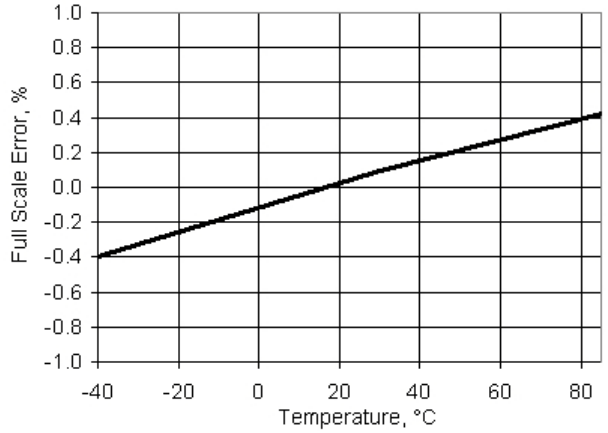


Figure 11-45. VDAC Full Scale Error vs Temperature, 4 V Mode

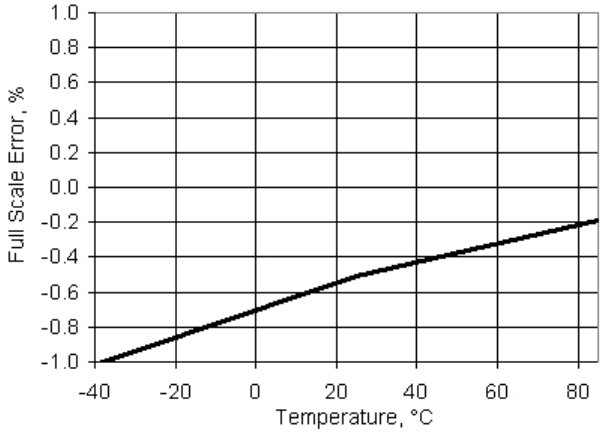


Figure 11-46. VDAC Operating Current vs Temperature, 1V Mode, Low speed mode

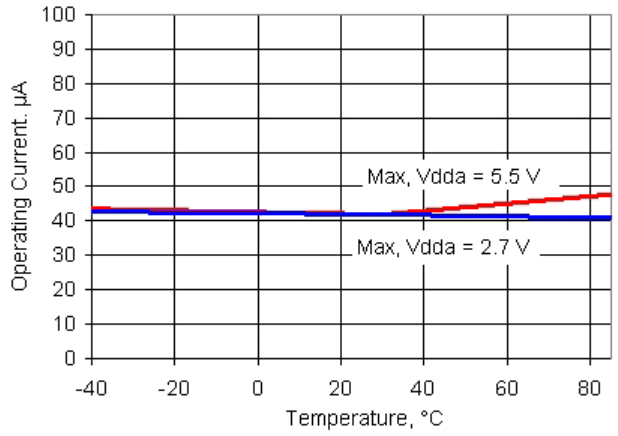
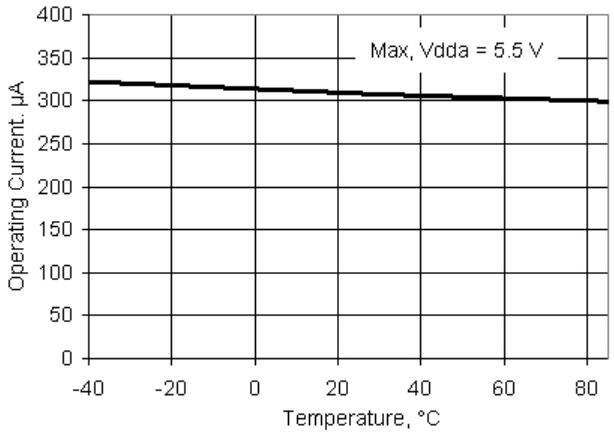


Figure 11-47. VDAC Operating Current vs Temperature, 1 V Mode, High speed mode



11.7.5 External Memory Interface

Figure 11-53. Asynchronous Write and Read Cycle Timing, No Wait States

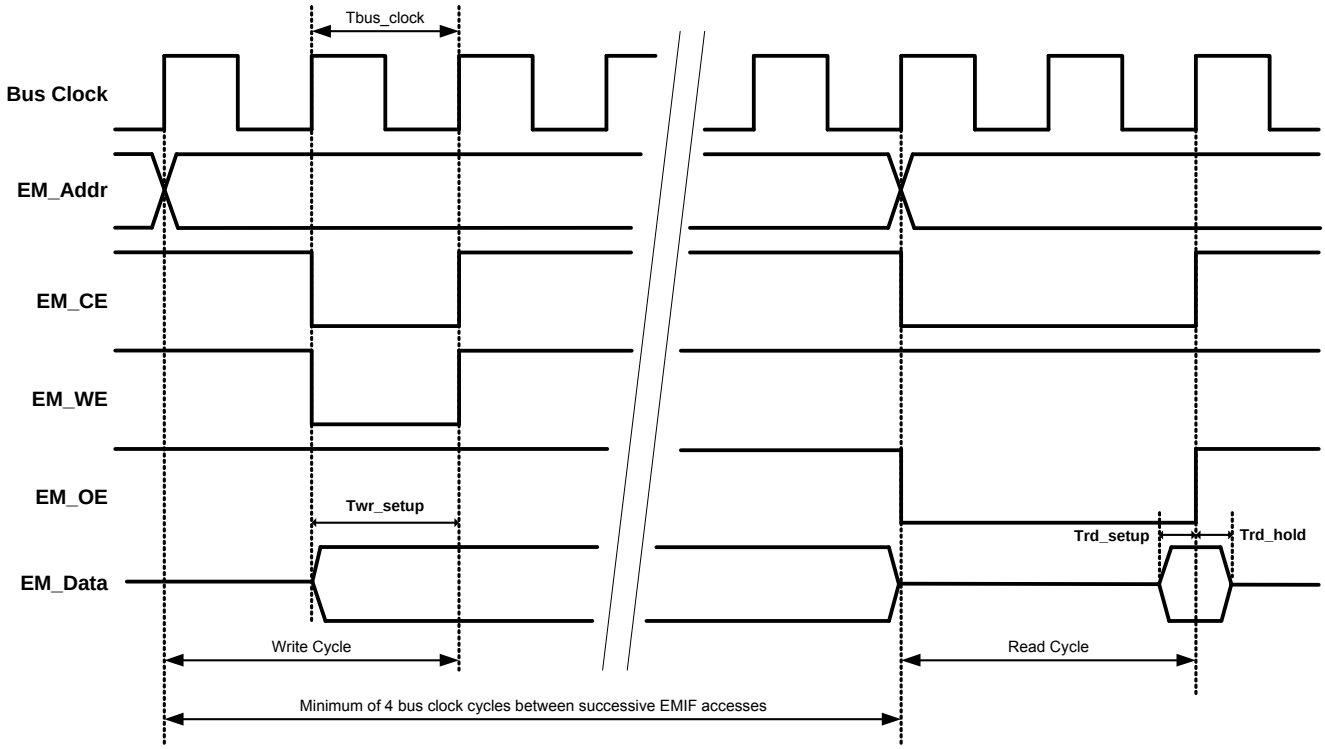


Table 11-53. Asynchronous Write and Read Timing Specifications[56]

Parameter	Description	Conditions	Min	Typ	Max	Units
Fbus_clock	Bus clock frequency[57]		–	–	33	MHz
Tbus_clock	Bus clock period[58]		30.3	–	–	ns
Twr_Setup	Time from EM_data valid to rising edge of EM_WE and EM_CE		Tbus_clock – 10	–	–	ns
Trd_setup	Time that EM_data must be valid before rising edge of EM_OE		5	–	–	ns
Trd_hold	Time that EM_data must be valid after rising edge of EM_OE		5	–	–	ns

Notes
56. Based on device characterization (Not production tested).
57. EMIF signal timings are limited by GPIO frequency limitations. See "GPIO" section on page 76.
58. EMIF output signals are generally synchronized to bus clock, so EMIF signal timings are dependent on bus clock frequency.

11.9.4 kHz External Crystal Oscillator

Table 11-71. kHzECO DC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{CC}	Operating current	Low-power mode; CL = 6 pF	–	0.25	1.0	µA
DL	Drive level		–	–	1	µW

Table 11-72. kHzECO AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
F	Frequency		–	32.768	–	kHz
T_{ON}	Startup time	High power mode	–	1	–	s

11.9.5 External Clock Reference

Table 11-73. External Clock Reference AC Specifications[72]

Parameter	Description	Conditions	Min	Typ	Max	Units
	External frequency range		0	–	33	MHz
	Input duty cycle range	Measured at $V_{DDIO}/2$	30	50	70	%
	Input edge rate	V_{IL} to V_{IH}	0.5	–	–	V/ns

11.9.6 Phase–Locked Loop

Table 11-74. PLL DC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
I_{DD}	PLL operating current	In = 3 MHz, Out = 24 MHz	–	200	–	µA

Table 11-75. PLL AC Specifications

Parameter	Description	Conditions	Min	Typ	Max	Units
Fpllin	PLL input frequency[73]		1	–	48	MHz
	PLL intermediate frequency[74]	Output of prescaler	1	–	3	MHz
Fpllout	PLL output frequency[73]		24	–	50	MHz
	Lock time at startup		–	–	250	µs
Jperiod-rms	Jitter (rms)[72]		–	–	250	ps

Notes
72. Based on device characterization (Not production tested).
73. This specification is guaranteed by testing the PLL across the specified range using the IMO as the source for the PLL.
74. PLL input divider, Q, must be set so that the input frequency is divided down to the intermediate frequency range. Value for Q ranges from 1 to 16.

12. Ordering Information

In addition to the features listed in Table 12-1, every CY8C32 device includes: a precision on-chip voltage reference, precision oscillators, flash, ECC, DMA, a fixed function I²C, 4 KB trace RAM, JTAG/SWD programming and debug, external memory interface, and more. In addition to these features, the flexible UDBs and analog subsection support a wide range of peripherals. To assist you in selecting the ideal part, PSoC Creator makes a part recommendation after you choose the components required by your application. All CY8C32 derivatives incorporate device and flash security in user-selectable security levels; see the TRM for details.

Table 12-1. CY8C32 Family with Single Cycle 8051

Part Number	MCU Core				Analog								Digital				I/O[76]				Package	JTAG ID[77]
	CPU Speed (MHz)	Flash (KB)	SRAM (KB)	EEPROM (KB)	LCD Segment Drive	ADC	DAC	Comparator	SC/CT Analog Blocks	Opamps	DFB	CapSense	UDBs[75]	16-bit Timer/PWM	FS USB	CAN 2.0b	Total I/O	GPIO	SIO	USBIO		
16 KB Flash																						
CY8C3244AXI-153	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	70	62	8	0	100-pin TQFP	0×1E099069
CY8C3244LTI-130	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	46	38	8	0	68-pin QFN	0×1E082069
CY8C3244LTI-123	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	29	25	4	0	48-pin QFN	0×1E07B069
CY8C3244PVI-133	50	16	2	0.5	✔	12-bit Del-Sig	1	2	0	0	–	✔	16	4	–	–	29	25	4	0	48-pin SSOP	0×1E085069
32 KB Flash																						
CY8C3245AXI-158	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	70	62	8	0	100-pin TQFP	0×1E09E069
CY8C3245LTI-163	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	46	38	8	0	68-pin QFN	0×1E0A3069
CY8C3245LTI-139	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	29	25	4	0	48-pin QFN	0×1E08B069
CY8C3245PVI-134	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	29	25	4	0	48-pin SSOP	0×1E086069
CY8C3245AXI-166	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	72	62	8	2	100-pin TQFP	0×1E0A6069
CY8C3245LTI-144	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	31	25	4	2	48-pin QFN	0×1E090069
CY8C3245PVI-150	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	✔	–	31	25	4	2	48-pin SSOP	0×1E096069
CY8C3245FNI-212	50	32	4	1	✔	12-bit Del-Sig	1	2	0	0	–	✔	20	4	–	–	46	38	8	0	72-pin WLCSP	0x1E0D4069
64 KB Flash																						
CY8C3246LTI-149	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	46	38	8	0	68-pin QFN	0×1E095069
CY8C3246PVI-147	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	31	25	4	2	48-pin SSOP	0×1E093069
CY8C3246AXI-131	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	70	62	8	0	100-pin TQFP	0×1E083069
CY8C3246LTI-162	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	29	25	4	0	48-pin QFN	0×1E0A2069
CY8C3246PVI-122	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	–	–	29	25	4	0	48-pin SSOP	0×1E07A069
CY8C3246AXI-138	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	72	62	8	2	100-pin TQFP	0×1E08A069
CY8C3246LTI-128	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	48	38	8	2	68-pin QFN	0×1E080069
CY8C3246LTI-125	50	64	8	2	✔	12-bit Del-Sig	1	2	0	0	–	✔	24	4	✔	–	31	25	4	2	48-pin QFN	0×1E07D069
CY8C3246FNI-213	50	64	8	2	✔	12-bit Del-Sig	1	2	–	–	–	✔	24	4	–	–	46	38	8	–	72-pin WLCSP	0x1E0D5069

Notes

75. UDBs support a wide variety of functionality including SPI, LIN, UART, timer, counter, PWM, PRS, and others. Individual functions may use a fraction of a UDB or multiple UDBs. Multiple functions can share a single UDB. See the Example Peripherals on page 45 for more information on how UDBs can be used.
76. The I/O Count includes all types of digital I/O: GPIO, SIO, and the two USB I/O. See the I/O System and Routing on page 37 for details on the functionality of each of these types of I/O.
77. The JTAG ID has three major fields. The most significant nibble (left digit) is the version, followed by a 2 byte part number and a 3 nibble manufacturer ID.

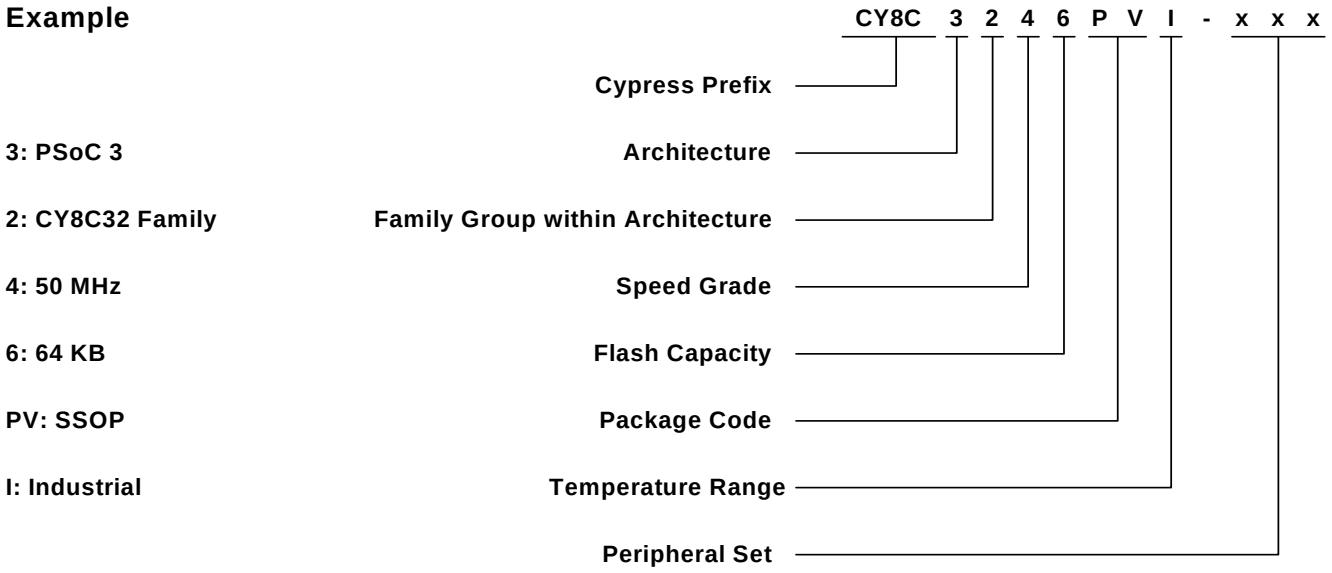
12.1 Part Numbering Conventions

PSoC 3 devices follow the part numbering convention described here. All fields are single character alphanumeric (0, 1, 2, …, 9, A, B, …, Z) unless stated otherwise.

CY8Cabcdefg-xxx

- a: Architecture
  - 3: PSoC 3
  - 5: PSoC 5
- b: Family group within architecture
  - 2: CY8C32 family
  - 4: CY8C34 family
  - 6: CY8C36 family
  - 8: CY8C38 family
- c: Speed grade
  - 4: 50 MHz
  - 6: 67 MHz
- d: Flash capacity
  - 4: 16 KB
  - 5: 32 KB
  - 6: 64 KB
- ef: Package code
  - Two character alphanumeric
  - AX: TQFP
  - LT: QFN
  - PV: SSOP
  - FN: CSP
- g: Temperature range
  - C: commercial
  - I: industrial
  - A: automotive
- xxx: Peripheral set
  - Three character numeric
  - No meaning is associated with these three characters.

Example



Tape and reel versions of these devices are available and are marked with a "T" at the end of the part number.

All devices in the PSoC 3 CY8C32 family comply to RoHS-6 specifications, demonstrating the commitment by Cypress to lead-free products. Lead (Pb) is an alloying element in solders that has resulted in environmental concerns due to potential toxicity. Cypress uses nickel-palladium-gold (NiPdAu) technology for the majority of leadframe-based packages.

A high level review of the Cypress Pb-free position is available on our website. Specific package information is also available. Package Material Declaration Datasheets (PMDDs) identify all substances contained within Cypress packages. PMDDs also confirm the absence of many banned substances. The information in the PMDDs will help Cypress customers plan for recycling or other “end of life” requirements.

14. Acronyms

Table 14-1. Acronyms Used in this Document

Acronym	Description
abus	analog local bus
ADC	analog-to-digital converter
AG	analog global
AHB	AMBA (advanced microcontroller bus architecture) high-performance bus, an ARM data transfer bus
ALU	arithmetic logic unit
AMUXBUS	analog multiplexer bus
API	application programming interface
APSR	application program status register
ARM®	advanced RISC machine, a CPU architecture
ATM	automatic thump mode
BW	bandwidth
CAN	Controller Area Network, a communications protocol
CMRR	common-mode rejection ratio
CPU	central processing unit
CRC	cyclic redundancy check, an error-checking protocol
DAC	digital-to-analog converter, see also IDAC, VDAC
DFB	digital filter block
DIO	digital input/output, GPIO with only digital capabilities, no analog. See GPIO.
DMA	direct memory access, see also TD
DNL	differential nonlinearity, see also INL
DNU	do not use
DR	port write data registers
DSI	digital system interconnect
DWT	data watchpoint and trace
ECC	error correcting code
ECO	external crystal oscillator
EEPROM	electrically erasable programmable read-only memory
EMI	electromagnetic interference
EMIF	external memory interface
EOC	end of conversion
EOF	end of frame
EPSR	execution program status register
ESD	electrostatic discharge
ETM	embedded trace macrocell

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
FIR	finite impulse response, see also IIR
FPB	flash patch and breakpoint
FS	full-speed
GPIO	general-purpose input/output, applies to a PSoC pin
HVI	high-voltage interrupt, see also LVI, LVD
IC	integrated circuit
IDAC	current DAC, see also DAC, VDAC
IDE	integrated development environment
I^2C, or IIC	Inter-Integrated Circuit, a communications protocol
IIR	infinite impulse response, see also FIR
ILO	internal low-speed oscillator, see also IMO
IMO	internal main oscillator, see also ILO
INL	integral nonlinearity, see also DNL
I/O	input/output, see also GPIO, DIO, SIO, USBIO
IPOR	initial power-on reset
IPSR	interrupt program status register
IRQ	interrupt request
ITM	instrumentation trace macrocell
LCD	liquid crystal display
LIN	Local Interconnect Network, a communications protocol.
LR	link register
LUT	lookup table
LVD	low-voltage detect, see also LVI
LVI	low-voltage interrupt, see also HVI
LVTTL	low-voltage transistor-transistor logic
MAC	multiply-accumulate
MCU	microcontroller unit
MISO	master-in slave-out
NC	no connect
NMI	nonmaskable interrupt
NRZ	non-return-to-zero
NVIC	nested vectored interrupt controller
NVL	nonvolatile latch, see also WOL
opamp	operational amplifier
PAL	programmable array logic, see also PLD
PC	program counter
PCB	printed circuit board
PGA	programmable gain amplifier

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
PHUB	peripheral hub
PHY	physical layer
PICU	port interrupt control unit
PLA	programmable logic array
PLD	programmable logic device, see also PAL
PLL	phase-locked loop
PMDD	package material declaration datasheet
POR	power-on reset
PRES	precise low-voltage reset
PRS	pseudo random sequence
PS	port read data register
PSoC®	Programmable System-on-Chip™
PSRR	power supply rejection ratio
PWM	pulse-width modulator
RAM	random-access memory
RISC	reduced-instruction-set computing
RMS	root-mean-square
RTC	real-time clock
RTL	register transfer language
RTR	remote transmission request
RX	receive
SAR	successive approximation register
SC/CT	switched capacitor/continuous time
SCL	I^2C serial clock
SDA	I^2C serial data
S/H	sample and hold
SINAD	signal to noise and distortion ratio
SIO	special input/output, GPIO with advanced features. See GPIO.
SOC	start of conversion

Table 14-1. Acronyms Used in this Document *(continued)*

Acronym	Description
SOF	start of frame
SPI	Serial Peripheral Interface, a communications protocol
SR	slew rate
SRAM	static random access memory
SRES	software reset
SWD	serial wire debug, a test protocol
SWV	single-wire viewer
TD	transaction descriptor, see also DMA
THD	total harmonic distortion
TIA	transimpedance amplifier
TRM	technical reference manual
TTL	transistor-transistor logic
TX	transmit
UART	Universal Asynchronous Transmitter Receiver, a communications protocol
UDB	universal digital block
USB	Universal Serial Bus
USBIO	USB input/output, PSoC pins used to connect to a USB port
VDAC	voltage DAC, see also DAC, IDAC
WDT	watchdog timer
WOL	write once latch, see also NVL
WRES	watchdog timer reset
XRES	external reset I/O pin
XTAL	crystal

15. Reference Documents

PSoC® 3, PSoC® 5 Architecture TRM

PSoC® 3 Registers TRM

Description Title: PSoC® 3: CY8C32 Family Data Sheet Programmable System-on-Chip (PSoC®) *(continued)* Document Number: 001-56955				
Revision	**ECN**	**Submission Date**	**Orig. of Change**	**Description of Change**
*C	2903576	04/01/10	MKEA	Updated Vb pin in PCB Schematic. Updated Tstartup parameter in AC Specifications table. Added Load regulation and Line regulation parameters to Inductive Boost Regulator DC Specifications table. Updated I_{CC} parameter in LCD Direct Drive DC Specs table. In page 1, updated internal oscillator range under Prescision programmable clocking to start from 3 MHz. Updated I_{OUT} parameter in LCD Direct Drive DC Specs table. Updated Table 6-2 and Table 6-3. Added bullets on CapSense in page 1; added CapSense column in Section 12 Removed some references to footnote [1]. Changed INC_Rn cycles from 3 to 2 (Table 4-1). Added footnote in PLL AC Specification table. Added PLL intermediate frequency row with footnote in PLL AC Specs table. Added UDBs subsection under 11.6 Digital Peripherals. Updated Figure 2-6 (PCB Layout). Updated Pin Descriptions section and modified Figures 6-6, 6-8, 6-9. Updated LVD in Tables 6-2 and 6-3; modified Low-power modes bullet in page 1. Added note to Figures 2-5 and 6-2; Updated Figure 6-2 to add capacitors for V_{DDA} and V_{DDD} pins. Updated boost converter section (6.2.2). Updated Tstartup values in Table 11-3. Removed IPOR rows from Table 11-53. Updated 6.3.1.1, Power Voltage Level Monitors. Updated section 5.2 and Table 11-2 to correct suggestion of execution from flash. Updated IMO max frequency in Figure 6-1, Table 11-63, and Table 11-64. Updated V_{REF} specs in Table 11-19. Updated IDAC uncompensated gain error in Table 11-23. Updated Delay from Interrupt signal input to ISR code execution from ISR code in Table-71. Removed other line in table. Added sentence to last paragraph of section 6.1.1.3. Updated Tresp, high and low-power modes, in Table 11-22. Updated f_TCK values in Table 11-58 and f_SWDCK values in Table 11-59. Updated SNR condition in Table 11-18. Updated sleep wakeup time in Table 6-3 and Tsleep in Table 11-3. Added 1.71 V <= V_{DDD} < 3.3 V, SWD over USBIO pins value to Table 11-59. Removed mention of hibernate reset (HRES) from page 1 features, Table 6-3, Section 6.2.1.4, Section 6.3, and Section 6.3.1.1. Change PPOR/PRES to TBDs in Section 6.3.1.1, Section 6.4.1.6 (changed PPOR to reset), Table 11-3 (changed PPOR to PRES), Table 11-53 (changed title, values TBD), and Table 11-54 (changed PPOR_TR to PRES_TR). Added sentence saying that LVD circuits can generate a reset to Section 6.3.1.1. Changed I_{DD} values on page 1, page 5, and Table 11-2. Changed resume time value in Section 6.2.1.3. Changed ESD HBM value in Table 11-1. Changed sample rate row in Table 11-18. Removed V_{DDA} = 1.65 V rows and changed BWag value in Table 11-20. Changed Vioff values and changed CMRR value in Table 11-21. Changed INL max value in Table 11-25. Changed occurrences of “Block” to “Row” and deleted the “ECC not included” footnote in Table 11-41. Changed max response time value in Tables 11-54 and 11-56. Change the Startup time in Table 11-64. Added condition to intermediate frequency row in Table 11-70. Added row to Table 11-54. Added brown out note to Section 11.8.1.