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"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	20
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 9x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SSOP (0.209", 5.30mm Width)
Supplier Device Package	28-SSOP
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb202-e-ss

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TABLE 4-6: TIMER REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
TMR1	024C	Timer1 Register																0000
PR1	024E	Timer1 Period Register																FFFF
T1CON	0250	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	—	TSYNC	TCS	—	0000
TMR2	0252	Timer2 Register																0000
TMR3HLD	0254	Timer3 Holding Register (for 32-bit timer operations only)																0000
TMR3	0256	Timer3 Register																0000
PR2	0258	Timer2 Period Register																FFFF
PR3	025A	Timer3 Period Register																FFFF
T2CON	025C	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	T32	—	TCS	—	0000
T3CON	025E	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000
TMR4	0260	Timer4 Register																0000
TMR5HLD	0262	Timer5 Holding Register (for 32-bit operations only)																0000
TMR5	0264	Timer5 Register																0000
PR4	0266	Timer4 Period Register																FFFF
PR5	0268	Timer5 Period Register																FFFF
T4CON	026A	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	T45	—	TCS	—	0000
T5CON	026C	TON	—	TSIDL	—	—	—	TECS1	TECS0	—	TGATE	TCKPS1	TCKPS0	—	—	TCS	—	0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-9: I²C™ REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
I2C1RCV	02DA	—	—	—	—	—	—	—	—	I2C1 Receive Register								0000
I2C1TRN	02DC	—	—	—	—	—	—	—	—	I2C1 Transmit Register								00FF
I2C1BRG	02DE	—	—	—	—	I2C1 Baud Rate Generator Register												0000
I2C1CONL	02E0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C1CONH	02E2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C1STAT	02E4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C1ADD	02E6	—	—	—	—	—	—	I2C1 Address Register										0000
I2C1MSK	02E8	—	—	—	—	—	—	12C1 Address Mask Register										0000
I2C2RCV	02EA	—	—	—	—	—	—	—	—	I2C2 Receive Register								0000
I2C2TRN	02EC	—	—	—	—	—	—	—	—	I2C2 Transmit Register								00FF
I2C2BRG	02EE	—	—	—	—	I2C2 Baud Rate Generator Register												0000
I2C2CONL	02F0	I2CEN	—	I2CSIDL	SCLREL	STRICT	A10M	DISSLW	SMEN	GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN	1000
I2C2CONH	02F2	—	—	—	—	—	—	—	—	—	PCIE	SCIE	BOEN	SDAHT	SBCDE	AHEN	DHEN	0000
I2C2STAT	02F4	ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10	IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF	0000
I2C2ADD	02F6	—	—	—	—	—	—	I2C2 Address Register										0000
I2C2MSK	02F8	—	—	—	—	—	—	I2C2 Address Mask Register										0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

REGISTER 8-3: INTCON1: INTERRUPT CONTROL REGISTER 1

R/W-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
NSTDIS	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0
—	—	—	MATHERR	ADDRERR	STKERR	OSCFAIL	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **NSTDIS:** Interrupt Nesting Disable bit
1 = Interrupt nesting is disabled
0 = Interrupt nesting is enabled

bit 14-5 **Unimplemented:** Read as '0'

bit 4 **MATHERR:** Arithmetic Error Trap Status bit
1 = Overflow trap has occurred
0 = Overflow trap has not occurred

bit 3 **ADDRERR:** Address Error Trap Status bit
1 = Address error trap has occurred
0 = Address error trap has not occurred

bit 2 **STKERR:** Stack Error Trap Status bit
1 = Stack error trap has occurred
0 = Stack error trap has not occurred

bit 1 **OSCFAIL:** Oscillator Failure Trap Status bit
1 = Oscillator failure trap has occurred
0 = Oscillator failure trap has not occurred

bit 0 **Unimplemented:** Read as '0'

REGISTER 8-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	DMA4IF	PMPIF	—	—	OC6IF	OC5IF	IC6IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC5IF	IC4IF	IC3IF	DMA3IF	CRYROLLIF	CRYFREEIF	SPI2TXIF	SPI2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DMA4IF:** DMA Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **PMPIF:** Parallel Master Port Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OC6IF:** Output Compare Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **OC5IF:** Output Compare Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **IC6IF:** Input Capture Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **IC5IF:** Input Capture Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **IC4IF:** Input Capture Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **DMA3IF:** DMA Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CRYROLLIF:** Cryptographic Rollover Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CRYFREEIF:** Cryptographic Buffer Free Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 9-3: OSCTUN: FRC OSCILLATOR TUNE REGISTER

R/W-0	U-0	R/W-0	R/W-0	R-0	R/W-0	R-0	R/W-0
STEN	—	STSIDL	STSRC(1)	STLOCK	STLPOL	STOR	STORPOL
bit 15							bit 8

U-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
—	—	TUN5	TUN4	TUN3	TUN2	TUN1	TUN0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **STEN:** FRC Self-Tune Enable bit
1 = FRC self-tuning is enabled; TUNx bits are controlled by hardware
0 = FRC self-tuning is disabled; application may optionally control TUNx bits

bit 14 **Unimplemented:** Read as '0'

bit 13 **STSIDL:** FRC Self-Tune Stop in Idle bit
1 = Self-tuning stops during Idle mode
0 = Self-tuning continues during Idle mode

bit 12 **STSRC:** FRC Self-Tune Reference Clock Source bit(1)
1 = FRC is tuned to approximately match the USB host clock tolerance
0 = FRC is tuned to approximately match the 32.768 kHz SOSC tolerance

bit 11 **STLOCK:** FRC Self-Tune Lock Status bit
1 = FRC accuracy is currently within ±0.2% of the STSRC reference accuracy
0 = FRC accuracy may not be within ±0.2% of the STSRC reference accuracy

bit 10 **STLPOL:** FRC Self-Tune Lock Interrupt Polarity bit
1 = A self-tune lock interrupt is generated when STLOCK = 0
0 = A self-tune lock interrupt is generated when STLOCK = 1

bit 9 **STOR:** FRC Self-Tune Out of Range Status bit
1 = STSRC reference clock error is beyond the range of TUN<5:0>; no tuning is performed
0 = STSRC reference clock is within the tunable range; tuning is performed

bit 8 **STORPOL:** FRC Self-Tune Out of Range Interrupt Polarity bit
1 = A self-tune out of range interrupt is generated when STOR is = 0
0 = A self-tune out of range interrupt is generated when STOR is = 1

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **TUN<5:0>:** FRC Oscillator Tuning bits
011111 = Maximum frequency deviation
011110 =
•
•
•
000001 =
000000 = Center frequency, oscillator is running at factory calibrated frequency
111111 =
•
•
•
100001 =
100000 = Minimum frequency deviation

Note 1: Use of either clock recovery source has specific application requirements. For more information, see **Section 9.5 "FRC Self-Tuning"**.

10.1.2 HARDWARE-BASED POWER-SAVING MODE

The hardware-based VBAT mode does not require any action by the user during code development. Instead, it is a hardware design feature that allows the microcontroller to retain critical data (using the DSGPRx registers) and maintain the RTCC when VDD is removed from the application. This is accomplished by supplying a backup power source to a specific power pin. VBAT mode is described in more detail in **Section 10.5 "VBAT Mode"**.

10.1.3 LOW-VOLTAGE/RETENTION REGULATOR

PIC24FJ128GB204 family devices incorporate a second on-chip voltage regulator, designed to provide power to select microcontroller features at 1.2V nominal. This regulator allows features, such as data RAM and the WDT, to be maintained in power-saving modes, where they would otherwise be inactive, or maintain them at a lower power than would otherwise be the case.

The low-voltage/retention regulator is only available when Sleep mode is invoked. It is controlled by the LPCFG Configuration bit (CW1<10>) and in firmware by the RETEN bit (RCON<12>). LPCFG must be programmed (= 0) and the RETEN bit must be set (= 1) for the regulator to be enabled.

10.2 Idle Mode

Idle mode includes these features:

- The CPU will stop executing instructions.
- The WDT is automatically cleared.
- The system clock source remains active. By default, all peripheral modules continue to operate normally from the system clock source, but can also be selectively disabled (see **Section 10.8 "Selective Peripheral Module Control"**).
- If the WDT or FSCM is enabled, the LPRC will also remain active.

The device will wake from Idle mode on any of these events:

- Any interrupt that is individually enabled
- Any device Reset
- A WDT time-out

On wake-up from Idle, the clock is reapplied to the CPU and instruction execution begins immediately, starting with the instruction following the PWRSAV instruction or the first instruction in the Interrupt Service Routine (ISR).

10.3 Sleep Mode

Sleep mode includes these features:

- The system clock source is shut down. If an on-chip oscillator is used, it is turned off.
- The device current consumption will be reduced to a minimum provided that no I/O pin is sourcing current.
- The I/O pin directions and states are frozen.
- The Fail-Safe Clock Monitor does not operate during Sleep mode since the system clock source is disabled.
- The LPRC clock will continue to run in Sleep mode if the WDT or RTCC, with LPRC as the clock source, is enabled.
- The WDT, if enabled, is automatically cleared prior to entering Sleep mode.
- Some device features or peripherals may continue to operate in Sleep mode. This includes items, such as the Input Change Notification on the I/O ports or peripherals that use an external clock input. Any peripheral that requires the system clock source for its operation will be disabled in Sleep mode.

The device will wake-up from Sleep mode on any of these events:

- On any interrupt source that is individually enabled
- On any form of device Reset
- On a WDT time-out

On wake-up from Sleep, the processor will restart with the same clock source that was active when Sleep mode was entered.

10.3.1 LOW-VOLTAGE/RETENTION SLEEP MODE

Low-Voltage/Retention Sleep mode functions as Sleep mode with the same features and wake-up triggers. The difference is that the low-voltage/retention regulator allows core digital logic voltage (VCORE) to drop to 1.2V nominal. This permits an incremental reduction of power consumption over what would be required if VCORE was maintained at a 1.8V (minimum) level.

Low-Voltage Sleep mode requires a longer wake-up time than Sleep mode, due to the additional time required to bring VCORE back to 1.8V (known as TREG). In addition, the use of the low-voltage/retention regulator limits the amount of current that can be sourced to any active peripherals, such as the RTCC, etc.

13.0 TIMER2/3 AND TIMER4/5

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Timers"** (DS39704). The information in this data sheet supersedes the information in the FRM.

The Timer2/3 and Timer4/5 modules are 32-bit timers, which can also be configured as four independent, 16-bit timers with selectable operating modes.

As 32-bit timers, Timer2/3 and Timer4/5 can each operate in three modes:

- Two Independent 16-Bit Timers with all 16-Bit Operating modes (except Asynchronous Counter mode)
- Single 32-Bit Timer
- Single 32-Bit Synchronous Counter

They also support these features:

- Timer Gate Operation
- Selectable Prescaler Settings
- Timer Operation during Idle and Sleep modes
- Interrupt on a 32-Bit Period Register Match
- A/D Event Trigger (only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode)

Individually, all four of the 16-bit timers can function as synchronous timers or counters. They also offer the features listed above, except for the A/D Event Trigger. This trigger is implemented only on Timer2/3 in 32-bit mode and Timer3 in 16-bit mode. The operating modes and enabled features are determined by setting the appropriate bit(s) in the T2CON, T3CON, T4CON and T5CON registers. T2CON and T4CON are shown in generic form in Register 13-1; T3CON and T5CON are shown in Register 13-2.

For 32-bit timer/counter operation, Timer2 and Timer4 are the least significant word; Timer3 and Timer5 are the most significant word of the 32-bit timers.

Note: For 32-bit operation, T3CON and T5CON control bits are ignored. Only T2CON and T4CON control bits are used for setup and control. Timer2 and Timer4 clock and gate inputs are utilized for the 32-bit timer modules, but an interrupt is generated with the Timer3 or Timer5 interrupt flags.

To configure Timer2/3 or Timer4/5 for 32-bit operation:

1. Set the T32 or T45 bit (T2CON<3> or T4CON<3> = 1).
2. Select the prescaler ratio for Timer2 or Timer4 using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. If TCS is set to an external clock, RPINRx (TxCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.
4. Load the timer period value. PR3 (or PR5) will contain the most significant word (msw) of the value, while PR2 (or PR4) contains the least significant word (lsw).
5. If interrupts are required, set the Timer3/5 Interrupt Enable bit, T3IE or T5IE. Use the Timer3/5 Interrupt Priority bits, T3IP<2:0> or T5IP<2:0>, to set the interrupt priority. Note that while Timer2 or Timer4 controls the timer, the interrupt appears as a Timer3 or Timer5 interrupt.
6. Set the TON bit (= 1).

The timer value, at any point, is stored in the register pair, TMR<3:2> (or TMR<5:4>). TMR3 (TMR5) always contains the most significant word of the count, while TMR2 (TMR4) contains the least significant word.

To configure any of the timers for individual 16-bit operation:

1. Clear the T32 bit corresponding to that timer (T2CON<3> for Timer2 and Timer3 or T4CON<3> for Timer4 and Timer5).
2. Select the timer prescaler ratio using the TCKPS<1:0> bits.
3. Set the Clock and Gating modes using the TCS and TGATE bits. See **Section 11.4 "Peripheral Pin Select (PPS)"** for more information.
4. Load the timer period value into the PRx register.
5. If interrupts are required, set the Timerx Interrupt Enable bit, TxIE. Use the Timerx Interrupt Priority bits, TxIP<2:0>, to set the interrupt priority.
6. Set the TON (TxCON<15> = 1) bit.

REGISTER 13-2: TyCON: TIMER3 AND TIMER5 CONTROL REGISTER(1)

R/W-0	U-0	R/W-0	U-0	U-0	U-0	R/W-0	R/W-0
TON(2)	—	TSIDL(2)	—	—	—	TECS1(2,3)	TECS0(2,3)
bit 15							bit 8

U-0	R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	U-0
—	TGATE(2)	TCKPS1(2)	TCKPS0(2)	—	—	TCS(2,3)	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **TON:** Timery On bit(2)
1 = Starts 16-bit Timery
0 = Stops 16-bit Timery

bit 14 **Unimplemented:** Read as '0'

bit 13 **TSIDL:** Timery Stop in Idle Mode bit(2)
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12-10 **Unimplemented:** Read as '0'

bit 9-8 **TECS<1:0>:** Timery Extended Clock Source Select bits (selected when TCS = 1)(2,3)
11 = Generic Timer (TMRCK) external input
10 = LPRC Oscillator
01 = TxCK external clock input
00 = SOSC

bit 7 **Unimplemented:** Read as '0'

bit 6 **TGATE:** Timery Gated Time Accumulation Enable bit(2)
When TCS = 1:
This bit is ignored.
When TCS = 0:
1 = Gated time accumulation is enabled
0 = Gated time accumulation is disabled

bit 5-4 **TCKPS<1:0>:** Timery Input Clock Prescale Select bits(2)
11 = 1:256
10 = 1:64
01 = 1:8
00 = 1:1

bit 3-2 **Unimplemented:** Read as '0'

bit 1 **TCS:** Timery Clock Source Select bit(2,3)
1 = External clock from pin, TyCK (on the rising edge)
0 = Internal clock (FOSC/2)

bit 0 **Unimplemented:** Read as '0'

Note 1: Changing the value of TyCON while the timer is running (TON = 1) causes the timer prescale counter to reset and is not recommended.

2: When 32-bit operation is enabled (T2CON<3> or T4CON<3> = 1), these bits have no effect on Timery operation; all timer functions are set through T2CON and T4CON.

3: If TCS = 1 and TECS<1:0> = x1, the selected external timer input (TyCK) must be configured to an available RPn/RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

REGISTER 17-1: I2CxCONL: I2Cx CONTROL REGISTER LOW

R/W-0	U-0	R/W-0, HC	R/W-1	R/W-0	R/W-0	R/W-0	R/W-0
I2CEN	—	I2CSIDL	SCLREL(1)	STRICT	A10M	DISSLW	SMEN
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC	R/W-0, HC
GCEN	STREN	ACKDT	ACKEN	RCEN	PEN	RSEN	SEN
bit 7							bit 0

Legend:	HC = Hardware Clearable bit		
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **I2CEN:** I2Cx Enable bit (writable from SW only)
1 = Enables the I²C™ module, and configures the SDAx and SCLx pins as serial port pins
0 = Disables I²C module; all I²C pins are controlled by port functions

bit 14 **Unimplemented:** Read as '0'

bit 13 **I2CSIDL:** I2Cx Stop in Idle Mode bit
1 = Discontinues module operation when device enters Idle mode
0 = Continues module operation in Idle mode

bit 12 **SCLREL:** SCLx Release Control bit (I²C Slave mode only)(1)
Module resets and (I2CEN = 0) sets SCLREL = 1.
If STREN = 0:(2)
1 = Releases clock
0 = Forces clock low (clock stretch)
If STREN = 1:
1 = Releases clock
0 = Holds clock low (clock stretch); user may program this bit to '0', clock stretch is at the next SCLx low

bit 11 **STRICT:** I2Cx Strict Reserved Address Rule Enable bit
1 = Strict reserved addressing is enforced; for reserved addresses, refer to Table 17-1
(In Slave Mode) – The device doesn't respond to reserved address space and addresses falling in that category are NACKed.
(In Master Mode) – The device is allowed to generate addresses with reserved address space.
0 = Reserved addressing would be Acknowledged
(In Slave Mode) – The device will respond to an address falling in the reserved address space. When there is a match with any of the reserved addresses, the device will generate an ACK.
(In Master Mode) – Reserved.

bit 10 **A10M:** 10-Bit Slave Address Flag bit
1 = I2CxADD is a 10-bit slave address
0 = I2CADD is a 7-bit slave address

bit 9 **DISSLW:** Slew Rate Control Disable bit
1 = Slew rate control is disabled for Standard Speed mode (100 kHz, also disabled for 1 MHz mode)
0 = Slew rate control is enabled for High-Speed mode (400 kHz)

bit 8 **SMEN:** SMBus Input Levels Enable bit
1 = Enables input logic so thresholds are compliant with the SMBus specification
0 = Disables SMBus-specific inputs

Note 1: Automatically cleared to '0' at the beginning of slave transmission; automatically cleared to '0' at the end of slave reception.
2: Automatically cleared to '0' at the beginning of slave transmission.

REGISTER 18-3: UxTXREG: UARTx TRANSMIT REGISTER (NORMALLY WRITE-ONLY)

W-x	U-0	U-0	U-0	U-0	U-0	U-0	W-x
LAST(1)	—	—	—	—	—	—	UxTXREG8
bit 15							bit 8

W-x	W-x	W-x	W-x	W-x	W-x	W-x	W-x
UxTXREG<7:0>							
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **LAST:** Last Byte Indicator for Smart Card Support bit(1)

bit 14-9 **Unimplemented:** Read as '0'

bit 8 **UxTXREG8:** UARTx Data of the Transmitted Character bit (in 9-bit mode)

bit 7-0 **UxTXREG<7:0>:** UARTx Data of the Transmitted Character bits

Note 1: This bit is only available for UART1 and UART2.

REGISTER 18-4: UxADMD: UARTx ADDRESS MATCH DETECT REGISTER

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADMMASK7	ADMMASK6	ADMMASK5	ADMMASK4	ADMMASK3	ADMMASK2	ADMMASK1	ADMMASK0
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
ADMADDR7	ADMADDR6	ADMADDR5	ADMADDR4	ADMADDR3	ADMADDR2	ADMADDR1	ADMADDR0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-8 **ADMMASK<7:0>:** UARTx ADDMADDR<7:0> (UxADMD<7:0>) Masking bits

For ADMMASK<x>:

1 = ADMADDR<x> is used to detect the address match

0 = ADMADDR<x> is not used to detect the address match

bit 7-0 **ADMADDR<7:0>:** UARTx Address Detect Task Off-Load bits

Used with the ADMMASK<7:0> bits (UxADMD<15:8>) to off-load the task of detecting the address character from the processor during Address Detect mode.

19.1.2.3 VBUS Voltage Generation with External Devices

When operating as a USB host, either as an A-device in an OTG configuration or as an embedded host, VBUS must be supplied to the attached device. PIC24FJ128GB204 family devices have an internal VBUS boost assist to help generate the required 5V VBUS from the available voltages on the board. This is comprised of a simple PWM output to control a Switch mode power supply, and built-in comparators to monitor output voltage and limit current.

To enable voltage generation:

1. Verify that the USB module is powered (U1PWRC<0> = 1) and that the VBUS discharge is disabled (U1OTGCON<0> = 0).
2. Select the desired target voltage using the VBUSCHG bit (U1OTGCON<1>).
3. Enable the VBUS generation circuit (U1OTGCON<3> = 1).

Note: This section describes the general process for VBUS voltage generation and control. Please refer to the *"dsPIC33/PIC24 Family Reference Manual"* for additional examples.

19.1.3 CALCULATING TRANSCEIVER POWER REQUIREMENTS

The USB transceiver consumes a variable amount of current depending on the characteristic impedance of the USB cable, the length of the cable, the VUSB3V3 supply voltage and the actual data patterns moving across the USB cable. Longer cables have larger capacitances and consume more total energy when switching output states. The total transceiver current consumption will be application-specific. Equation 19-1 can help estimate how much current actually may be required in full-speed applications.

Refer to the *"dsPIC33/PIC24 Family Reference Manual*", **"USB On-The-Go (OTG)"** (DS39721) for a complete discussion on transceiver power consumption.

EQUATION 19-1: ESTIMATING USB TRANSCEIVER CURRENT CONSUMPTION

$$IXCVR = \frac{40\ mA \bullet V_{USB3V3} \bullet P_{ZERO} \bullet P_{IN} \bullet L_{CABLE}}{3.3V \bullet 5m} + I_{PULLUP}$$

Legend: V_{USB3V3} – Voltage applied to the VUSB3V3 pin in volts (3.0V to 3.6V).

P_{ZERO} – Percentage (in decimal) of the IN traffic bits sent by the PIC® microcontroller that are a value of '0'.

P_{IN} – Percentage (in decimal) of total bus bandwidth that is used for In traffic.

L_{CABLE} – Length (in meters) of the USB cable. The *"USB 2.0 Specification"* requires that full-speed applications use cables no longer than 5m.

I_{PULLUP} – Current which the nominal, 1.5 kΩ pull-up resistor (when enabled) must supply to the USB cable.

19.2 USB Buffer Descriptors and the BDT

Endpoint buffer control is handled through a structure called the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configurations.

The BDT can be located in any available, 512-byte aligned block of data RAM. The BDT Pointer (U1BDTP1) contains the upper address byte of the BDT and sets the location of the BDT in RAM. The user must set this pointer to indicate the table's location.

The BDT is composed of Buffer Descriptors (BDs) which are used to define and control the actual buffers in the USB RAM space. Each BD consists of two, 16-bit "soft" (non-fixed address) registers, BDnSTAT and BDnADR, where n represents one of the 64 possible BDs (range of 0 to 63). BDnSTAT is the status register for BDn, while BDnADR specifies the starting address for the buffer associated with BDn.

Note:	Since BDnADR is a 16-bit register, only the first 64 Kbytes of RAM can be accessed by the USB module.

Depending on the endpoint buffering configuration used, there are up to 64 sets of Buffer Descriptors, for a total of 256 bytes. At a minimum, the BDT must be at least 8 bytes long. This is because the *"USB 2.0 Specification"* mandates that every device must have Endpoint 0 with both input and output for initial setup.

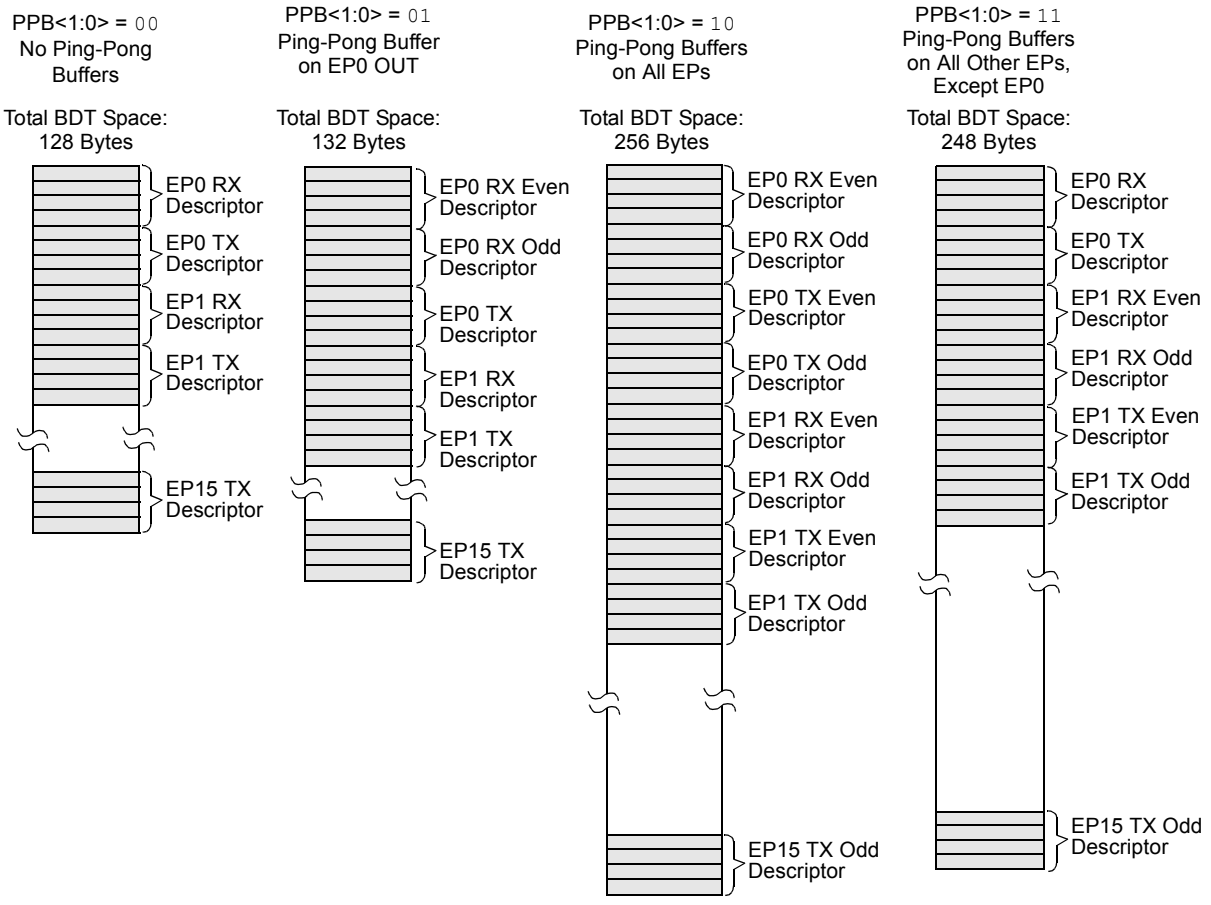
Endpoint mapping in the BDT is dependent on three variables:

- Endpoint number (0 to 15)
- Endpoint direction (RX or TX)
- Ping-pong settings (U1CNFG1<1:0>)

Figure 19-8 illustrates how these variables are used to map endpoints in the BDT.

In Host mode, only Endpoint 0 Buffer Descriptors are used. All transfers utilize the Endpoint 0 Buffer Descriptor and USB Endpoint Control register (U1EP0). For received packets, the attached device's source endpoint is indicated by the value of ENDPT<3:0> in the USB Status register (U1STAT<7:4>). For transmitted packets, the attached device's destination endpoint is indicated by the value written to the USB Token register (U1TOK).

FIGURE 19-8: BDT MAPPING FOR ENDPOINT BUFFERING MODES



Note: Memory area is not shown to scale.

REGISTER 21-6: PMCSxBS: EPMP CHIP SELECT x BASE ADDRESS REGISTER(2)

R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)	R/W(1)
BASE<23:16>							
bit 15							bit 8

R/W(1)	U-0	U-0	U-0	R/W(1)	U-0	U-0	U-0
BASE15	—	—	—	BASE11	—	—	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **BASE<23:15>:** Chip Select x Base Address bits(1)

bit 6-4 **Unimplemented:** Read as '0'

bit 3 **BASE11:** Chip Select x Base Address bit(1)

bit 2-0 **Unimplemented:** Read as '0'

Note 1: The value at POR is 0080h for PMCS1BS and 0880h for PMCS2BS.

2: If the whole PMCS2BS register is written together as 0x0000, then the last EDS address for Chip Select 1 will be FFFFFFh. In this case, Chip Select 2 should not be used. PMCS1BS has no such feature.

23.5.3 ENCRYPTING A SESSION KEY

Note: ECB and CBC modes are restricted to 128-bit session keys only.

1. If not already set, set the CRYON bit.
2. If not already programmed, program the SKEYEN bit to '1'.

Note: Setting SKEYEN permanently makes Key #1 available as a Key Encryption Key only. It cannot be used for other encryption or decryption operations after that.

3. Set OPMOD<3:0> to '1110'.
4. Configure the CPHRSEL, CPHRMOD<2:0> and KEYMOD<1:0> register bit fields as desired, set SKEYSEL to '0'.
5. Read the KEYFAIL status bit. If this bit is '1', an illegal configuration has been selected, and the encrypt operation will not be performed.
6. Write the software generated session key into the CRYKEY register or generate a random key into the CRYKEY register. It is only necessary to write the lowest *n* bits of CRYKEY for a key length of *n*, as all unused key bits are ignored.
7. Set the CRYGO bit. Poll the bit until it is cleared by hardware; alternatively, set the DONEIE bit (CRYCONL<11>) to generate an interrupt when the encryption is done.
8. Read the encrypted session key out of the appropriate CRYTXT register.
9. For total key lengths of more than 128 bits, set SKEYSEL to '1' and repeat Steps 6 and 7.
10. Set KEYSRC<3:0> to '0000' to use the session key to encrypt data.

23.5.4 RECEIVING A SESSION KEY

Note: ECB and CBC modes are restricted to 128-bit session keys only.

1. If not already set, set the CRYON bit.
2. If not already programmed, program the SKEYEN bit to '1'.

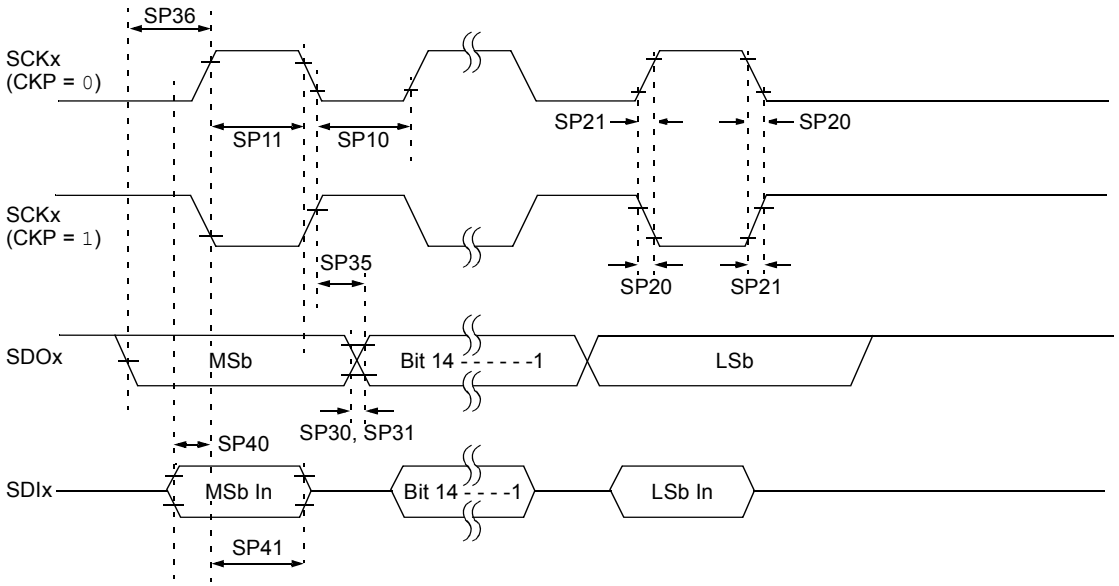
Note: Setting SKEYEN permanently makes Key #1 available as a Key Encryption Key only. It cannot be used for other encryption or decryption operations after that. It also permanently disables the ability of software to decrypt the session key into the CRYTXTA register, thereby breaking programmatic security (i.e., software can read the unencrypted key).

3. Set OPMOD<3:0> to '1111'.
4. Configure the CPHRSEL, CPHRMOD<2:0> and KEYMOD<1:0> register bit fields as desired, set SKEYSEL to '0'.
5. Read the KEYFAIL status bit. If this bit is '1', an illegal configuration has been selected and the encrypt operation will NOT be performed.
6. Write the encrypted session key received into the appropriate CRYTXT register.
7. Set the CRYGO bit. Poll the bit until it is cleared by hardware; alternatively, set the DONEIE bit (CRYCONL<11>) to generate an interrupt when the process is done.
8. For total key lengths of more than 128 bits, set SKEYSEL to '1' and repeat Steps 6 and 7.
9. Set KEYSRC<3:0> to '0000' to use the newly generated session key to encrypt and decrypt data.

TABLE 32-2: INSTRUCTION SET OVERVIEW (CONTINUED)

Assembly Mnemonic	Assembly Syntax		Description	# of Words	# of Cycles	Status Flags Affected
GOTO	GOTO	Expr	Go to Address	2	2	None
	GOTO	Wn	Go to Indirect	1	2	None
INC	INC	f	f = f + 1	1	1	C, DC, N, OV, Z
	INC	f,WREG	WREG = f + 1	1	1	C, DC, N, OV, Z
	INC	Ws,Wd	Wd = Ws + 1	1	1	C, DC, N, OV, Z
INC2	INC2	f	f = f + 2	1	1	C, DC, N, OV, Z
	INC2	f,WREG	WREG = f + 2	1	1	C, DC, N, OV, Z
	INC2	Ws,Wd	Wd = Ws + 2	1	1	C, DC, N, OV, Z
IOR	IOR	f	f = f .IOR. WREG	1	1	N, Z
	IOR	f,WREG	WREG = f .IOR. WREG	1	1	N, Z
	IOR	#lit10,Wn	Wd = lit10 .IOR. Wd	1	1	N, Z
	IOR	Wb,Ws,Wd	Wd = Wb .IOR. Ws	1	1	N, Z
	IOR	Wb,#lit5,Wd	Wd = Wb .IOR. lit5	1	1	N, Z
LNK	LNK	#lit14	Link Frame Pointer	1	1	None
LSR	LSR	f	f = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	f,WREG	WREG = Logical Right Shift f	1	1	C, N, OV, Z
	LSR	Ws,Wd	Wd = Logical Right Shift Ws	1	1	C, N, OV, Z
	LSR	Wb,Wns,Wnd	Wnd = Logical Right Shift Wb by Wns	1	1	N, Z
	LSR	Wb,#lit5,Wnd	Wnd = Logical Right Shift Wb by lit5	1	1	N, Z
MOV	MOV	f,Wn	Move f to Wn	1	1	None
	MOV	[Wns+Slit10],Wnd	Move [Wns+Slit10] to Wnd	1	1	None
	MOV	f	Move f to f	1	1	N, Z
	MOV	f,WREG	Move f to WREG	1	1	N, Z
	MOV	#lit16,Wn	Move 16-bit Literal to Wn	1	1	None
	MOV.b	#lit8,Wn	Move 8-bit Literal to Wn	1	1	None
	MOV	Wn,f	Move Wn to f	1	1	None
	MOV	Wns,[Wns+Slit10]	Move Wns to [Wns+Slit10]	1	1	
	MOV	Wso,Wdo	Move Ws to Wd	1	1	None
	MOV	WREG,f	Move WREG to f	1	1	N, Z
	MOV.D	Wns,Wd	Move Double from W(ns):W(ns+1) to Wd	1	2	None
	MOV.D	Ws,Wnd	Move Double from Ws to W(nd+1):W(nd)	1	2	None
MUL	MUL.SS	Wb,Ws,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Signed(Ws)	1	1	None
	MUL.SU	Wb,Ws,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(Ws)	1	1	None
	MUL.US	Wb,Ws,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Signed(Ws)	1	1	None
	MUL.UU	Wb,Ws,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(Ws)	1	1	None
	MUL.SU	Wb,#lit5,Wnd	{Wnd+1, Wnd} = Signed(Wb) * Unsigned(lit5)	1	1	None
	MUL.UU	Wb,#lit5,Wnd	{Wnd+1, Wnd} = Unsigned(Wb) * Unsigned(lit5)	1	1	None
	MUL	f	W3:W2 = f * WREG	1	1	None
NEG	NEG	f	f = $\bar{f}$ + 1	1	1	C, DC, N, OV, Z
	NEG	f,WREG	WREG = $\bar{f}$ + 1	1	1	C, DC, N, OV, Z
	NEG	Ws,Wd	Wd = $\overline{Ws}$ + 1	1	1	C, DC, N, OV, Z
NOP	NOP		No Operation	1	1	None
	NOPR		No Operation	1	1	None
POP	POP	f	Pop f from Top-of-Stack (TOS)	1	1	None
	POP	Wdo	Pop from Top-of-Stack (TOS) to Wdo	1	1	None
	POP.D	Wnd	Pop from Top-of-Stack (TOS) to W(nd):W(nd+1)	1	2	None
	POP.S		Pop Shadow Registers	1	1	All
PUSH	PUSH	f	Push f to Top-of-Stack (TOS)	1	1	None
	PUSH	Wso	Push Wso to Top-of-Stack (TOS)	1	1	None
	PUSH.D	Wns	Push W(ns):W(ns+1) to Top-of-Stack (TOS)	1	2	None
	PUSH.S		Push Shadow Registers	1	1	None

FIGURE 33-10: SPIx MODULE MASTER MODE (CKE = 1) TIMING CHARACTERISTICS



Note: Refer to Figure 33-2 for load conditions.

TABLE 33-33: SPIx MODULE MASTER MODE (CKE = 1) TIMING REQUIREMENTS

AC CHARACTERISTICS			Standard Operating Conditions: 2.0V to 3.6V (unless otherwise stated) Operating temperature -40°C ≤ TA ≤ +85°C for Industrial -40°C ≤ TA ≤ +125°C for Extended				
Param No.	**Symbol**	**Characteristic(1)**	**Min**	**Typ(2)**	**Max**	**Units**	**Conditions**
SP10	TscL	SCKx Output Low Time(3)	TCY/2	—	—	ns	
SP11	TscH	SCKx Output High Time(3)	TCY/2	—	—	ns	
SP20	TscF	SCKx Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP21	TscR	SCKx Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP30	TdoF	SDOx Data Output Fall Time(4)	—	—	—	ns	See Parameter DO32
SP31	TdoR	SDOx Data Output Rise Time(4)	—	—	—	ns	See Parameter DO31
SP35	TscH2doV, TscL2doV	SDOx Data Output Valid After SCKx Edge	—	6	20	ns	
SP36	TdoV2sc, TdoV2scL	SDOx Data Output Setup to First SCKx Edge	30	—	—	ns	
SP40	TdiV2scH, TdiV2scL	Setup Time of SDIx Data Input to SCKx Edge	23	—	—	ns	
SP41	TscH2diL, TscL2diL	Hold Time of SDIx Data Input to SCKx Edge	30	—	—	ns	

Note 1: These parameters are characterized but not tested in manufacturing.

2: Data in "Typ" column is at 3.3V, +25°C unless otherwise stated.

3: The minimum clock period for SCKx is 100 ns. Therefore, the clock generated in Master mode must not violate this specification.

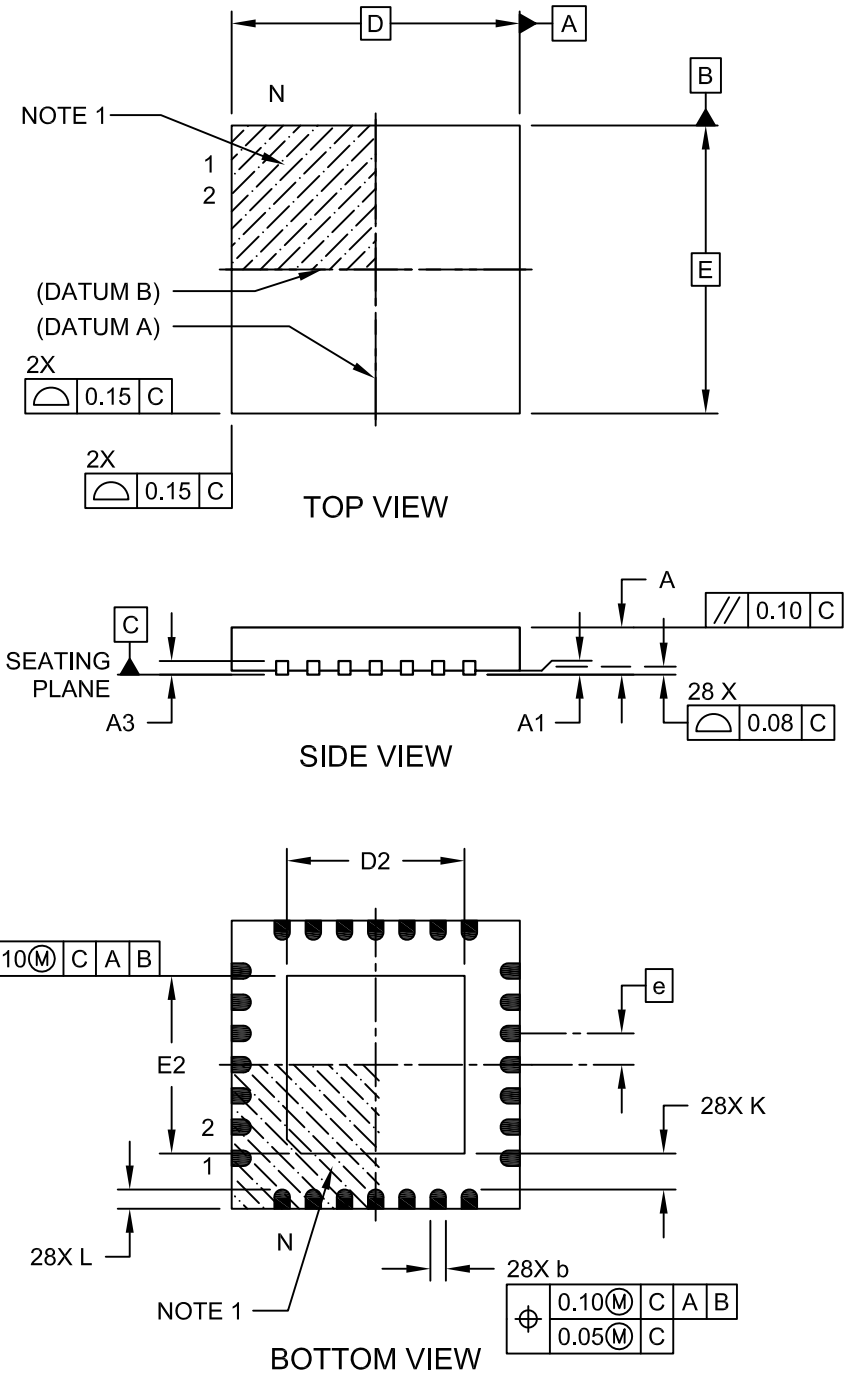
4: Assumes 50 pF load on all SPIx pins.

34.2 Package Details

The following sections give the technical details of the packages.

28-Lead Plastic Quad Flat, No Lead Package (MM) - 6x6x0.9mm Body [QFN-S] With 0.40 mm Terminal Length

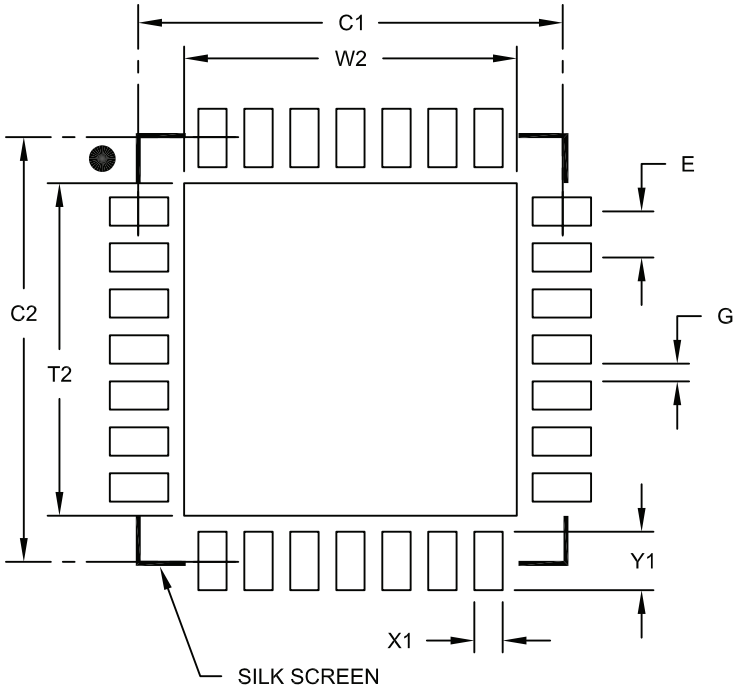
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-124C Sheet 1 of 2

28-Lead Plastic Quad Flat, No Lead Package (MM) – 6x6x0.9 mm Body [QFN-S] with 0.40 mm Contact Length

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Optional Center Pad Width	W2			4.70
Optional Center Pad Length	T2			4.70
Contact Pad Spacing	C1		6.00	
Contact Pad Spacing	C2		6.00	
Contact Pad Width (X28)	X1			0.40
Contact Pad Length (X28)	Y1			0.85
Distance Between Pads	G	0.25		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2124A