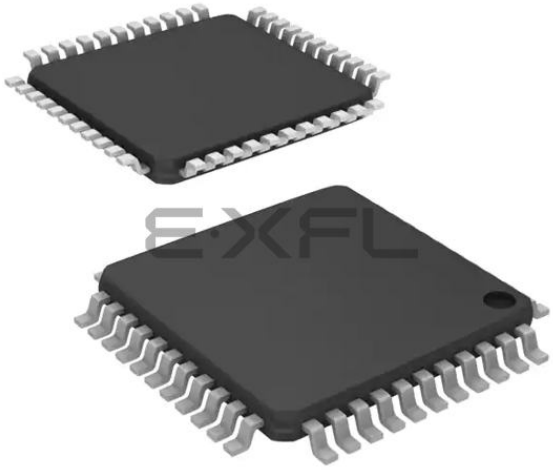

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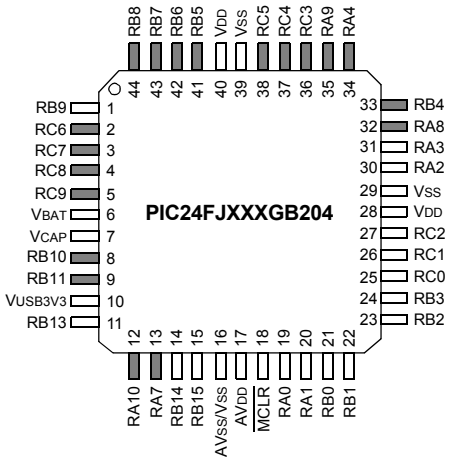
Details	
Product Status	Active
Core Processor	PIC
Core Size	16-Bit
Speed	32MHz
Connectivity	I²C, IrDA, LINbus, PMP, SPI, UART/USART, USB OTG
Peripherals	Brown-out Detect/Reset, DMA, LVD, POR, PWM, WDT
Number of I/O	34
Program Memory Size	128KB (43K x 24)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	8K x 8
Voltage - Supply (Vcc/Vdd)	2V ~ 3.6V
Data Converters	A/D 12x10b/12b
Oscillator Type	Internal
Operating Temperature	-40°C ~ 125°C (TA)
Mounting Type	Surface Mount
Package / Case	44-TQFP
Supplier Device Package	44-TQFP (10x10)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/pic24fj128gb204-e-pt

Pin Diagrams (Continued)

44-Pin TQFP,
44-Pin QFN(1,2,3)



Note 1: Gray shading indicates 5.5V tolerant input pins.
2: The back pad on QFN devices should be connected to VSS.
3: See Table 1 for complete pinout descriptions.

TABLE 1: PIC24FJXXXGB204 PIN FUNCTION DESCRIPTIONS

Pin	Function	Pin	Function
1	C1INC/C2INC/C3INC/**RP9**/SDA1/T1CK/CTED4/PMD3/CN21/RB9	23	AN4/C1INB/**RP2**/SDA2/T5CK/T4CK/CTED13/CN6/PMD2/RB2
2	**RP22**/PMA1/PMALH/CN18/RC6	24	AN5/C1INA/**RP3**/SCL2/CTED8/CN7/PMWR/RB3
3	**RP23**/PMA0/PMALL/CN17/RC7	25	AN10/**RP16**/PMBE1/CN8/RC0
4	**RP24**/PMA5/CN20/RC8	26	AN11/**RP17**/CN9/RC1
5	**RP25**/CTED7/PMA6/CN19/RC9	27	AN12/**RP18**/PMACK1/CN10/RC2
6	VBAT	28	VDD
7	VCAP	29	VSS
8	**RP10**/CTED11/CN16/PGD2/D+/RB10	30	OSCI/C1IND/CLKI/PMCS1/CN30/RA2
9	REFI/**RP11**/CTED9/CN15/PGC2/D-/RB11	31	OSCO/C2IND/CLKO/CN29/RA3
10	VUSB3V3	32	TDO/PMA8/CN34/RA8
11	AN7/C1INC/REFO/**RP13**/CTPLS/PMRD/CN13/RB13	33	SOSCI/CN1/**RPI4**/RB4
12	TMS/PMA2/PMALU/CN36/RA10	34	SOSCO/SCLKI/CN0/RA4
13	TCK/PMA7/CN33/RA7	35	TDI/PMA9/CN35/RA9
14	CVREF/AN6/C3INB/**RP14**/RTCC/CTED5/CN12/RB14	36	**RP19**/PMBE0/CN28/RC3
15	AN9/C3INA/**RP15**/T3CK/T2CK/CTED6/PMA14/CS1/CN11/PMCS/PMCS1/RB15	37	**RP20**/PMA4/CN25/RC4
16	AVSS/VSS	38	**RP21**/PMA3/CN26/RC5
17	AVDD	39	VSS
18	$\overline{\text{MCLR}}$	40	VDD
19	CVREF+/VREF+/AN0/C3INC/**RP5**/ASDA1(1)/CTED1/CN2/PMD7/PGD3/RA0	41	CN27/USBID/RB5
20	CVREF-/VREF-/AN1/C3IND/**RP6**/ASCL1(1)/CTED2/CN3/PGC3/RA1	42	PMD6/CN24/VBUS/RB6
21	AN2/CTCMP/C2INB/**RP0**/CN4/PGD1/HLVDIN/PMD0/RB0	43	**RP7**/CTED3/INT0/CN23/PMD5/RB7
22	AN3/C2INA/**RP1**/CTED12/CN5/PMD1/PGC1/RB1	44	**RP8**/SCL1/CTED10/PMD4/CN22/USBOEN/RB8

Legend: **RPn** represents remappable peripheral pins.
Note 1: Alternative multiplexing for SDA1 and SCL1 when the I2C1SEL Configuration bit is set.

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
CN0	12	9	34	—	—	Interrupt-on-Change Inputs.
CN1	11	8	33	—	—	
CN2	2	27	19	—	—	
CN3	3	28	20	—	—	
CN4	4	1	21	—	—	
CN5	5	2	22	—	—	
CN6	6	3	23	—	—	
CN7	7	4	24	—	—	
CN8	—	—	25	—	—	
CN9	—	—	26	—	—	
CN10	—	—	27	—	—	
CN11	26	23	15	—	—	
CN12	25	22	14	—	—	
CN13	24	21	11	—	—	
CN15	22	19	9	—	—	
CN16	21	18	8	—	—	
CN17	—	—	3	—	—	
CN18	—	—	2	—	—	
CN19	—	—	5	—	—	
CN20	—	—	4	—	—	
CN21	18	15	1	—	—	
CN22	17	14	44	—	—	
CN23	16	13	43	—	—	
CN24	15	12	42	—	—	
CN25	—	—	37	—	—	
CN26	—	—	38	—	—	
CN27	14	11	41	—	—	
CN28	—	—	36	—	—	
CN29	10	7	31	—	—	
CN30	9	6	30	—	—	
CN33	—	—	13	—	—	
CN34	—	—	32	—	—	
CN35	—	—	35	—	—	
CN36	—	—	12	—	—	
CTCMP	4	1	21	I	ANA	CTMU Comparator 2 Input (Pulse mode).

Legend: ST = Schmitt Trigger input
TTL = TTL compatible input
I = Input
ANA = Analog input
O = Output
P = Power
I^2C = ST with I^2C™ or SMBus levels

TABLE 1-3: PIC24FJ128GB204 FAMILY PINOUT DESCRIPTION (CONTINUED)

Pin Function	Pin Number/Grid Locator			I/O	Input Buffer	Description
	28-Pin SPDIP/SOIC/ SSOP	28-Pin QFN-S	44-Pin TQFP/QFN			
RP0	4	1	21	I/O	ST	Remappable Peripheral (input or output).
RP1	5	2	22	I/O	ST	
RP2	6	3	23	I/O	ST	
RP3	7	4	24	I/O	ST	
RP5	2	27	19	I/O	ST	
RP6	3,15	28	20	I/O	ST	
RP7	16	13	43	I/O	ST	
RP8	17	14	44	I/O	ST	
RP9	18	15	1	I/O	ST	
RP10	21	18	8	I/O	ST	
RP11	22	19	9	I/O	ST	
RP13	24	21	11	I/O	ST	
RP14	25	22	14	I/O	ST	
RP15	26	23	15	I/O	ST	
RP16	—	—	25	I/O	ST	
RP17	—	—	26	I/O	ST	
RP18	—	—	27	I/O	ST	
RP19	—	—	36	I/O	ST	
RP20	—	—	37	I/O	ST	
RP21	—	—	38	I/O	ST	
RP22	—	—	2	I/O	ST	
RP23	—	—	3	I/O	ST	
RP24	—	—	4	I/O	ST	
RP25	—	—	5	I/O	ST	
RPI4	11	8	33	I	ST	Remappable Peripheral (input).
RTCC	25	22	14	O	—	Real-Time Clock Alarm/Seconds Pulse Output.
SCL1	17	14	44	I/O	I^2C	I2C1 Synchronous Serial Clock Input/Output.
SCL2	7	4	24	I/O	I^2C	I2C2 Synchronous Serial Clock Input/Output.
SCLKI	12	9	34	I	—	Secondary Oscillator Digital Clock Input.
SDA1	18	15	1	I/O	I^2C	I2C1 Data Input/Output.
SDA2	6	3	23	I/O	I^2C	I2C2 Data Input/Output.
SOSCI	11	8	33	I	ANA	Secondary Oscillator/Timer1 Clock Input.
SOSCO	12	9	34	O	ANA	Secondary Oscillator/Timer1 Clock Output.

Legend: ST = Schmitt Trigger input
ANA = Analog input
I^2C = ST with I^2C™ or SMBus levels
TTL = TTL compatible input
O = Output
I = Input
P = Power

REGISTER 3-2: CORCON: CPU CORE CONTROL REGISTER

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	U-0	U-0	U-0	R/C-0	r-1	U-0	U-0
—	—	—	—	IPL3(1)	—	—	—
bit 7							bit 0

Legend:	C = Clearable bit	r = Reserved bit	
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-4 **Unimplemented:** Read as '0'

bit 3 **IPL3:** CPU Interrupt Priority Level Status bit(1)
1 = CPU Interrupt Priority Level is greater than 7
0 = CPU Interrupt Priority Level is 7 or less

bit 2 **Reserved:** Read as '1'

bit 1-0 **Unimplemented:** Read as '0'

Note 1: The IPL3 bit is concatenated with the IPL<2:0> bits (SR<7:5>) to form the CPU Interrupt Priority Level; see Register 3-1 for bit description.

TABLE 4-11: SPI1 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI1CON1L	0300	SPIEN	—	SPISIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF	0000
SPI1CON1H	0302	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD1	AUDMOD0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT2	FRMCNT1	FRMCNT0	0000
SPI1CON2L	0304	—	—	—	—	—	—	—	—	—	—	—	WLENGTH<4:0>					0000
SPI1STATL	0308	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
SPI1STATH	030A	—	—	RXELM5	RXELM4	RXELM3	RXELM2	RXELM1	RXELM0	—	—	TXELM5	TXELM4	TXELM3	TXELM2	TXELM1	TXELM0	0000
SPI1BUFL	030C	SPI1BUFL<15:0>																0000
SPI1BUFH	030E	SPI1BUFH<31:16>																0000
SPI1BRGL	0310	—	—	—	SPI1BRG<12:0>													0000
SPI1IMSKL	0314	—	—	—	FRMERREN	BUSYEN	—	—	SPITUREN	SRMTEN	SPIROVEN	SPIRBEN	—	SPITBEN	—	SPITBFEN	SPIRBFEN	0000
SPI1IMSKH	0316	RXWIEN	—	RXMSK5	RXMSK4	RXMSK3	RXMSK2	RXMSK1	RXMSK0	TXWIEN	—	TXMSK5	TXMSK4	TXMSK3	TXMSK2	TXMSK1	TXMSK0	0000
SPI1URDTL	0318	SPI1URDTL<15:0>																0000
SPI1URDTH	031A	SPI1URDTH<31:16>																0000

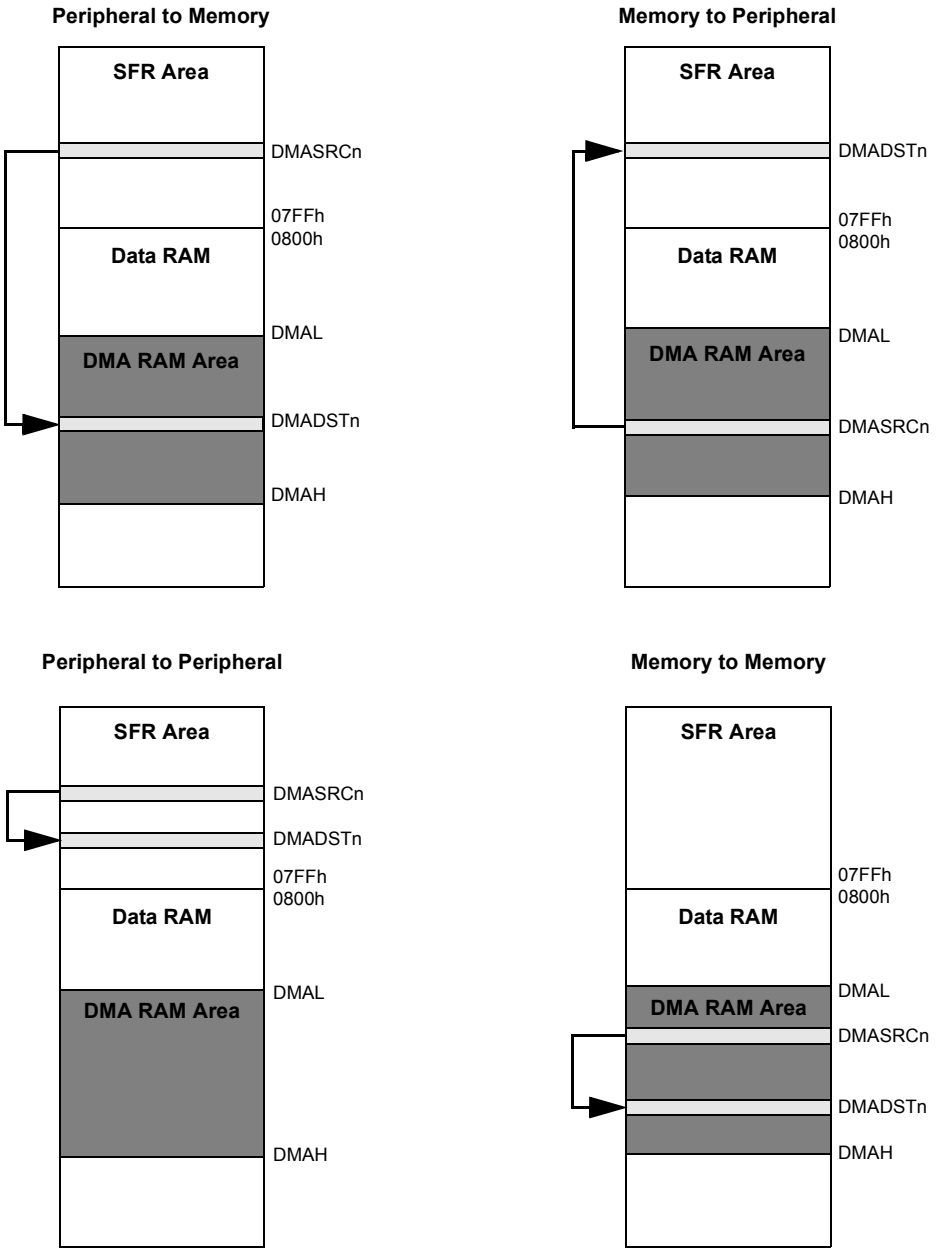
Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

TABLE 4-12: SPI2 REGISTER MAP

File Name	Addr	Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	All Resets
SPI2CON1L	031C	SPIEN	—	SPISIDL	DISSDO	MODE32	MODE16	SMP	CKE	SSEN	CKP	MSTEN	DISSDI	DISSCK	MCLKEN	SPIFE	ENHBUF	0000
SPI2CON1H	031E	AUDEN	SPISGNEXT	IGNROV	IGNTUR	AUDMONO	URDTEN	AUDMOD1	AUDMOD0	FRMEN	FRMSYNC	FRMPOL	MSSEN	FRMSYPW	FRMCNT2	FRMCNT1	FRMCNT0	0000
SPI2CON2L	0320	—	—	—	—	—	—	—	—	—	—	—	WLENGTH<4:0>					0000
SPI2STATL	0324	—	—	—	FRMERR	SPIBUSY	—	—	SPITUR	SRMT	SPIROV	SPIRBE	—	SPITBE	—	SPITBF	SPIRBF	0028
SPI2STATH	0326	—	—	RXELM5	RXELM4	RXELM3	RXELM2	RXELM1	RXELM0	—	—	TXELM5	TXELM4	TXELM3	TXELM2	TXELM1	TXELM0	0000
SPI2BUFL	0328	SPI2BUFL<15:0>																0000
SPI2BUFH	032A	SPI2BUFH<31:16>																0000
SPI2BRGL	032C	—	—	—	SPI2BRG<12:0>													0000
SPI2IMSKL	0330	—	—	—	FRMERREN	BUSYEN	—	—	SPITUREN	SRMTEN	SPIROVEN	SPIRBEN	—	SPITBEN	—	SPITBFEN	SPIRBFEN	0000
SPI2IMSKH	0332	RXWIEN	—	RXMSK5	RXMSK4	RXMSK3	RXMSK2	RXMSK1	RXMSK0	TXWIEN	—	TXMSK5	TXMSK4	TXMSK3	TXMSK2	TXMSK1	TXMSK0	0000
SPI2URDTL	0334	SPI2URDTL<15:0>																0000
SPI2URDTH	0336	SPI2URDTH<31:16>																0000

Legend: — = unimplemented, read as '0'. Reset values are shown in hexadecimal.

FIGURE 5-2: TYPES OF DMA DATA TRANSFERS



Note: Relative sizes of memory areas are not shown to scale.

REGISTER 8-7: IFS2: INTERRUPT FLAG STATUS REGISTER 2

U-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	R/W-0
—	DMA4IF	PMPIF	—	—	OC6IF	OC5IF	IC6IF
bit 15							bit 8

R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
IC5IF	IC4IF	IC3IF	DMA3IF	CRYROLLIF	CRYFREEIF	SPI2TXIF	SPI2IF
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **DMA4IF:** DMA Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 13 **PMPIF:** Parallel Master Port Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **OC6IF:** Output Compare Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 9 **OC5IF:** Output Compare Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 8 **IC6IF:** Input Capture Channel 6 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 7 **IC5IF:** Input Capture Channel 5 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 6 **IC4IF:** Input Capture Channel 4 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 5 **IC3IF:** Input Capture Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 4 **DMA3IF:** DMA Channel 3 Interrupt Flag Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 3 **CRYROLLIF:** Cryptographic Rollover Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

bit 2 **CRYFREEIF:** Cryptographic Buffer Free Status bit
1 = Interrupt request has occurred
0 = Interrupt request has not occurred

REGISTER 8-16: IEC3: INTERRUPT ENABLE CONTROL REGISTER 3

U-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	U-0	R/W-0
—	RTCIE	DMA5IE	SPI3RXIE	SPI2RXIE	SPI1RXIE	—	KEYSTRIE
bit 15							bit 8

R/W-0	R/W-0	R/W-0	U-0	U-0	R/W-0	R/W-0	U-0
CRYDNIE	INT4IE(1)	INT3IE(1)	—	—	MI2C2IE	SI2C2IE	—
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **Unimplemented:** Read as '0'

bit 14 **RTCIE:** Real-Time Clock and Calendar Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 13 **DMA5IE:** DMA Channel 5 Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 12 **SPI3RXIE:** SPI3 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 11 **SPI2RXIE:** SPI2 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 10 **SPI1RXIE:** SPI1 Receive Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 9 **Unimplemented:** Read as '0'

bit 8 **KEYSTRIE:** Cryptographic Key Store Program Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 7 **CRYDNIE:** Cryptographic Operation Done Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 6 **INT4IE:** External Interrupt 4 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 5 **INT3IE:** External Interrupt 3 Enable bit(1)
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

bit 4-3 **Unimplemented:** Read as '0'

bit 2 **MI2C2IE:** Master I2C2 Event Interrupt Enable bit
1 = Interrupt request is enabled
0 = Interrupt request is not enabled

Note 1: If an external interrupt is enabled, the interrupt input must also be configured to an available RPn or RPIn pin. For more information, see **Section 11.4 "Peripheral Pin Select (PPS)"**.

9.4 Clock Switching Operation

With few limitations, applications are free to switch between any of the four clock sources (POSC, SOSC, FRC and LPRC) under software control and at any time. To limit the possible side effects that could result from this flexibility, PIC24F devices have a safeguard lock built into the switching process.

Note:	The Primary Oscillator mode has three different submodes (XT, HS and EC) which are determined by the POSCMDx Configuration bits. While an application can switch to and from Primary Oscillator mode in software, it cannot switch between the different primary submodes without reprogramming the device.

9.4.1 ENABLING CLOCK SWITCHING

To enable clock switching, the FCKSM1 Configuration bit in CW2 must be programmed to '0'. (For more information, refer to **Section 30.1 "Configuration Bits"**.) If the FCKSM1 Configuration bit is unprogrammed ('1'), the clock switching function and Fail-Safe Clock Monitor function are disabled; this is the default setting.

The NOSCx control bits (OSCCON<10:8>) do not control the clock selection when clock switching is disabled. However, the COSC<2:0> bits (OSCCON<14:12>) will reflect the clock source selected by the FNOSCx Configuration bits.

The OSWEN control bit (OSCCON<0>) has no effect when clock switching is disabled; it is held at '0' at all times.

9.4.2 OSCILLATOR SWITCHING SEQUENCE

At a minimum, performing a clock switch requires this basic sequence:

1. If desired, read the COSC<2:0> bits (OSCCON<14:12>) to determine the current oscillator source.
2. Perform the unlock sequence to allow a write to the OSCCON register high byte.
3. Write the appropriate value to the NOSCx bits (OSCCON<10:8>) for the new oscillator source.
4. Perform the unlock sequence to allow a write to the OSCCON register low byte.
5. Set the OSWEN bit to initiate the oscillator switch.

Once the basic sequence is completed, the system clock hardware responds automatically as follows:

1. The clock switching hardware compares the COSCx bits with the new value of the NOSCx bits. If they are the same, then the clock switch is a redundant operation. In this case, the OSWEN bit is cleared automatically and the clock switch is aborted.
2. If a valid clock switch has been initiated, the LOCK (OSCCON<5>) and CF (OSCCON<3>) bits are cleared.
3. The new oscillator is turned on by the hardware if it is not currently running. If a crystal oscillator must be turned on, the hardware will wait until the OST expires. If the new source is using the PLL, then the hardware waits until a PLL lock is detected (LOCK = 1).
4. The hardware waits for 10 clock cycles from the new clock source and then performs the clock switch.
5. The hardware clears the OSWEN bit to indicate a successful clock transition. In addition, the NOSCx bits value is transferred to the COSCx bits.
6. The old clock source is turned off at this time, with the exception of LPRC (if WDT or FSCM is enabled) or SOSC (if SOSCEN remains set).

Note 1:	The processor will continue to execute code throughout the clock switching sequence. Timing-sensitive code should not be executed during this time.
2:	Direct clock switches between any Primary Oscillator mode with PLL and FRCPLL mode are not permitted. This applies to clock switches in either direction. In these instances, the application must switch to FRC mode as a transitional clock source between the two PLL modes.

REGISTER 11-16: RPINR22: PERIPHERAL PIN SELECT INPUT REGISTER 22

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SCK2R5	SCK2R4	SCK2R3	SCK2R2	SCK2R1	SCK2R0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SDI2R5	SDI2R4	SDI2R3	SDI2R2	SDI2R1	SDI2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **SCK2R<5:0>:** Assign SPI2 Clock Input (SCK2IN) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **SDI2R<5:0>:** Assign SPI2 Data Input (SDI2) to Corresponding RPn or RPIn Pin bits

REGISTER 11-17: RPINR23: PERIPHERAL PIN SELECT INPUT REGISTER 23

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	TMRCKR5	TMRCKR4	TMRCKR3	TMRCKR2	TMRCKR1	TMRCKR0
bit 15							bit 8

U-0	U-0	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
—	—	SS2R5	SS2R4	SS2R3	SS2R2	SS2R1	SS2R0
bit 7							bit 0

Legend:			
R = Readable bit	W = Writable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-14 **Unimplemented:** Read as '0'

bit 13-8 **TMRCKR<5:0>:** Assign General Timer External Input (TMRCK) to Corresponding RPn or RPIn Pin bits

bit 7-6 **Unimplemented:** Read as '0'

bit 5-0 **SS2R<5:0>:** Assign SPI2 Slave Select Input (SS2IN) to Corresponding RPn or RPIn Pin bits

REGISTER 14-2: ICxCON2: INPUT CAPTURE x CONTROL REGISTER 2 (CONTINUED)

bit 4-0 **SYNCSEL<4:0>:** Synchronization/Trigger Source Selection bits

1111x = Reserved
11101 = Reserved
11100 = CTMU(1)
11011 = A/D(1)
11010 = Comparator 3(1)
11001 = Comparator 2(1)
11000 = Comparator 1(1)
10111 = Reserved
10110 = Reserved
10101 = Input Capture 6(2)
10100 = Input Capture 5(2)
10011 = Input Capture 4(2)
10010 = Input Capture 3(2)
10001 = Input Capture 2(2)
10000 = Input Capture 1(2)
01111 = Timer5
01110 = Timer4
01101 = Timer3
01100 = Timer2
01011 = Timer1
01010 = Reserved
01001 = Reserved
01000 = Reserved
00111 = Reserved
00110 = Output Compare 6
00101 = Output Compare 5
00100 = Output Compare 4
00011 = Output Compare 3
00010 = Output Compare 2
00001 = Output Compare 1
00000 = Not synchronized to any other module

Note 1: Use these inputs as trigger sources only and never as sync sources.
2: Never use an IC module as its own trigger source by selecting this mode.

15.0 OUTPUT COMPARE WITH DEDICATED TIMERS

Note: This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information, refer to the *"dsPIC33/PIC24 Family Reference Manual",* **"Output Compare with Dedicated Timer"** (DS70005159). The information in this data sheet supersedes the information in the FRM.

Devices in the PIC24FJ128GB204 family all feature six independent output compare modules. Each of these modules offers a wide range of configuration and operating options for generating pulse trains on internal device events, and can produce Pulse-Width Modulated (PWM) waveforms for driving power applications.

Key features of the output compare module include:

- Hardware-configurable for 32-bit operation in all modes by cascading two adjacent modules
- Synchronous and Trigger modes of output compare operation, with up to 31 user-selectable trigger/sync sources available
- Two separate Period registers (a main register, OCxR, and a secondary register, OCxRS) for greater flexibility in generating pulses of varying widths
- Configurable for single pulse or continuous pulse generation on an output event, or continuous PWM waveform generation
- Up to 6 clock sources available for each module, driving a separate internal 16-bit counter

15.1 General Operating Modes

15.1.1 SYNCHRONOUS AND TRIGGER MODES

When the output compare module operates in a Free-Running mode, the internal 16-bit counter, OCxTMR, runs counts up continuously, wrapping around from 0xFFFF to 0x0000 on each overflow. Its period is synchronized to the selected external clock source. Compare or PWM events are generated each time a match between the internal counter and one of the Period registers occurs.

In Synchronous mode, the module begins performing its compare or PWM operation as soon as its selected clock source is enabled. Whenever an event occurs on the selected sync source, the module's internal counter is reset. In Trigger mode, the module waits for a sync event from another internal module to occur before allowing the counter to run.

Free-Running mode is selected by default or any time that the SYNCSELx bits (OCxCON2<4:0>) are set to '00000'. Synchronous or Trigger modes are selected any time the SYNCSELx bits are set to any value except '00000'. The OCTRIG bit (OCxCON2<7>) selects either Synchronous or Trigger mode; setting the bit selects Trigger mode operation. In both modes, the SYNCSELx bits determine the sync/trigger source.

15.1.2 CASCADED (32-BIT) MODE

By default, each module operates independently with its own set of 16-bit Timer and Duty Cycle registers. To increase resolution, adjacent even and odd modules can be configured to function as a single 32-bit module. (For example, Modules 1 and 2 are paired, as are Modules 3 and 4, and so on.) The odd numbered module, Output Compare x (OCx), provides the Least Significant 16 bits of the 32-bit register pairs and the even numbered module, Output Compare y (OCy), provides the Most Significant 16 bits. Wrap arounds of the OCx registers cause an increment of their corresponding OCy registers.

Cascaded operation is configured in hardware by setting the OC32 bit (OCxCON2<8>) for both modules. For more information on cascading, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"Output Compare with Dedicated Timer"** (DS70005159).

16.3 Enhanced Slave Mode

To set up the SPIx module for the Enhanced Buffer Master mode of operation:

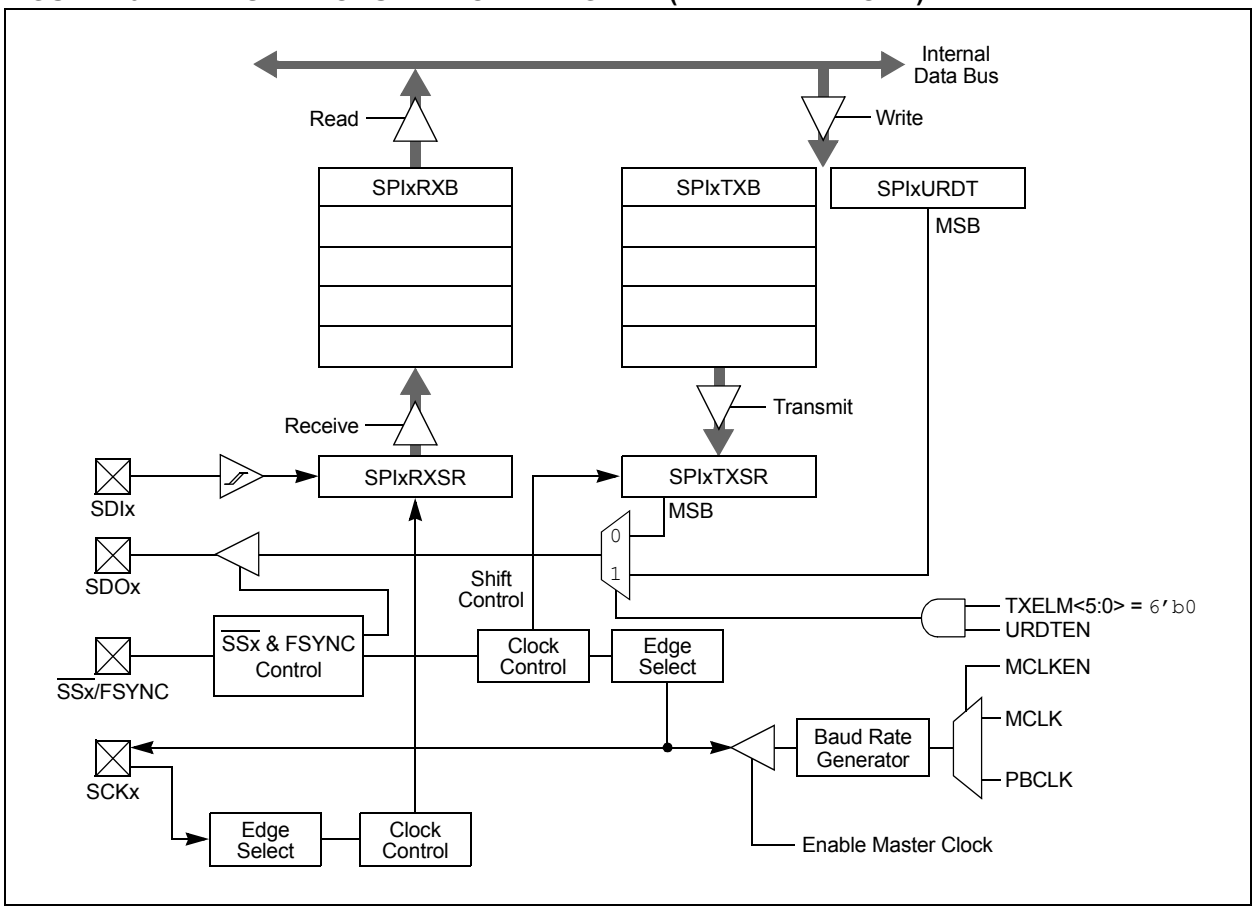
1. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP<2:0> bits in the respective IPCx register.
2. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with MSTEN (SPIxCON1L<5>) = 1.
3. Clear the SPIROV bit (SPIxSTATL<6>).
4. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
5. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).
6. Write the data to be transmitted to the SPIxBUFL and SPIxBUFH registers. Transmission (and reception) will start as soon as data is written to the SPIxBUFL and SPIxBUFH registers.

16.4 Enhanced Master Mode

To set up the SPIx module for the Enhanced Buffer Slave mode of operation:

1. Clear the SPIxBUFL and SPIxBUFH registers.
2. If using interrupts:
   a) Clear the interrupt flag bits in the respective IFSx register.
   b) Set the interrupt enable bits in the respective IECx register.
   c) Write the SPIxIP<2:0> bits in the respective IPCx register to set the interrupt priority.
3. Write the desired settings to the SPIxCON1L, SPIxCON1H and SPIxCON2L registers with the MSTEN bit (SPIxCON1L<5>) = 0.
4. Clear the SMP bit.
5. If the CKE bit is set, then the SSEN bit must be set, thus enabling the $\overline{SSx}$ pin.
6. Clear the SPIROV bit (SPIxSTATL<6>).
7. Select Enhanced Buffer mode by setting the ENHBUF bit (SPIxCON1L<0>).
8. Enable SPIx operation by setting the SPIEN bit (SPIxCON1L<15>).

FIGURE 16-2: SPIx MODULE BLOCK DIAGRAM (ENHANCED MODE)



REGISTER 17-3: I2CxSTAT: I2Cx STATUS REGISTER

R-0, HSC	R-0, HSC	R-0, HSC	U-0	U-0	R/C-0, HSC	R-0, HSC	R-0, HSC
ACKSTAT	TRSTAT	ACKTIM	—	—	BCL	GCSTAT	ADD10
bit 15							bit 8

R/C-0, HS	R/C-0, HS	R-0, HSC	R/C-0, HSC	R/C-0, HSC	R-0, HSC	R-0, HSC	R-0, HSC
IWCOL	I2COV	D/$\overline{A}$	P	S	R/$\overline{W}$	RBF	TBF
bit 7							bit 0

Legend:	C = Clearable bit	HSC = Hardware Settable/Clearable bit	
R = Readable bit	HS = Hardware Settable bit	U = Unimplemented bit, read as '0'	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15 **ACKSTAT:** Acknowledge Status bit (updated in all Master and Slave modes)
1 = Acknowledge was not received from slave
0 = Acknowledge was received from slave

bit 14 **TRSTAT:** Transmit Status bit (when operating as I^2C™ master; applicable to master transmit operation)
1 = Master transmit is in progress (8 bits + ACK)
0 = Master transmit is not in progress

bit 13 **ACKTIM:** Acknowledge Time Status bit (valid in I^2C Slave mode only)
1 = Indicates I^2C bus is in an Acknowledge sequence, set on 8th falling edge of SCLx clock
0 = Not an Acknowledge sequence, cleared on 9th rising edge of SCLx clock

bit 12-11 **Unimplemented:** Read as '0'

bit 10 **BCL:** Bus Collision Detect bit (Master/Slave mode; cleared when I^2C module is disabled, I2CEN = 0)
1 = A bus collision has been detected during a master or slave transmit operation
0 = No bus collision has been detected

bit 9 **GCSTAT:** General Call Status bit (cleared after Stop detection)
1 = General call address was received
0 = General call address was not received

bit 8 **ADD10:** 10-Bit Address Status bit (cleared after Stop detection)
1 = 10-bit address was matched
0 = 10-bit address was not matched

bit 7 **IWCOL:** I2Cx Write Collision Detect bit
1 = An attempt to write to the I2CxTRN register failed because the I^2C module is busy; must be cleared in software
0 = No collision

bit 6 **I2COV:** I2Cx Receive Overflow Flag bit
1 = A byte was received while the I2CxRCV register is still holding the previous byte; I2COV is a "don't care" in Transmit mode, must be cleared in software
0 = No overflow

bit 5 **D/$\overline{A}$:** Data/$\overline{\text{Address}}$ bit (when operating as I^2C slave)
1 = Indicates that the last byte received was data
0 = Indicates that the last byte received or transmitted was an address

bit 4 **P:** I2Cx Stop bit
Updated when Start, Reset or Stop is detected; cleared when the I^2C module is disabled, I2CEN = 0.
1 = Indicates that a Stop bit has been detected last
0 = Stop bit was not detected last

19.2 USB Buffer Descriptors and the BDT

Endpoint buffer control is handled through a structure called the Buffer Descriptor Table (BDT). This provides a flexible method for users to construct and control endpoint buffers of various lengths and configurations.

The BDT can be located in any available, 512-byte aligned block of data RAM. The BDT Pointer (U1BDTP1) contains the upper address byte of the BDT and sets the location of the BDT in RAM. The user must set this pointer to indicate the table's location.

The BDT is composed of Buffer Descriptors (BDs) which are used to define and control the actual buffers in the USB RAM space. Each BD consists of two, 16-bit "soft" (non-fixed address) registers, BDnSTAT and BDnADR, where n represents one of the 64 possible BDs (range of 0 to 63). BDnSTAT is the status register for BDn, while BDnADR specifies the starting address for the buffer associated with BDn.

Note:	Since BDnADR is a 16-bit register, only the first 64 Kbytes of RAM can be accessed by the USB module.

Depending on the endpoint buffering configuration used, there are up to 64 sets of Buffer Descriptors, for a total of 256 bytes. At a minimum, the BDT must be at least 8 bytes long. This is because the *"USB 2.0 Specification"* mandates that every device must have Endpoint 0 with both input and output for initial setup.

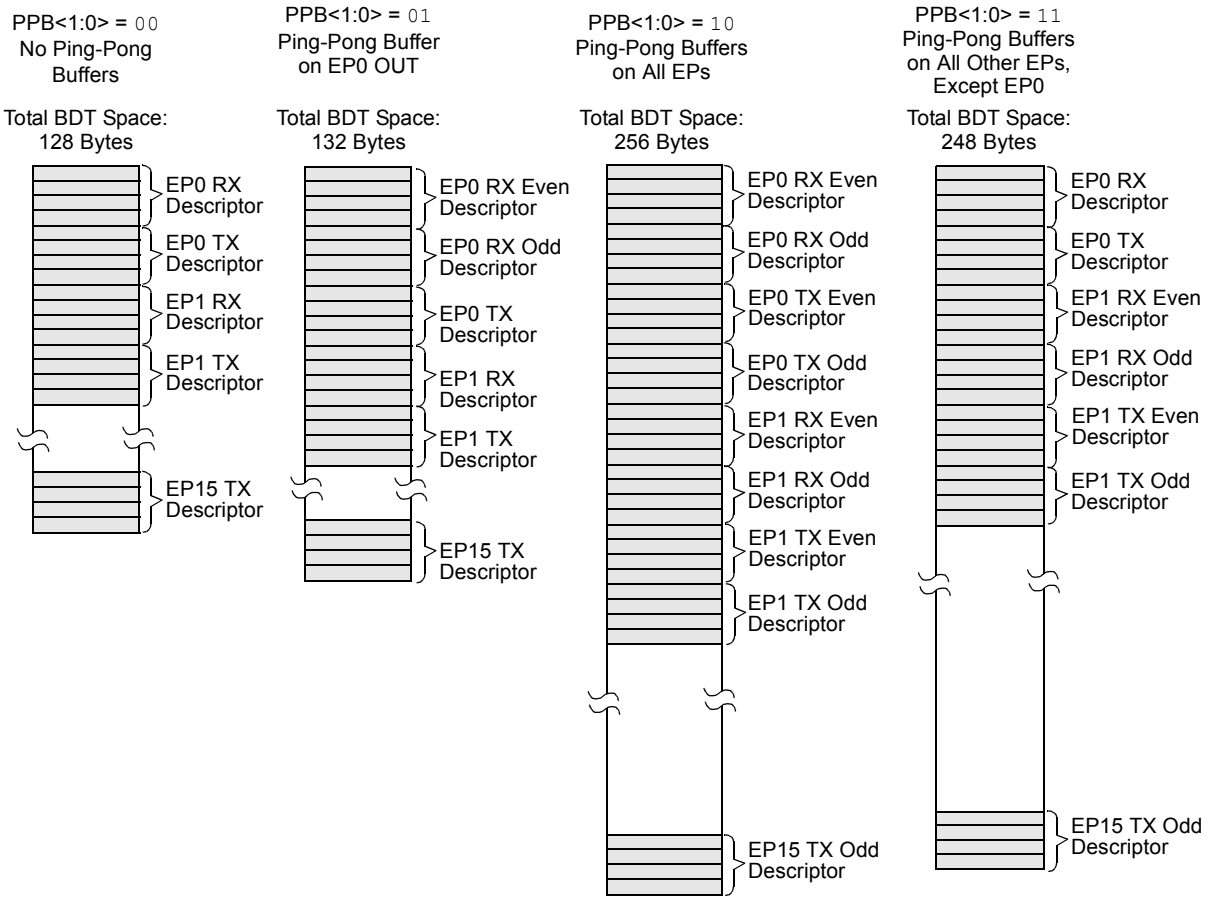
Endpoint mapping in the BDT is dependent on three variables:

- Endpoint number (0 to 15)
- Endpoint direction (RX or TX)
- Ping-pong settings (U1CNFG1<1:0>)

Figure 19-8 illustrates how these variables are used to map endpoints in the BDT.

In Host mode, only Endpoint 0 Buffer Descriptors are used. All transfers utilize the Endpoint 0 Buffer Descriptor and USB Endpoint Control register (U1EP0). For received packets, the attached device's source endpoint is indicated by the value of ENDPT<3:0> in the USB Status register (U1STAT<7:4>). For transmitted packets, the attached device's destination endpoint is indicated by the value written to the USB Token register (U1TOK).

FIGURE 19-8: BDT MAPPING FOR ENDPOINT BUFFERING MODES



Note: Memory area is not shown to scale.

REGISTER 19-7: U1CON: USB CONTROL REGISTER (DEVICE MODE)

U-0	U-0	U-0	U-0	U-0	U-0	U-0	U-0
—	—	—	—	—	—	—	—
bit 15							bit 8

U-0	R-x, HSC	R/W-0	U-0	R/W-0	R/W-0	R/W-0	R/W-0
—	SE0	PKTDIS	—	HOSTEN	RESUME	PPBRST	USBEN
bit 7							bit 0

Legend:	U = Unimplemented bit, read as '0'		
R = Readable bit	W = Writable bit	HSC = Hardware Settable/Clearable bit	
-n = Value at POR	'1' = Bit is set	'0' = Bit is cleared	x = Bit is unknown

bit 15-7 **Unimplemented:** Read as '0'

bit 6 **SE0:** Live Single-Ended Zero Flag bit
1 = Single-ended zero is active on the USB bus
0 = No single-ended zero is detected

bit 5 **PKTDIS:** Packet Transfer Disable bit
1 = SIE token and packet processing are disabled; automatically set when a SETUP token is received
0 = SIE token and packet processing are enabled

bit 4 **Unimplemented:** Read as '0'

bit 3 **HOSTEN:** Host Mode Enable bit
1 = USB host capability is enabled; pull-downs on D+ and D- are activated in hardware
0 = USB host capability is disabled

bit 2 **RESUME:** Resume Signaling Enable bit
1 = Resume signaling is activated
0 = Resume signaling is disabled

bit 1 **PPBRST:** Ping-Pong Buffers Reset bit
1 = Resets all Ping-Pong Buffer Pointers to the Even BD banks
0 = Ping-Pong Buffer Pointers are not reset

bit 0 **USBEN:** USB Module Enable bit
1 = USB module and supporting circuitry are enabled (device attached); D+ pull-up is activated in hardware
0 = USB module and supporting circuitry are disabled (device detached)

28.2 Measuring Time

Time measurements on the pulse width can be similarly performed using the A/D module's Internal Capacitor (CAD) and a precision resistor for current calibration. Figure 28-2 displays the external connections used for time measurements, and how the CTMU and A/D modules are related in this application. This example also shows both edge events coming from the external CTED pins, but other configurations using internal edge sources are possible.

28.3 Pulse Generation and Delay

The CTMU module can also generate an output pulse with edges that are not synchronous with the device's system clock. More specifically, it can generate a pulse with a programmable delay from an edge event input to the module.

When the module is configured for pulse generation delay by setting the TGEN bit (CTMUCON1<12>), the internal current source is connected to the B input of Comparator 2. A Capacitor (CDELAY) is connected to the Comparator 2 pin, C2INB, and the Comparator voltage Reference, CVREF, is connected to C2INA. CVREF is then configured for a specific trip point. The module begins to charge CDELAY when an edge event is detected. When CDELAY charges above the CVREF trip point, a pulse is output on CTPLS. The length of the pulse delay is determined by the value of CDELAY and the CVREF trip point.

Figure 28-3 illustrates the external connections for pulse generation, as well as the relationship of the different analog modules required. While CTED1 is shown as the input pulse source, other options are available. A detailed discussion on pulse generation with the CTMU module is provided in the *"dsPIC33/PIC24 Family Reference Manual"*.

FIGURE 28-2: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR TIME MEASUREMENT

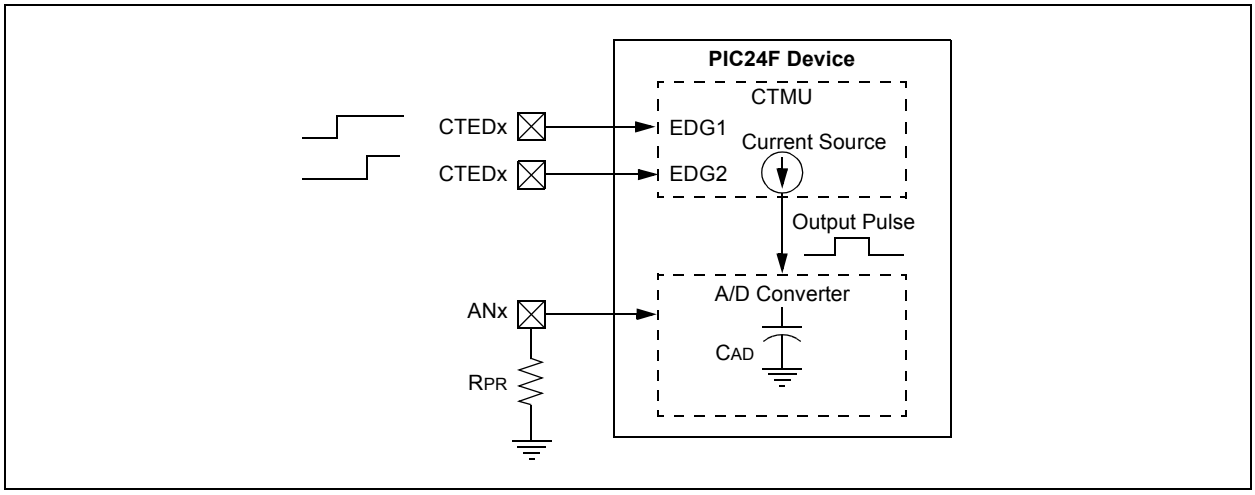
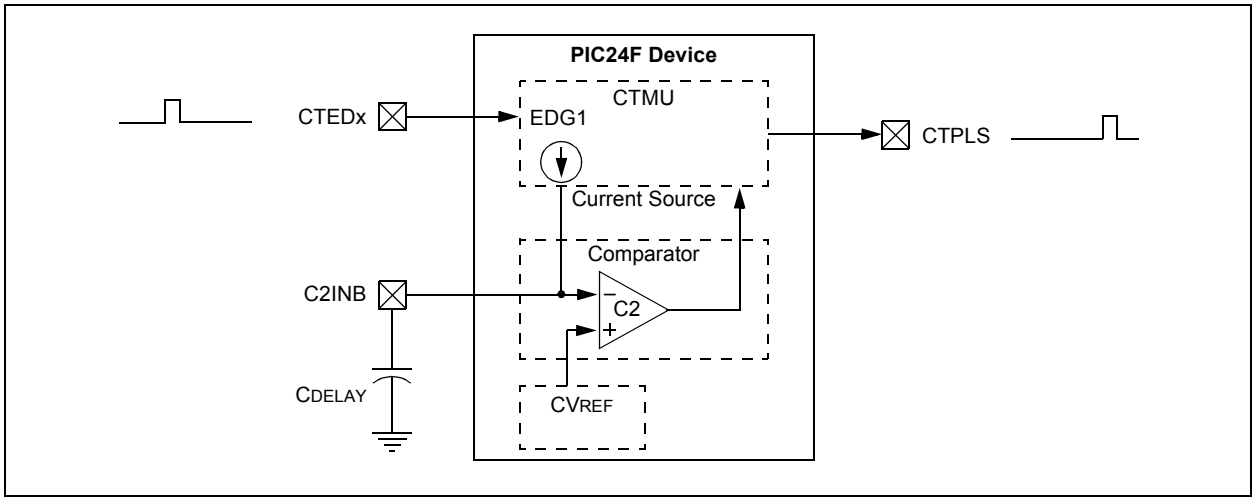


FIGURE 28-3: TYPICAL CONNECTIONS AND INTERNAL CONFIGURATION FOR PULSE DELAY GENERATION



29.0 HIGH/LOW-VOLTAGE DETECT (HLVD)

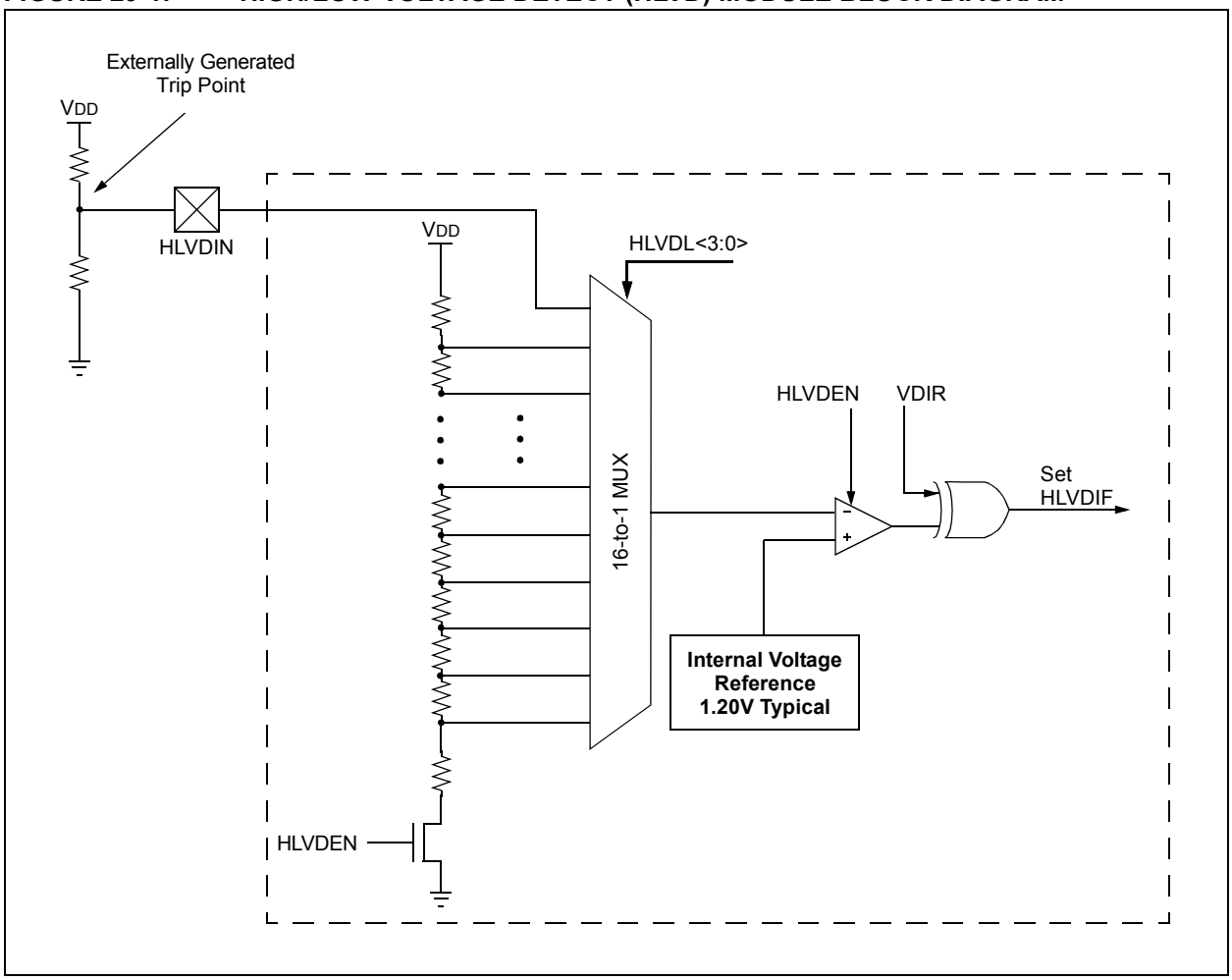
Note:	This data sheet summarizes the features of this group of PIC24F devices. It is not intended to be a comprehensive reference source. For more information on the High/Low-Voltage Detect, refer to the *"dsPIC33/PIC24 Family Reference Manual"*, **"High-Level Integration with Programmable High/Low-Voltage Detect (HLVD)"** (DS39725).

The High/Low-Voltage Detect (HLVD) module is a programmable circuit that allows the user to specify both the device voltage trip point and the direction of change.

An interrupt flag is set if the device experiences an excursion past the trip point in the direction of change. If the interrupt is enabled, the program execution will branch to the interrupt vector address and the software can then respond to the interrupt.

The HLVD Control register (see Register 29-1) completely controls the operation of the HLVD module. This allows the circuitry to be "turned off" by the user under software control, which minimizes the current consumption for the device.

FIGURE 29-1: HIGH/LOW-VOLTAGE DETECT (HLVD) MODULE BLOCK DIAGRAM



32.0 INSTRUCTION SET SUMMARY

Note: This chapter is a brief summary of the PIC24F Instruction Set Architecture (ISA) and is not intended to be a comprehensive reference source.

The PIC24F instruction set adds many enhancements to the previous PIC® MCU instruction sets, while maintaining an easy migration from previous PIC MCU instruction sets. Most instructions are a single program memory word. Only three instructions require two program memory locations.

Each single-word instruction is a 24-bit word divided into an 8-bit opcode, which specifies the instruction type and one or more operands, which further specify the operation of the instruction. The instruction set is highly orthogonal and is grouped into four basic categories:

- Word or byte-oriented operations
- Bit-oriented operations
- Literal operations
- Control operations

Table 32-1 shows the general symbols used in describing the instructions. The PIC24F instruction set summary in Table 32-2 lists all the instructions, along with the status flags affected by each instruction.

Most word or byte-oriented W register instructions (including barrel shift instructions) have three operands:

- The first source operand, which is typically a register, 'Wb', without any address modifier
- The second source operand, which is typically a register, 'Ws', with or without an address modifier
- The destination of the result, which is typically a register, 'Wd', with or without an address modifier

However, word or byte-oriented file register instructions have two operands:

- The file register specified by the value, 'f'
- The destination, which could either be the file register, 'f', or the W0 register, which is denoted as 'WREG'

Most bit-oriented instructions (including simple rotate/shift instructions) have two operands:

- The W register (with or without an address modifier) or file register (specified by the value of 'Ws' or 'f')
- The bit in the W register or file register (specified by a literal value or indirectly by the contents of register, 'Wb')

The literal instructions that involve data movement may use some of the following operands:

- A literal value to be loaded into a W register or file register (specified by the value of 'k')
- The W register or file register where the literal value is to be loaded (specified by 'Wb' or 'f')

However, literal instructions that involve arithmetic or logical operations use some of the following operands:

- The first source operand, which is a register, 'Wb', without any address modifier
- The second source operand, which is a literal value
- The destination of the result (only if not the same as the first source operand), which is typically a register, 'Wd', with or without an address modifier

The control instructions may use some of the following operands:

- A program memory address
- The mode of the Table Read and Table Write instructions

All instructions are a single word, except for certain double-word instructions, which were made double-word instructions so that all the required information is available in these 48 bits. In the second word, the 8 MSbs are '0's. If this second word is executed as an instruction (by itself), it will execute as a NOP.

Most single-word instructions are executed in a single instruction cycle, unless a conditional test is true or the Program Counter is changed as a result of the instruction. In these cases, the execution takes two instruction cycles, with the additional instruction cycle(s) executed as a NOP. Notable exceptions are the BRA (unconditional/computed branch), indirect CALL/GOTO, all Table Reads and Table Writes, and RETURN/RETFIE instructions, which are single-word instructions but take two or three cycles.

Certain instructions that involve skipping over the subsequent instruction require either two or three cycles if the skip is performed, depending on whether the instruction being skipped is a single-word or two-word instruction. Moreover, double-word moves require two cycles. The double-word instructions execute in two instruction cycles.