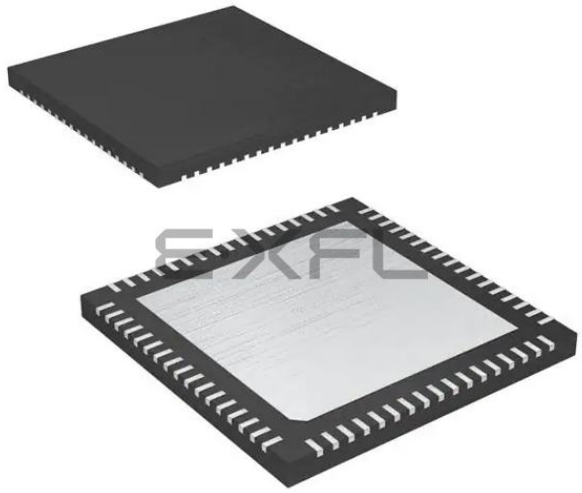

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | - |
| Number of I/O | 49 |
| Number of Gates | 30000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 68-VFQFN Exposed Pad |
| Supplier Device Package | 68-QFN (8x8) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p030-1qng68 |

### I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

***Table 1-1 •*** **I/O Standards Supported**

| I/O Bank Type | Device and Bank Location | I/O Standards Supported | | |
|---|---|---|---|---|
| | | LVTTL/ LVCMOS | PCI/PCI-X | LVPECL, LVDS, B-LVDS, M-LVDS |
| Advanced | East and west Banks of A3P250 and larger devices | ✓ | ✓ | ✓ |
| Standard Plus | North and south banks of A3P250 and larger devices<br>All banks of A3P060 and A3P125 | ✓ | ✓ | Not supported |
| Standard | All banks of A3P015 and A3P030 | ✓ | Not supported | Not supported |

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

### Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

## Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

**Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks**

| | $C_{LOAD}$ (pF) | VCCI (V) | Static Power PDC3 (mW)[2] | Dynamic Power PAC10 (µW/MHz)[3] |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 468.67 |
| 3.3 V LVCMOS Wide Range[4] | 35 | 3.3 | – | 468.67 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 267.48 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 149.46 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 103.12 |
| 3.3 V PCI | 10 | 3.3 | – | 201.02 |
| 3.3 V PCI-X | 10 | 3.3 | – | 201.02 |
| **Differential** | | | | |
| LVDS | – | 2.5 | 7.74 | 88.92 |
| LVPECL | – | 3.3 | 19.54 | 166.52 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

**Table 2-12 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1] Applicable to Standard Plus I/O Banks**

| | $C_{LOAD}$ (pF) | VCCI (V) | Static Power PDC3 (mW)[2] | Dynamic Power PAC10 (µW/MHz)[3] |
|---|---|---|---|---|
| **Single-Ended** | | | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 35 | 3.3 | – | 452.67 |
| 3.3 V LVCMOS Wide Range[4] | 35 | 3.3 | – | 452.67 |
| 2.5 V LVCMOS | 35 | 2.5 | – | 258.32 |
| 1.8 V LVCMOS | 35 | 1.8 | – | 133.59 |
| 1.5 V LVCMOS (JESD8-11) | 35 | 1.5 | – | 92.84 |
| 3.3 V PCI | 10 | 3.3 | – | 184.92 |
| 3.3 V PCI-X | 10 | 3.3 | – | 184.92 |

*Notes:*

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *$P_{DC3}$ is the static power (where applicable) measured on VMV.*
3. *$P_{AC10}$ is the total dynamic power measured on VCC and VMV.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

**Table 2-29 • I/O Output Buffer Maximum Resistances [1]**
**Applicable to Standard Plus I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 25 | 75 |
| 3.3 V LVCMOS Wide Range[4] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

**Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

**Table 2-66 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA[3] | Max mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

**Table 2-67 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA[3] | Max mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 8 | 8 | 44 | 35 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

**Table 2-93 • Minimum and Maximum DC Input and Output Levels**

| DC Parameter | Description | Min. | Max. | Min. | Max. | Min. | Max. | Units |
|---|---|---|---|---|---|---|---|---|
| VCCI | Supply Voltage | 3.0 | | 3.3 | | 3.6 | | V |
| VOL | Output Low Voltage | 0.96 | 1.27 | 1.06 | 1.43 | 1.30 | 1.57 | V |
| VOH | Output High Voltage | 1.8 | 2.11 | 1.92 | 2.28 | 2.13 | 2.41 | V |
| VIL, VIH | Input Low, Input High Voltages | 0 | 3.6 | 0 | 3.6 | 0 | 3.6 | V |
| VODIFF | Differential Output Voltage | 0.625 | 0.97 | 0.625 | 0.97 | 0.625 | 0.97 | V |
| VOCM | Output Common-Mode Voltage | 1.762 | 1.98 | 1.762 | 1.98 | 1.762 | 1.98 | V |
| VICM | Input Common-Mode Voltage | 1.01 | 2.57 | 1.01 | 2.57 | 1.01 | 2.57 | V |
| VIDIFF | Input Differential Voltage | 300 | | 300 | | 300 | | mV |

**Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads**

| Input Low (V) | Input High (V) | Measuring Point* (V) |
|---|---|---|
| 1.64 | 1.94 | Cross point |

*Note: *Measuring point = $V_{trip}$. See Table 2-22 on page 2-22 for a complete table of trip points.*

## Timing Characteristics

**Table 2-95 • LVPECL**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | Units |
|---|---|---|---|---|---|
| Std. | 0.66 | 1.80 | 0.04 | 1.40 | ns |
| –1 | 0.56 | 1.53 | 0.04 | 1.19 | ns |
| –2 | 0.49 | 1.34 | 0.03 | 1.05 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

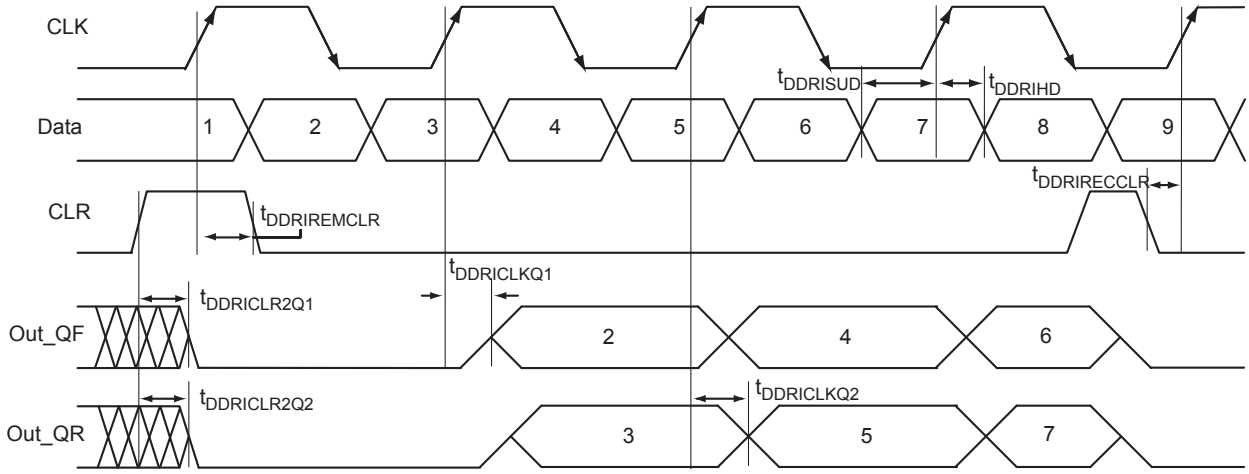



***Figure 2-21 •*** **Input DDR Timing Diagram**

## *Timing Characteristics*

***Table 2-102 •*** **Input DDR Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{DDRICLKQ1}$ | Clock-to-Out Out_QR for Input DDR | 0.27 | 0.31 | 0.37 | ns |
| $t_{DDRICLKQ2}$ | Clock-to-Out Out_QF for Input DDR | 0.39 | 0.44 | 0.52 | ns |
| $t_{DDRISUD}$ | Data Setup for Input DDR (Fall) | 0.25 | 0.28 | 0.33 | ns |
| | Data Setup for Input DDR (Rise) | 0.25 | 0.28 | 0.33 | ns |
| $t_{DDRIHD}$ | Data Hold for Input DDR (Fall) | 0.00 | 0.00 | 0.00 | ns |
| | Data Hold for Input DDR (Rise) | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDRICLR2Q1}$ | Asynchronous Clear-to-Out Out_QR for Input DDR | 0.46 | 0.53 | 0.62 | ns |
| $t_{DDRICLR2Q2}$ | Asynchronous Clear-to-Out Out_QF for Input DDR | 0.57 | 0.65 | 0.76 | ns |
| $t_{DDRIREMCLR}$ | Asynchronous Clear Removal time for Input DDR | 0.00 | 0.00 | 0.00 | ns |
| $t_{DDRIRECCLR}$ | Asynchronous Clear Recovery time for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDRIWCLR}$ | Asynchronous Clear Minimum Pulse Width for Input DDR | 0.22 | 0.25 | 0.30 | ns |
| $t_{DDRICKMPWH}$ | Clock Minimum Pulse Width High for Input DDR | 0.36 | 0.41 | 0.48 | ns |
| $t_{DDRICKMPWL}$ | Clock Minimum Pulse Width Low for Input DDR | 0.32 | 0.37 | 0.43 | ns |
| $F_{DDRIMAX}$ | Maximum Frequency for Input DDR | 350 | 309 | 263 | MHz |

*Note: For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Characteristics

**Table 2-105 • Combinatorial Cell Propagation Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Combinatorial Cell | Equation | Parameter | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|---|
| INV | Y = !A | $t_{PD}$ | 0.40 | 0.46 | 0.54 | ns |
| AND2 | Y = A · B | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| NAND2 | Y = !(A · B) | $t_{PD}$ | 0.47 | 0.54 | 0.63 | ns |
| OR2 | Y = A + B | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| NOR2 | Y = !(A + B) | $t_{PD}$ | 0.49 | 0.55 | 0.65 | ns |
| XOR2 | Y = A ⊕ B | $t_{PD}$ | 0.74 | 0.84 | 0.99 | ns |
| MAJ3 | Y = MAJ(A, B, C) | $t_{PD}$ | 0.70 | 0.79 | 0.93 | ns |
| XOR3 | Y = A ⊕ B ⊕ C | $t_{PD}$ | 0.87 | 1.00 | 1.17 | ns |
| MUX2 | Y = A !S + B S | $t_{PD}$ | 0.51 | 0.58 | 0.68 | ns |
| AND3 | Y = A · B · C | $t_{PD}$ | 0.56 | 0.64 | 0.75 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

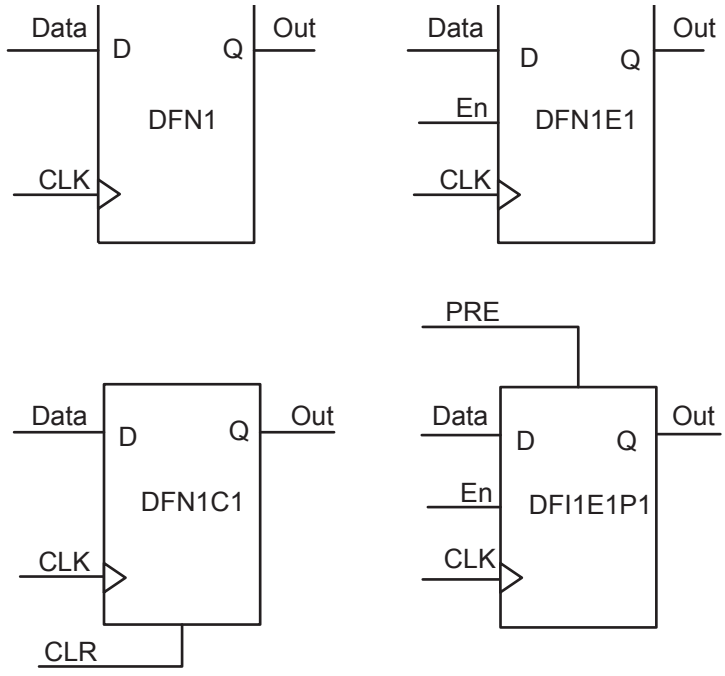



**Figure 2-26 • Sample of Sequential Cells**

## Timing Characteristics

***Table 2-107* • A3P015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.66 | 0.81 | 0.75 | 0.92 | 0.88 | 1.08 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.67 | 0.84 | 0.76 | 0.96 | 0.89 | 1.13 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.25 | ns |

***Notes:***

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-108* • A3P030 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.67 | 0.81 | 0.76 | 0.92 | 0.89 | 1.09 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.68 | 0.85 | 0.77 | 0.97 | 0.91 | 1.14 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.24 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-117 • RAM512X18**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.13 | 0.15 | 0.17 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{DS}$ | Input data (WD) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (WD) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on RD (output retained) | 2.16 | 2.46 | 2.89 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on RD (pipelined) | 0.90 | 1.02 | 1.20 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.50 | 0.43 | 0.38 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge | 0.59 | 0.50 | 0.44 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to data out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-119* • FIFO (for A3P250 only, aspect-ratio-dependent)**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 3.26 | 3.71 | 4.36 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

mode is not used in the design, the FF pin is available as a regular I/O. For IGLOOe, ProASIC3EL, and RT ProASIC3 only, the FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

# JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

### TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 1 for more information.

***Table 1 •*** **Recommended Tie-Off Values for the TCK and TRST Pins**

| VJTAG | Tie-Off Resistance |
|---|---|
| 3.3 V | 200 Ω –1 kΩ |
| 2.5 V | 200 Ω –1 kΩ |
| 1.8 V | 500 Ω –1 kΩ |
| 1.5 V | 500 Ω –1 kΩ |

*Notes:*

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

### TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

### TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

### TMS Test Mode Select

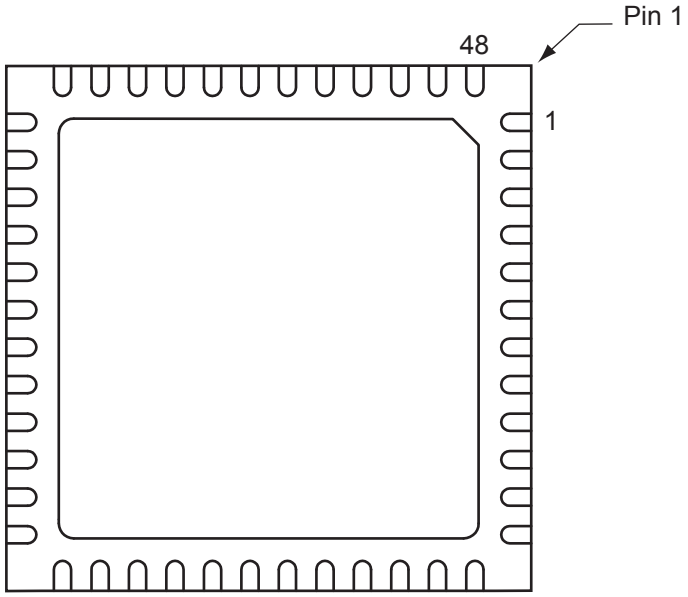
The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

### TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 1 and must satisfy the parallel resistance value requirement. The values in Table 1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

# 4 – Package Pin Assignments

## QN48 – Bottom View




*Note: The die attach paddle center of the package is tied to ground (GND).*

### Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

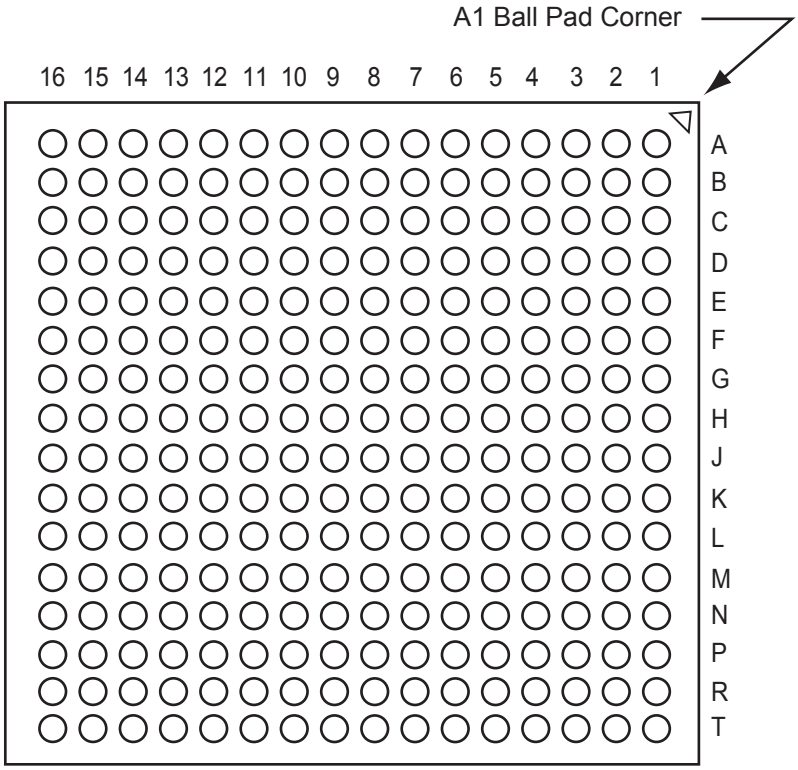
| QN132 | |
|---|---|
| Pin Number | A3P060 Function |
| A1 | GAB2/IO00RSB1 |
| A2 | IO93RSB1 |
| A3 | VCCIB1 |
| A4 | GFC1/IO89RSB1 |
| A5 | GFB0/IO86RSB1 |
| A6 | VCCPLF |
| A7 | GFA1/IO84RSB1 |
| A8 | GFC2/IO81RSB1 |
| A9 | IO78RSB1 |
| A10 | VCC |
| A11 | GEB1/IO75RSB1 |
| A12 | GEA0/IO72RSB1 |
| A13 | GEC2/IO69RSB1 |
| A14 | IO65RSB1 |
| A15 | VCC |
| A16 | IO64RSB1 |
| A17 | IO63RSB1 |
| A18 | IO62RSB1 |
| A19 | IO61RSB1 |
| A20 | IO58RSB1 |
| A21 | GDB2/IO55RSB1 |
| A22 | NC |
| A23 | GDA2/IO54RSB1 |
| A24 | TDI |
| A25 | TRST |
| A26 | GDC1/IO48RSB0 |
| A27 | VCC |
| A28 | IO47RSB0 |
| A29 | GCC2/IO46RSB0 |
| A30 | GCA2/IO44RSB0 |
| A31 | GCA0/IO43RSB0 |
| A32 | GCB1/IO40RSB0 |
| A33 | IO36RSB0 |
| A34 | VCC |
| A35 | IO31RSB0 |
| A36 | GBA2/IO28RSB0 |

| QN132 | |
|---|---|
| Pin Number | A3P060 Function |
| A37 | GBB1/IO25RSB0 |
| A38 | GBC0/IO22RSB0 |
| A39 | VCCIB0 |
| A40 | IO21RSB0 |
| A41 | IO18RSB0 |
| A42 | IO15RSB0 |
| A43 | IO14RSB0 |
| A44 | IO11RSB0 |
| A45 | GAB1/IO08RSB0 |
| A46 | NC |
| A47 | GAB0/IO07RSB0 |
| A48 | IO04RSB0 |
| B1 | IO01RSB1 |
| B2 | GAC2/IO94RSB1 |
| B3 | GND |
| B4 | GFC0/IO88RSB1 |
| B5 | VCOMPLF |
| B6 | GND |
| B7 | GFB2/IO82RSB1 |
| B8 | IO79RSB1 |
| B9 | GND |
| B10 | GEB0/IO74RSB1 |
| B11 | VMV1 |
| B12 | GEB2/IO70RSB1 |
| B13 | IO67RSB1 |
| B14 | GND |
| B15 | NC |
| B16 | NC |
| B17 | GND |
| B18 | IO59RSB1 |
| B19 | GDC2/IO56RSB1 |
| B20 | GND |
| B21 | GNDQ |
| B22 | TMS |
| B23 | TDO |
| B24 | GDC0/IO49RSB0 |

| QN132 | |
|---|---|
| Pin Number | A3P060 Function |
| B25 | GND |
| B26 | NC |
| B27 | GCB2/IO45RSB0 |
| B28 | GND |
| B29 | GCB0/IO41RSB0 |
| B30 | GCC1/IO38RSB0 |
| B31 | GND |
| B32 | GBB2/IO30RSB0 |
| B33 | VMV0 |
| B34 | GBA0/IO26RSB0 |
| B35 | GBC1/IO23RSB0 |
| B36 | GND |
| B37 | IO20RSB0 |
| B38 | IO17RSB0 |
| B39 | GND |
| B40 | IO12RSB0 |
| B41 | GAC0/IO09RSB0 |
| B42 | GND |
| B43 | GAA1/IO06RSB0 |
| B44 | GNDQ |
| C1 | GAA2/IO02RSB1 |
| C2 | IO95RSB1 |
| C3 | VCC |
| C4 | GFB1/IO87RSB1 |
| C5 | GFA0/IO85RSB1 |
| C6 | GFA2/IO83RSB1 |
| C7 | IO80RSB1 |
| C8 | VCCIB1 |
| C9 | GEA1/IO73RSB1 |
| C10 | GNDQ |
| C11 | GEA2/IO71RSB1 |
| C12 | IO68RSB1 |
| C13 | VCCIB1 |
| C14 | NC |
| C15 | NC |
| C16 | IO60RSB1 |

| TQ144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| 109 | NC |
| 110 | NC |
| 111 | GBA1/IO24RSB0 |
| 112 | GBA0/IO23RSB0 |
| 113 | GBB1/IO22RSB0 |
| 114 | GBB0/IO21RSB0 |
| 115 | GBC1/IO20RSB0 |
| 116 | GBC0/IO19RSB0 |
| 117 | VCCIB0 |
| 118 | GND |
| 119 | VCC |
| 120 | IO18RSB0 |
| 121 | IO17RSB0 |
| 122 | IO16RSB0 |
| 123 | IO15RSB0 |
| 124 | IO14RSB0 |
| 125 | IO13RSB0 |
| 126 | IO12RSB0 |
| 127 | IO11RSB0 |
| 128 | NC |
| 129 | IO10RSB0 |
| 130 | IO09RSB0 |
| 131 | IO08RSB0 |
| 132 | GAC1/IO07RSB0 |
| 133 | GAC0/IO06RSB0 |
| 134 | NC |
| 135 | GND |
| 136 | NC |
| 137 | GAB1/IO05RSB0 |
| 138 | GAB0/IO04RSB0 |
| 139 | GAA1/IO03RSB0 |
| 140 | GAA0/IO02RSB0 |
| 141 | IO01RSB0 |
| 142 | IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

# FG256 – Bottom View




## Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO16RSB0 |
| A6 | IO22RSB0 |
| A7 | IO28RSB0 |
| A8 | IO35RSB0 |
| A9 | IO45RSB0 |
| A10 | IO50RSB0 |
| A11 | IO55RSB0 |
| A12 | IO61RSB0 |
| A13 | GBB1/IO75RSB0 |
| A14 | GBA0/IO76RSB0 |
| A15 | GBA1/IO77RSB0 |
| A16 | GND |
| B1 | GAB2/IO224PDB3 |
| B2 | GAA2/IO225PDB3 |
| B3 | GNDQ |
| B4 | GAB1/IO03RSB0 |
| B5 | IO17RSB0 |
| B6 | IO21RSB0 |
| B7 | IO27RSB0 |
| B8 | IO34RSB0 |
| B9 | IO44RSB0 |
| B10 | IO51RSB0 |
| B11 | IO57RSB0 |
| B12 | GBC1/IO73RSB0 |
| B13 | GBB0/IO74RSB0 |
| B14 | IO71RSB0 |
| B15 | GBA2/IO78PDB1 |
| B16 | IO81PDB1 |
| C1 | IO224NDB3 |
| C2 | IO225NDB3 |
| C3 | VMV3 |
| C4 | IO11RSB0 |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| C7 | IO25RSB0 |
| C8 | IO36RSB0 |
| C9 | IO42RSB0 |
| C10 | IO49RSB0 |
| C11 | IO56RSB0 |
| C12 | GBC0/IO72RSB0 |
| C13 | IO62RSB0 |
| C14 | VMV0 |
| C15 | IO78NDB1 |
| C16 | IO81NDB1 |
| D1 | IO222NDB3 |
| D2 | IO222PDB3 |
| D3 | GAC2/IO223PDB3 |
| D4 | IO223NDB3 |
| D5 | GNDQ |
| D6 | IO23RSB0 |
| D7 | IO29RSB0 |
| D8 | IO33RSB0 |
| D9 | IO46RSB0 |
| D10 | IO52RSB0 |
| D11 | IO60RSB0 |
| D12 | GNDQ |
| D13 | IO80NDB1 |
| D14 | GBB2/IO79PDB1 |
| D15 | IO79NDB1 |
| D16 | IO82NSB1 |
| E1 | IO217PDB3 |
| E2 | IO218PDB3 |
| E3 | IO221NDB3 |
| E4 | IO221PDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO38RSB0 |
| E9 | IO47RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| E13 | GBC2/IO80PDB1 |
| E14 | IO83PPB1 |
| E15 | IO86PPB1 |
| E16 | IO87PDB1 |
| F1 | IO217NDB3 |
| F2 | IO218NDB3 |
| F3 | IO216PDB3 |
| F4 | IO216NDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO83NPB1 |
| F14 | IO86NPB1 |
| F15 | IO90PPB1 |
| F16 | IO87NDB1 |
| G1 | IO210PSB3 |
| G2 | IO213NDB3 |
| G3 | IO213PDB3 |
| G4 | GFC1/IO209PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |
| G13 | GCC1/IO91PPB1 |
| G14 | IO90NPB1 |
| G15 | IO88PDB1 |
| G16 | IO88NDB1 |
| H1 | GFB0/IO208NPB3 |
| H2 | GFA0/IO207NDB3 |

| Revision | Changes | Page |
|---|---|---|
| **Revision 5 (Aug 2008)**<br>DC and Switching Characteristics v1.3 | TJ, Maximum Junction Temperature, was changed to 100° from 110º in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W. | 2-6 |
| | Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics. | 2-7 |
| | Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. $P_{AC14}$ was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new. | 2-11, 2-12 |
| | The "PLL Contribution—PPLL" section was updated to change the $P_{PLL}$ formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$. | 2-14 |
| | Both fall and rise values were included for $t_{DDRISUD}$ and $t_{DDRIHD}$ in Table 2-102 • Input DDR Propagation Delays. | 2-78 |
| | Table 2-107 • A3P015 Global Resource is new. | 2-86 |
| | The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification. | 2-90 |
| **Revision 4 (Jun 2008)**<br>DC and Switching Characteristics v1.2 | Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed. | 2-2 |
| | The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os." | 2-3 |
| | The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power. | 2-7 |
| | Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X. | 2-27 |
| | Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated. | 2-66 |
| **Revision 3 (Jun 2008)**<br>Packaging v1.3 | Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram. | 4-3 |
| | The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new. | 4-6 |
| **Revision 2 (Feb 2008)**<br>Product Brief v1.0 | This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview. | N/A |
| | This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated:<br>"Features and Benefits"<br>"ProASIC3 Ordering Information"<br>"Temperature Grade Offerings"<br>"ProASIC3 Flash Family FPGAs"<br>"A3P015 and A3P030" note<br>Introduction and Overview (NA) | N/A |

| Revision | Changes | Page |
|---|---|---|
| **Revision 2 (cont'd)** | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | III |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | IV |
| | In the General Description section the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68 – Bottom View" section is new. | 4-3 |
| **Revision 1 (Feb 2008)**<br>DC and Switching Characteristics v1.1 | In Table 2-2 • Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$. | 2-2 |
| | In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | In the "PLL Contribution—PPLL" section, the following was deleted:<br>FCLKIN is the input clock frequency. | 2-14 |
| | In Table 2-21 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$. | 2-21 |
| | In Table 2-115 • ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new. | 2-90 |
| | Table 2-125 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-108 |
| Packaging v1.1 | In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 4-19 |
| **Revision 0 (Jan 2008)** | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. | N/A |
| v2.2<br>(July 2007) | The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |
| v2.1<br>(May 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii |
| | Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.2, (continued) | Table 2-43 was updated. | 2-64 |
| | Table 2-18 was updated. | 2-45 |
| | Pin descriptions in the "JTAG Pins" section were updated. | 2-51 |
| | The "User I/O Naming Convention" section was updated. | 2-48 |
| | Table 3-7 was updated. | 3-6 |
| | The "Methodology" section was updated. | 3-10 |
| | Table 3-40 and Table 3-39 were updated. | 3-33,3-32 |
| | The A3P250 "100-Pin VQFP*" pin table was updated. | 4-14 |
| | The A3P250 "208-Pin PQFP*" pin table was updated. | 4-23 |
| | The A3P1000 "208-Pin PQFP*" pin table was updated. | 4-29 |
| | The A3P250 "144-Pin FBGA*" pin table was updated. | 4-36 |
| | The A3P1000 "144-Pin FBGA*" pin table was updated. | 4-32 |
| | The A3P250 "256-Pin FBGA*" pin table was updated. | 4-45 |
| | The A3P1000 "256-Pin FBGA*" pin table was updated. | 4-54 |
| | The A3P1000 "484-Pin FBGA*" pin table was updated. | 4-68 |