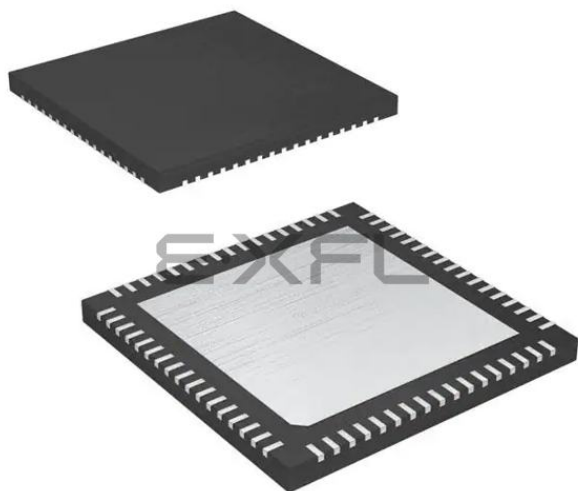




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	49
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	68-VFQFN Exposed Pad
Supplier Device Package	68-QFN (8x8)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p030-1qng68i

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Typical (25°C)	2 mA	2 mA	2 mA	2 mA	3 mA	3 mA	5 mA	8 mA
Max. (Commercial)	10 mA	10 mA	10 mA	10 mA	20 mA	20 mA	30 mA	50 mA
Max. (Industrial)	15 mA	15 mA	15 mA	15 mA	30 mA	30 mA	45 mA	75 mA

Note: I_{DD} Includes V_{CC} , V_{PUMP} , V_{CCI} , and V_{MV} currents. Values do not include I/O static contribution, which is shown in [Table 2-11](#) and [Table 2-12](#) on page 2-9.

Power per I/O Pin

**Table 2-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power $PAC9$ (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.22
3.3 V LVCMOS Wide Range ³	3.3	–	16.22
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. $PAC9$ is the total dynamic power measured on V_{CC} and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

**Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power $PAC9$ (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.23
3.3 V LVCMOS Wide Range ³	3.3	–	16.23

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. $PAC9$ is the total dynamic power measured on V_{CC} and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-13 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings ¹
Applicable to Standard I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	431.08
3.3 V LVCMOS Wide Range ⁴	35	3.3	–	431.08
2.5 V LVCMOS	35	2.5	–	247.36
1.8 V LVCMOS	35	1.8	–	128.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	89.46

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on VCCI.
3. P_{AC10} is the total dynamic power measured on VCC and VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min	Max	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, $f = 1.0$ MHz	–	8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, $f = 1.0$ MHz	–	8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN} (\Omega)^2$	$R_{PULL-UP} (\Omega)^3$
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

3.3 V LVC MOS Wide Range

Table 2-47 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVC MOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
		Min V	Max V	Min V	Max V	Max V	Min V	μA	μA	Max mA ⁴	Max mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	132	127	10	10
100 μA	24 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	268	181	10	10

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 85°C junction temperature.
5. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.
6. Software default selection highlighted in gray.

Table 2-48 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

3.3 V LVC MOS Wide Range	Equiv. Software Default Drive Strength Option ¹	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
		Min V	Max V	Min V	Max V	Max V	Min V	μA	μA	Max mA ⁴	Max mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	12 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10
100 μA	16 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	103	109	10	10

Notes:

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 85°C junction temperature.
5. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.
6. Software default selection highlighted in gray.

Table 2-49 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ²	IIH ³
Drive Strength	Drive Strength Option ¹	Min V	Max V	Min V	Max V	Max V	Min V	μA	μA	Max mA ⁴	Max mA ⁴	μA ⁵	μA ⁵
100 μA	2 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	4 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	25	27	10	10
100 μA	6 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10
100 μA	8 mA	−0.3	0.8	2	3.6	0.2	VDD − 0.2	100	100	51	54	10	10

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where −0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 85°C junction temperature.
5. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
6. Software default selection highlighted in gray.

Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	11.14	0.04	1.52	0.43	11.14	9.54	3.51	3.61	14.53	12.94	ns
		–1	0.51	9.48	0.04	1.29	0.36	9.48	8.12	2.99	3.07	12.36	11.00	ns
		–2	0.45	8.32	0.03	1.14	0.32	8.32	7.13	2.62	2.70	10.85	9.66	ns
100 μA	4 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 μA	6 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 μA	8 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
100 μA	16 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-77 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-78 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

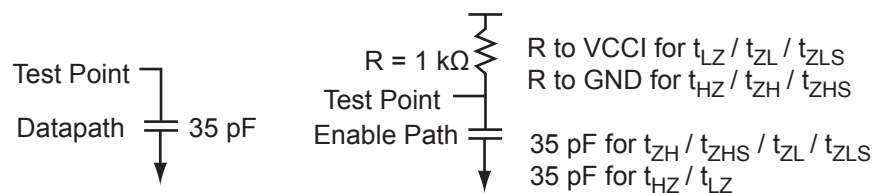


Figure 2-10 • AC Loading

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-22 for a complete table of trip points.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-86 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in [Figure 2-11](#).

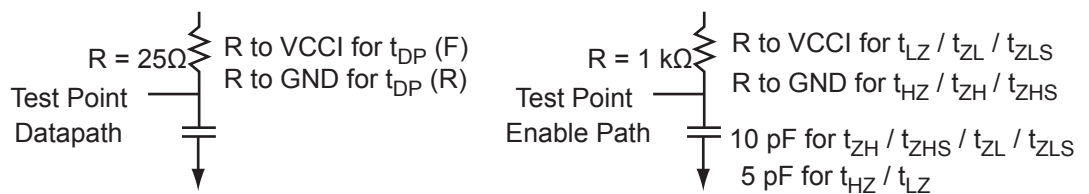


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in [Table 2-87](#).

Table 2-87 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	0.285 * V _{CCI} for $t_{DP}(R)$ 0.615 * V _{CCI} for $t_{DP}(F)$	10

Note: *Measuring point = V_{trip} . See [Table 2-22 on page 2-22](#) for a complete table of trip points.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

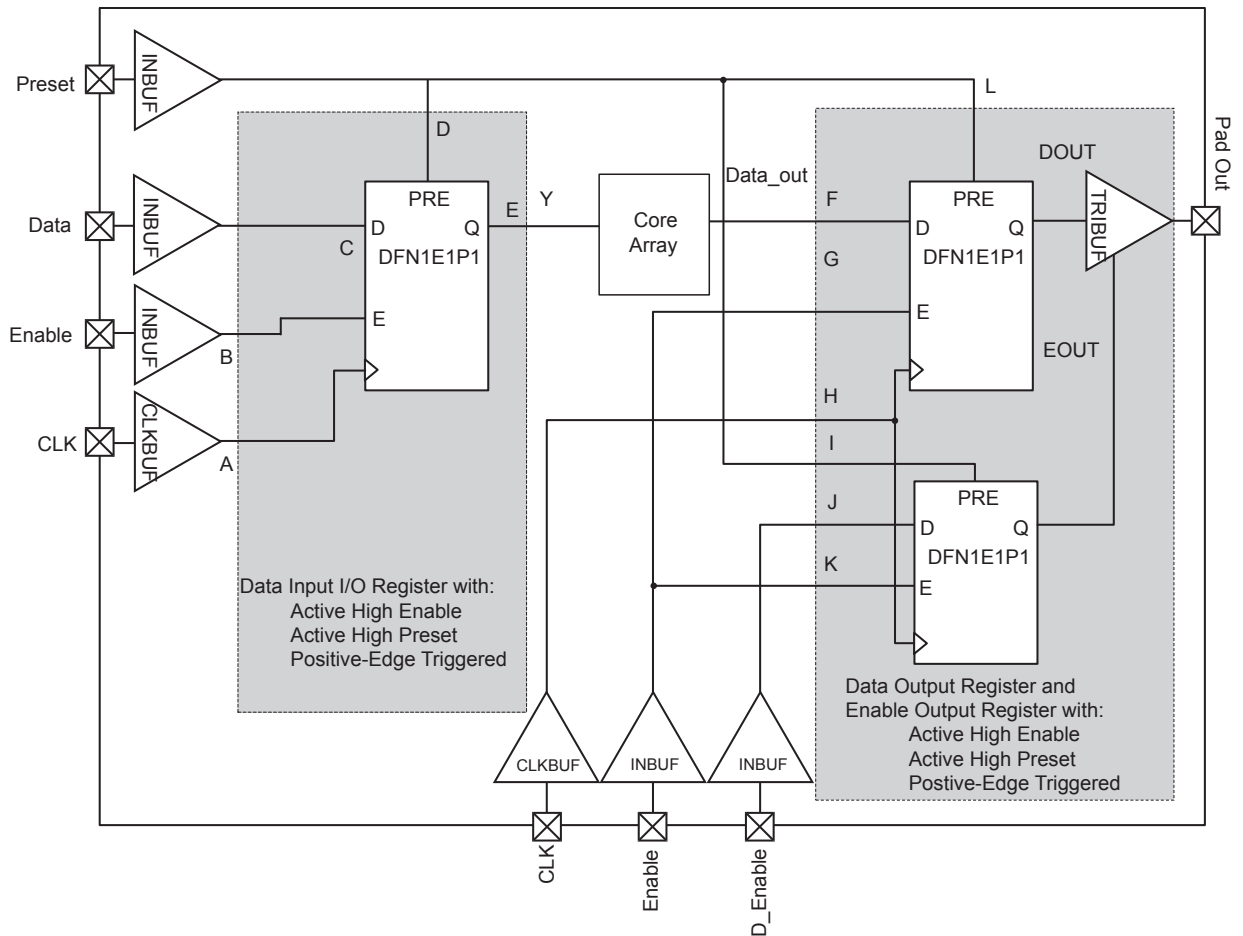


Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Output DDR Module

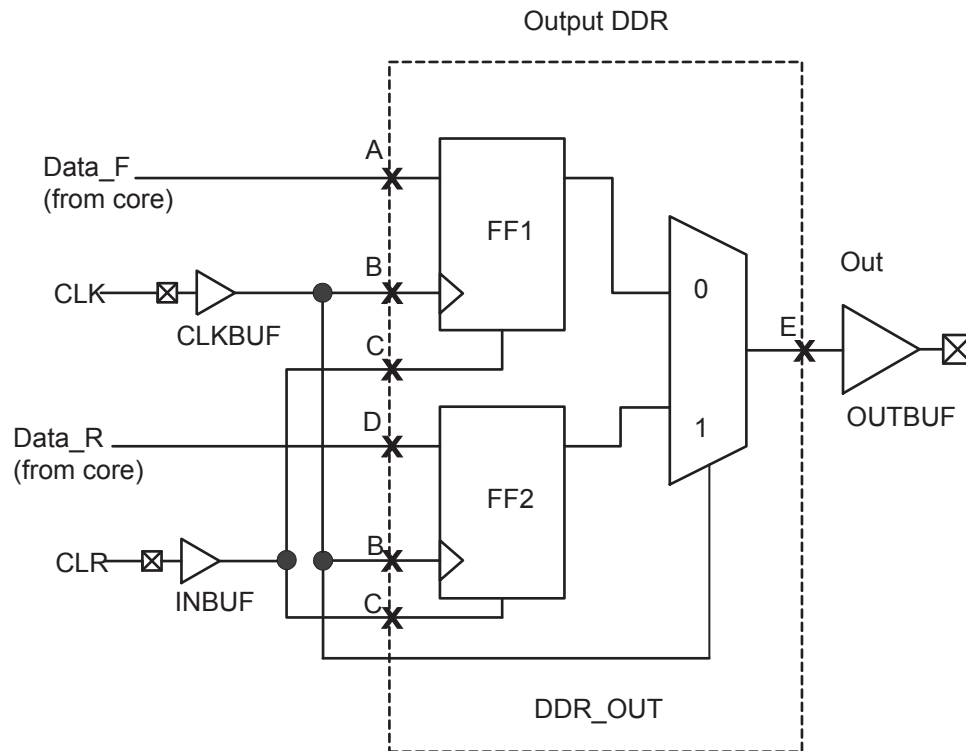


Figure 2-22 • Output DDR Timing Model

Table 2-103 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDROCLKQ}	Clock-to-Out	B, E
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out	C, E
$t_{\text{DDROREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRORECCLR}}$	Clear Recovery	C, B
t_{DDROSUD1}	Data Setup Data_F	A, B
t_{DDROSUD2}	Data Setup Data_R	D, B
t_{DDROHD1}	Data Hold Data_F	A, B
t_{DDROHD2}	Data Hold Data_R	D, B

Table 2-117 • RAM512X18**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$**

Parameter	Description	-2	-1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.13	0.15	0.17	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}^1	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}^1	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-119 • FIFO (for A3P250 only, aspect-ratio-dependent)
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.26	3.71	4.36	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

QN68	
Pin Number	A3P030 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	A3P030 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132	
Pin Number	A3P125 Function
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

CS121		CS121		CS121	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
A1	GNDQ	D4	IO10RSB0	G7	VCC
A2	IO01RSB0	D5	IO11RSB0	G8	GDC0/IO46RSB0
A3	GAA1/IO03RSB0	D6	IO18RSB0	G9	GDA1/IO49RSB0
A4	GAC1/IO07RSB0	D7	IO32RSB0	G10	GDB0/IO48RSB0
A5	IO15RSB0	D8	IO31RSB0	G11	GCA0/IO40RSB0
A6	IO13RSB0	D9	GCA2/IO41RSB0	H1	IO75RSB1
A7	IO17RSB0	D10	IO30RSB0	H2	IO76RSB1
A8	GBB1/IO22RSB0	D11	IO33RSB0	H3	GFC2/IO78RSB1
A9	GBA1/IO24RSB0	E1	IO87RSB1	H4	GFA2/IO80RSB1
A10	GNDQ	E2	GFC0/IO85RSB1	H5	IO77RSB1
A11	VMV0	E3	IO92RSB1	H6	GEC2/IO66RSB1
B1	GAA2/IO95RSB1	E4	IO94RSB1	H7	IO54RSB1
B2	IO00RSB0	E5	VCC	H8	GDC2/IO53RSB1
B3	GAA0/IO02RSB0	E6	VCCIB0	H9	VJTAG
B4	GAC0/IO06RSB0	E7	GND	H10	TRST
B5	IO08RSB0	E8	GCC0/IO36RSB0	H11	IO44RSB0
B6	IO12RSB0	E9	IO34RSB0	J1	GEC1/IO74RSB1
B7	IO16RSB0	E10	GCB1/IO37RSB0	J2	GEC0/IO73RSB1
B8	GBC1/IO20RSB0	E11	GCC1/IO35RSB0	J3	GEB1/IO72RSB1
B9	GBB0/IO21RSB0	F1	VCOMPLF	J4	GEA0/IO69RSB1
B10	GBB2/IO27RSB0	F2	GFB0/IO83RSB1	J5	GEB2/IO67RSB1
B11	GBA2/IO25RSB0	F3	GFA0/IO82RSB1	J6	IO62RSB1
C1	IO89RSB1	F4	GFC1/IO86RSB1	J7	GDA2/IO51RSB1
C2	GAC2/IO91RSB1	F5	VCCIB1	J8	GDB2/IO52RSB1
C3	GAB1/IO05RSB0	F6	VCC	J9	TDI
C4	GAB0/IO04RSB0	F7	VCCIB0	J10	TDO
C5	IO09RSB0	F8	GCB2/IO42RSB0	J11	GDC1/IO45RSB0
C6	IO14RSB0	F9	GCC2/IO43RSB0	K1	GEB0/IO71RSB1
C7	GBA0/IO23RSB0	F10	GCB0/IO38RSB0	K2	GEA1/IO70RSB1
C8	GBC0/IO19RSB0	F11	GCA1/IO39RSB0	K3	GEA2/IO68RSB1
C9	IO26RSB0	G1	VCCPLF	K4	IO64RSB1
C10	IO28RSB0	G2	GFB2/IO79RSB1	K5	IO60RSB1
C11	GBC2/IO29RSB0	G3	GFA1/IO81RSB1	K6	IO59RSB1
D1	IO88RSB1	G4	GFB1/IO84RSB1	K7	IO56RSB1
D2	IO90RSB1	G5	GND	K8	TCK
D3	GAB2/IO93RSB1	G6	VCCIB1	K9	TMS

VQ100	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

VQ100	
Pin Number	A3P125 Function
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

VQ100	
Pin Number	A3P125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

PQ208	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	NC
8	NC
9	IO130RSB1
10	IO129RSB1
11	NC
12	IO128RSB1
13	NC
14	NC
15	NC
16	VCC
17	GND
18	VCCIB1
19	IO127RSB1
20	NC
21	GFC1/IO126RSB1
22	GFC0/IO125RSB1
23	GFB1/IO124RSB1
24	GFB0/IO123RSB1
25	VCOMPLF
26	GFA0/IO122RSB1
27	VCCPLF
28	GFA1/IO121RSB1
29	GND
30	GFA2/IO120RSB1
31	NC
32	GFB2/IO119RSB1
33	NC
34	GFC2/IO118RSB1
35	IO117RSB1
36	NC

PQ208	
Pin Number	A3P125 Function
37	IO116RSB1
38	IO115RSB1
39	NC
40	VCCIB1
41	GND
42	IO114RSB1
43	IO113RSB1
44	GEC1/IO112RSB1
45	GEC0/IO111RSB1
46	GEB1/IO110RSB1
47	GEB0/IO109RSB1
48	GEA1/IO108RSB1
49	GEA0/IO107RSB1
50	VMV1
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO106RSB1
56	GEB2/IO105RSB1
57	GEC2/IO104RSB1
58	IO103RSB1
59	IO102RSB1
60	IO101RSB1
61	IO100RSB1
62	VCCIB1
63	IO99RSB1
64	IO98RSB1
65	GND
66	IO97RSB1
67	IO96RSB1
68	IO95RSB1
69	IO94RSB1
70	IO93RSB1
71	VCC
72	VCCIB1

PQ208	
Pin Number	A3P125 Function
73	IO92RSB1
74	IO91RSB1
75	IO90RSB1
76	IO89RSB1
77	IO88RSB1
78	IO87RSB1
79	IO86RSB1
80	IO85RSB1
81	GND
82	IO84RSB1
83	IO83RSB1
84	IO82RSB1
85	IO81RSB1
86	IO80RSB1
87	IO79RSB1
88	VCC
89	VCCIB1
90	IO78RSB1
91	IO77RSB1
92	IO76RSB1
93	IO75RSB1
94	IO74RSB1
95	IO73RSB1
96	GDC2/IO72RSB1
97	GND
98	GDB2/IO71RSB1
99	GDA2/IO70RSB1
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV1
105	GND
106	VPUMP
107	NC
108	TDO

PQ208	
Pin Number	A3P250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO115UDB3
9	IO115VDB3
10	IO114UDB3
11	IO114VDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	VCC
17	GND
18	VCCIB3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	VCOMPLF
26	GFA0/IO108NPB3
27	VCCPLF
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC

PQ208	
Pin Number	A3P250 Function
37	IO104PDB3
38	IO104NDB3
39	IO103PSB3
40	VCCIB3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	VCCIB2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P250 Function
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	VCC
89	VCCIB2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

FG256	
Pin Number	A3P400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0

FG256	
Pin Number	A3P400 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0

FG256	
Pin Number	A3P400 Function
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances ¹ (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances ¹ (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21