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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	-
Number of I/O	77
Number of Gates	30000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p030-1vq100i

ProASIC3 Flash Family FPGAs

ProASIC3 Devices	A3P015 ¹	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex-M1 Devices ²					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
Package Pins								
QFN	QN68	QN48, QN68, QN132 ⁷	QN132 ⁷	QN132 ⁷	QN132 ⁷			
CS			CS121	VQ100	VQ100			
VQFP		VQ100	VQ100	TQ144	TQ144			
TQFP			TQ144	PQ208	PQ208	PQ208	PQ208	PQ208
PQFP			PQ208	FG144	FG144/256 ⁵	FG144/256/ 484	FG144/256/ 484	FG144/256/ 484
FBGA			FG144					

Notes:

1. A3P015 is not recommended for new designs.
2. Refer to the [Cortex-M1](#) product brief for more information.
3. AES is not available for Cortex-M1 ProASIC3 devices.
4. Six chip (main) and three quadrant global networks are available for A3P060 and above.
5. The M1A3P250 device does not support this package.
6. For higher densities and support of additional features, refer to the [ProASIC3E Flash Family FPGAs](#) datasheet.
7. Package not available.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from -7.56 ns to $+11.12$ ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0° , 90° , 180° , and 270° . Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = $50\% \pm 1.5\%$ or better (for PLL only)
- Low output jitter: worst case $< 2.5\% \times$ clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = $300 \mu\text{s}$ (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of $40 \text{ ps} \times (350 \text{ MHz} / f_{OUT_CCC})$ (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported ([Table 1-1](#)).

Table 1-1 • I/O Standards Supported

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west Banks of A3P250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	✓	✓	Not supported
Standard	All banks of A3P015 and A3P030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the [FlashPro User's Guide](#) for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify ([Figure 1-4 on page 1-8](#)).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 – I/O is set to drive out logic High

Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings ¹
Applicable to Advanced I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	468.67
3.3 V LVCMOS Wide Range ⁴	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. PDC3 is the static power (where applicable) measured on VCCI.
3. PAC10 is the total dynamic power measured on VCC and VCCI.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-12 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings ¹
Applicable to Standard Plus I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	452.67
3.3 V LVCMOS Wide Range ⁴	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on VMV.
3. P_{AC10} is the total dynamic power measured on VCC and VMV.
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

User I/O Characteristics

Timing Model

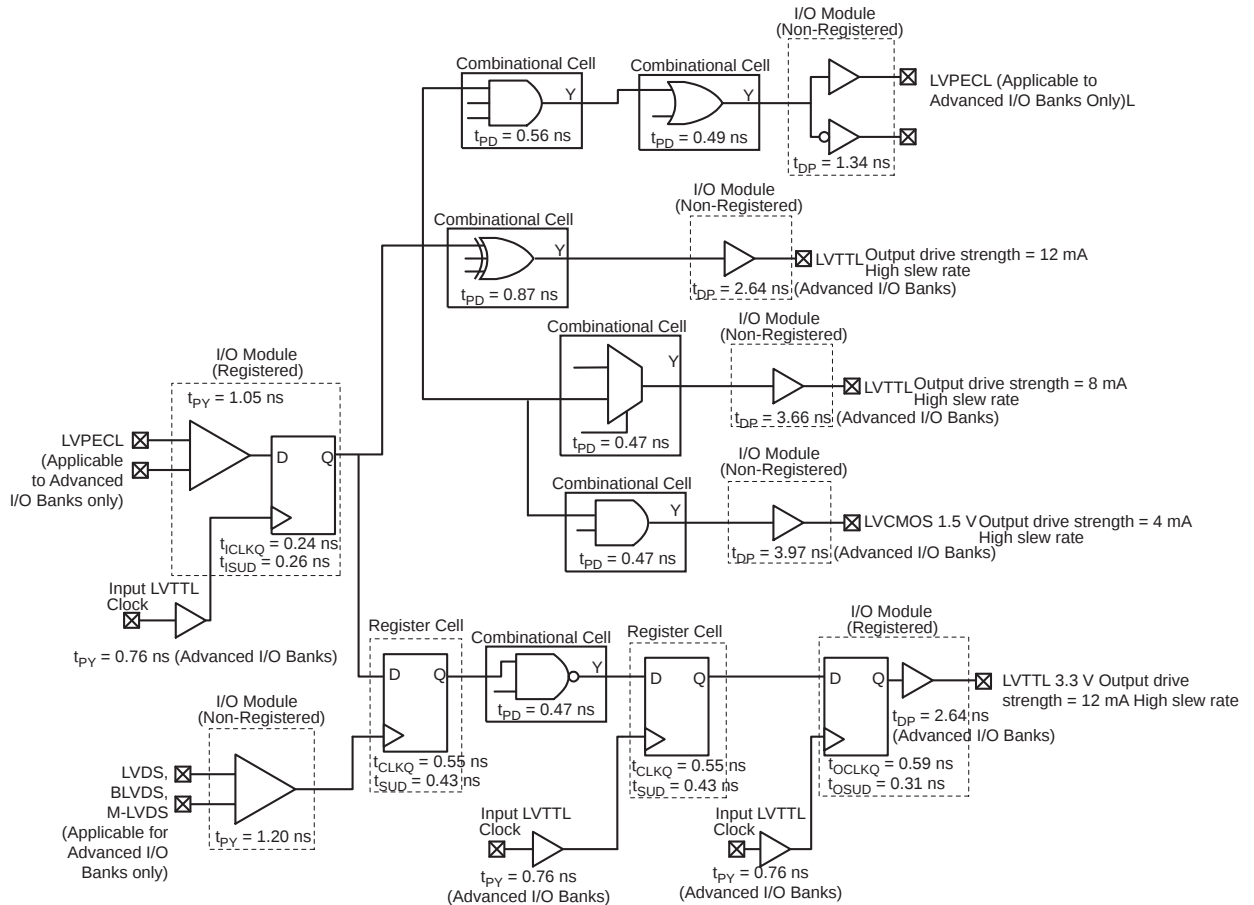


Figure 2-3 • Timing Model

Operating Conditions: -2 Speed, Commercial Temperature Range ($T_j = 70^\circ\text{C}$), Worst Case
VCC = 1.425 V

FG484	
Pin Number	A3P600 Function
K19	IO75NDB1
K20	NC
K21	IO76NDB1
K22	IO76PDB1
L1	NC
L2	IO155PDB3
L3	NC
L4	GFB0/IO163NPB3
L5	GFA0/IO162NDB3
L6	GFB1/IO163PPB3
L7	VCOMPLF
L8	GFC0/IO164NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO69NPB1
L16	GCB1/IO70PPB1
L17	GCA0/IO71NPB1
L18	IO67NPB1
L19	GCB0/IO70NPB1
L20	IO77PDB1
L21	IO77NDB1
L22	IO78NPB1
M1	NC
M2	IO155NDB3
M3	IO158NPB3
M4	GFA2/IO161PPB3
M5	GFA1/IO162PDB3
M6	VCCPLF
M7	IO160NDB3
M8	GFB2/IO160PDB3
M9	VCC
M10	GND

FG484	
Pin Number	A3P600 Function
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO73PPB1
M16	GCA1/IO71PPB1
M17	GCC2/IO74PPB1
M18	IO80PPB1
M19	GCA2/IO72PDB1
M20	IO79PPB1
M21	IO78PPB1
M22	NC
N1	IO154NDB3
N2	IO154PDB3
N3	NC
N4	GFC2/IO159PDB3
N5	IO161NPB3
N6	IO156PPB3
N7	IO129RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO73NPB1
N17	IO80NPB1
N18	IO74NPB1
N19	IO72NDB1
N20	NC
N21	IO79NPB1
N22	NC
P1	NC
P2	IO153PDB3

FG484	
Pin Number	A3P600 Function
P3	IO153NDB3
P4	IO159NDB3
P5	IO156NPB3
P6	IO151PPB3
P7	IO158PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO87NPB1
P17	IO85NDB1
P18	IO85PDB1
P19	IO84PDB1
P20	NC
P21	IO81PDB1
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO150PDB3
R5	IO151NPB3
R6	IO147NPB3
R7	GEC0/IO146NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO117RSB2
R12	IO110RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO94RSB2

Revision	Changes	Page								
Advance v0.6 (continued)	The "Programming" section was updated to include information concerning serialization.	2-53								
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54								
	"DC and Switching Characteristics" chapter was updated with new information.	3-1								
	The A3P060 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P125 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P060 "144-Pin TQFP" pin table was updated.	4-16								
	The A3P125 "144-Pin TQFP" pin table was updated.	4-18								
	The A3P125 "208-Pin PQFP" pin table was updated.	4-21								
	The A3P400 "208-Pin PQFP" pin table was updated.	4-25								
	The A3P060 "144-Pin FBGA" pin table was updated.	4-32								
	The A3P125 "144-Pin FBGA" pin table is new.	4-34								
	The A3P400 "144-Pin FBGA" is new.	4-38								
	The A3P400 "256-Pin FBGA" was updated.	4-48								
	The A3P1000 "256-Pin FBGA" was updated.	4-54								
	The A3P400 "484-Pin FBGA" was updated.	4-58								
	The A3P1000 "484-Pin FBGA" was updated.	4-68								
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14								
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23								
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29								
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36								
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32								
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45								
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54								
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68								
Advance v0.5 (November 2005)	The "I/Os Per Package" table was updated for the following devices and packages: <table><tr><td>Device</td><td>Package</td></tr><tr><td>A3P250/M7ACP250</td><td>VQ100</td></tr><tr><td>A3P250/M7ACP250</td><td>FG144</td></tr><tr><td>A3P1000</td><td>FG256</td></tr></table>	Device	Package	A3P250/M7ACP250	VQ100	A3P250/M7ACP250	FG144	A3P1000	FG256	ii
Device	Package									
A3P250/M7ACP250	VQ100									
A3P250/M7ACP250	FG144									
A3P1000	FG256									
Advance v0.4	M7 device information is new.	N/A								
	The I/O counts in the "I/Os Per Package" table were updated.	ii								
Advance v0.3	The "I/Os Per Package" table was updated.	ii								
	M7 device information is new.	N/A								
	Table 2-4 • ProASIC3 Globals/Spines/Rows by Device was updated to include the number or rows in each top or bottom spine.	2-16								
	EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options.	2-24								

Revision	Changes	Page
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68