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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p060-1fg144

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



ProASIC3 Devices	A3P015 ¹	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex-M1 Devices ²					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
Package Pins QFN CS VQFP TQFP PQFP FBGA	QN68	QN48, QN68, QN132 ⁷ VQ100	QN132 ⁷ CS121 VQ100 TQ144 FG144	QN132 ⁷ VQ100 TQ144 PQ208 FG144	QN132 ⁷ VQ100 PQ208 FG144/256 ⁵	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484

Notes:

- A3P015 is not recommended for new designs.
 Refer to the Cortex-M1 product brief for more information.
 AES is not available for Cortex-M1 ProASIC3 devices.
 Six chip (main) and three quadrant global networks are available for A3P060 and above.
 The M1A3P250 device does not support this package.
 For higher densities and support of additional features, refer to the ProASIC3E Flash Family FPGAs datasheet.
 Package not available.



User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero[®] System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.



I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

		I/O Standards Supported				
I/O Bank Type	Device and Bank Location	LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS		
Advanced	East and west Banks of A3P250 and larger devices	\checkmark	\checkmark	\checkmark		
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	\checkmark	\checkmark	Not supported		
Standard	All banks of A3P015 and A3P030	\checkmark	Not supported	Not supported		

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a poweredup system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

- Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.
 - 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
 - 2. From the FlashPro GUI, click PDB Configuration. A FlashPoint Programming File Generator window appears.
 - 3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
 - 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
 - 5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 I/O is set to drive out logic High



Table 2-2 • Recommended Operating Conditions¹

Symbol	Parame	eters ¹	Commercial	Industrial	Units
TJ	Junction temperature		0 to 85 ²	-40 to 100 ²	°C
VCC ³	1.5 V DC core supply volta	ge	1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage Programming Mode		3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL))	1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV ⁵	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage 2.5 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
			2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage	3.0 to 3. <u>6</u>	3.0 to 3. <u>6</u>	V	
	3.3 V wide range DC suppl	ly voltage ⁶	2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.

- 2. Software Default Junction Temperature Range in the Libero[®] System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.
- 3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.
- 4. VPUMP can be left floating during operation (not programming mode).
- 5. VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.
- 6. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.



F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1}, P_{AC2}, P_{AC3}, and P_{AC4} are device-dependent.

Sequential Cells Contribution—P_{S-CELL}

 $P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

 N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution—P_{C-CELL}

 $P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

 $N_{C\mbox{-}C\mbox{-}E\mbox{-}L\mbox{-}L}$ is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

 $\mathsf{F}_{\mathsf{CLK}}$ is the global clock signal frequency.

Routing Net Contribution—P_{NET}

 $P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

 α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

 F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution—PINPUTS

 $P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

N_{INPUTS} is the number of I/O input buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-14.

 F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution—POUTPUTS

 $P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

N_{OUTPUTS} is the number of I/O output buffers used in the design.

 α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-14.

 β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-17 on page 2-14.

F_{CLK} is the global clock signal frequency.





Figure 2-4 • Input Buffer Timing Model and Delays (Example)



I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min	Мах	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz	-	8	pF
CINCLK	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz	_	8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances¹ Applicable to Advanced I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range ⁴	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

- 2. R_(PULL-DOWN-MAX) = (VOLspec) / IOLspec
- 3. R_(PULL-UP-MAX) = (VCCImax VOHspec) / IOHspec

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

^{1.} These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

Table 2-34 • I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range ²	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

- 1. $T_{.1} = 100^{\circ}C$
- Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.



Table 2-64 • 2.5 V LVCMOS High Slew

Commercial-Case Conditions: T = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	-1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	-2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	–1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	-1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	-2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-65 • 2.5 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	-1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	-2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	-1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	-2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



I/O Register Specifications





Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.



Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-90. Table 2-108 to Table 2-114 on page 2-89 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.



Table 2-122 • A3P250 FIFO 2k×2

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup Time	4.39	5.00	5.88	ns
t _{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t _{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t _{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t _{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t _{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Table 2-123 • A3P250 FIFO 4k×1

Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup Time	4.86	5.53	6.50	ns
t _{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t _{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t _{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t _{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns



CS121					
Pin Number	A3P060 Function				
K10	VPUMP				
K11	GDB1/IO47RSB0				
L1	VMV1				
L2	GNDQ				
L3	IO65RSB1				
L4	IO63RSB1				
L5	IO61RSB1				
L6	IO58RSB1				
L7	IO57RSB1				
L8	IO55RSB1				
L9	GNDQ				
L10	GDA0/IO50RSB0				
L11	VMV1				



TQ144 – Top View



Note

For more information on package drawings, see PD3068: Package Mechanical Drawings.

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Package Pin Assignments

FG144		FG144 FG14		G144	
Pin Number	A3P125 Function	Pin Number	A3P125 Function	Pin Number	A3P125 Function
A1	GNDQ	D1	IO128RSB1	G1	GFA1/IO121RSB1
A2	VMV0	D2	IO129RSB1	G2	GND
A3	GAB0/IO02RSB0	D3	IO130RSB1	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO67RSB1	G4	GFA0/IO122RSB1
A5	IO11RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO18RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO61RSB0
A9	IO25RSB0	D9	GBB2/IO43RSB0	G9	IO48RSB0
A10	GBA0/IO39RSB0	D10	IO28RSB0	G10	GCC2/IO59RSB0
A11	GBA1/IO40RSB0	D11	IO44RSB0	G11	IO47RSB0
A12	GNDQ	D12	GCB1/IO53RSB0	G12	GCB2/IO58RSB0
B1	GAB2/IO69RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO125RSB1	H2	GFB2/IO119RSB1
B3	GAA0/IO00RSB0	E3	GFC1/IO126RSB1	H3	GFC2/IO118RSB1
B4	GAA1/IO01RSB0	E4	VCCIB1	H4	GEC1/IO112RSB1
B5	IO08RSB0	E5	IO68RSB1	H5	VCC
B6	IO14RSB0	E6	VCCIB0	H6	IO50RSB0
B7	IO19RSB0	E7	VCCIB0	H7	IO60RSB0
B8	IO22RSB0	E8	GCC1/IO51RSB0	H8	GDB2/IO71RSB1
B9	GBB0/IO37RSB0	E9	VCCIB0	H9	GDC0/IO62RSB0
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO56RSB0	H11	IO49RSB0
B12	VMV0	E12	IO46RSB0	H12	VCC
C1	IO132RSB1	F1	GFB0/IO123RSB1	J1	GEB1/IO110RSB1
C2	GFA2/IO120RSB1	F2	VCOMPLF	J2	IO115RSB1
C3	GAC2/IO131RSB1	F3	GFB1/IO124RSB1	J3	VCCIB1
C4	VCC	F4	IO127RSB1	J4	GEC0/IO111RSB1
C5	IO10RSB0	F5	GND	J5	IO116RSB1
C6	IO12RSB0	F6	GND	J6	IO117RSB1
C7	IO21RSB0	F7	GND	J7	VCC
C8	IO24RSB0	F8	GCC0/IO52RSB0	J8	ТСК
C9	IO27RSB0	F9	GCB0/IO54RSB0	J9	GDA2/IO70RSB1
C10	GBA2/IO41RSB0	F10	GND	J10	TDO
C11	IO42RSB0	F11	GCA1/IO55RSB0	J11	GDA1/IO65RSB0
C12	GBC2/IO45RSB0	F12	GCA2/IO57RSB0	J12	GDB1/IO63RSB0



FG144					
Pin Number	A3P250 Function				
K1	GEB0/IO99NDB3				
K2	GEA1/IO98PDB3				
K3	GEA0/IO98NDB3				
K4	GEA2/IO97RSB2				
K5	IO90RSB2				
K6	IO84RSB2				
K7	GND				
K8	IO66RSB2				
K9	GDC2/IO63RSB2				
K10	GND				
K11	GDA0/IO60VDB1				
K12	GDB0/IO59VDB1				
L1	GND				
L2	VMV3				
L3	GEB2/IO96RSB2				
L4	IO91RSB2				
L5	VCCIB2				
L6	IO82RSB2				
L7	IO80RSB2				
L8	IO72RSB2				
L9	TMS				
L10	VJTAG				
L11	VMV2				
L12	TRST				
M1	GNDQ				
M2	GEC2/IO95RSB2				
M3	IO92RSB2				
M4	IO89RSB2				
M5	IO87RSB2				
M6	IO85RSB2				
M7	IO78RSB2				
M8	IO76RSB2				
M9	TDI				
M10	VCCIB2				
M11	VPUMP				
M12	GNDQ				



FG144					
Pin Number	A3P600 Function				
K1	GEB0/IO145NDB3				
K2	GEA1/IO144PDB3				
K3	GEA0/IO144NDB3				
K4	GEA2/IO143RSB2				
K5	IO119RSB2				
K6	IO111RSB2				
K7	GND				
K8	IO94RSB2				
K9	GDC2/IO91RSB2				
K10	GND				
K11	GDA0/IO88NDB1				
K12	GDB0/IO87NDB1				
L1	GND				
L2	VMV3				
L3	GEB2/IO142RSB2				
L4	IO136RSB2				
L5	VCCIB2				
L6	IO115RSB2				
L7	IO103RSB2				
L8	IO97RSB2				
L9	TMS				
L10	VJTAG				
L11	VMV2				
L12	TRST				
M1	GNDQ				
M2	GEC2/IO141RSB2				
M3	IO138RSB2				
M4	IO123RSB2				
M5	IO126RSB2				
M6	IO134RSB2				
M7	IO108RSB2				
M8	IO99RSB2				
M9	TDI				
M10	VCCIB2				
M11	VPUMP				
M12	GNDQ				

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Package Pin Assignments

FG256		FG256		FG256		
Pin Number	A3P400 Function	Pin Number	A3P400 Function	Pin Number	A3P400 Function	
A1	GND	C5	GAC0/IO04RSB0	E9	IO31RSB0	
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	VCCIB0	
A3	GAA1/IO01RSB0	C7	IO20RSB0	E11	VCCIB0	
A4	GAB0/IO02RSB0	C8	IO24RSB0	E12	VMV1	
A5	IO16RSB0	C9	IO33RSB0	E13	GBC2/IO62PDB1	
A6	IO17RSB0	C10	IO39RSB0	E14	IO65RSB1	
A7	IO22RSB0	C11	IO45RSB0	E15	IO52RSB0	
A8	IO28RSB0	C12	GBC0/IO54RSB0	E16	IO66PDB1	
A9	IO34RSB0	C13	IO48RSB0	F1	IO150NDB3	
A10	IO37RSB0	C14	VMV0	F2	IO149NPB3	
A11	IO41RSB0	C15	IO61NPB1	F3	IO09RSB0	
A12	IO43RSB0	C16	IO63PDB1	F4	IO152UDB3	
A13	GBB1/IO57RSB0	D1	IO151VDB3	F5	VCCIB3	
A14	GBA0/IO58RSB0	D2	IO151UDB3	F6	GND	
A15	GBA1/IO59RSB0	D3	GAC2/IO153UDB3	F7	VCC	
A16	GND	D4	IO06RSB0	F8	VCC	
B1	GAB2/IO154UDB3	D5	GNDQ	F9	VCC	
B2	GAA2/IO155UDB3	D6	IO10RSB0	F10	VCC	
B3	IO12RSB0	D7	IO19RSB0	F11	GND	
B4	GAB1/IO03RSB0	D8	IO26RSB0	F12	VCCIB1	
B5	IO13RSB0	D9	IO30RSB0	F13	IO62NDB1	
B6	IO14RSB0	D10	IO40RSB0	F14	IO49RSB0	
B7	IO21RSB0	D11	IO46RSB0	F15	IO64PPB1	
B8	IO27RSB0	D12	GNDQ	F16	IO66NDB1	
B9	IO32RSB0	D13	IO47RSB0	G1	IO148NDB3	
B10	IO38RSB0	D14	GBB2/IO61PPB1	G2	IO148PDB3	
B11	IO42RSB0	D15	IO53RSB0	G3	IO149PPB3	
B12	GBC1/IO55RSB0	D16	IO63NDB1	G4	GFC1/IO147PPB3	
B13	GBB0/IO56RSB0	E1	IO150PDB3	G5	VCCIB3	
B14	IO44RSB0	E2	IO08RSB0	G6	VCC	
B15	GBA2/IO60PDB1	E3	IO153VDB3	G7	GND	
B16	IO60NDB1	E4	IO152VDB3	G8	GND	
C1	IO154VDB3	E5	VMV0	G9	GND	
C2	IO155VDB3	E6	VCCIB0	G10	GND	
C3	IO11RSB0	E7	VCCIB0	G11	VCC	
C4	IO07RSB0	E8	IO25RSB0	G12	VCCIB1	



Package Pin Assignments

FG256		FG256		FG256		
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	
A1	GND	C7	IO25RSB0	E13	GBC2/IO80PDB1	
A2	GAA0/IO00RSB0	C8	IO36RSB0	E14	IO83PPB1	
A3	GAA1/IO01RSB0	C9	IO42RSB0	E15	IO86PPB1	
A4	GAB0/IO02RSB0	C10	IO49RSB0	E16	IO87PDB1	
A5	IO16RSB0	C11	IO56RSB0	F1	IO217NDB3	
A6	IO22RSB0	C12	GBC0/IO72RSB0	F2	IO218NDB3	
A7	IO28RSB0	C13	IO62RSB0	F3	IO216PDB3	
A8	IO35RSB0	C14	VMV0	F4	IO216NDB3	
A9	IO45RSB0	C15	IO78NDB1	F5	VCCIB3	
A10	IO50RSB0	C16	IO81NDB1	F6	GND	
A11	IO55RSB0	D1	IO222NDB3	F7	VCC	
A12	IO61RSB0	D2	IO222PDB3	F8	VCC	
A13	GBB1/IO75RSB0	D3	GAC2/IO223PDB3	F9	VCC	
A14	GBA0/IO76RSB0	D4	IO223NDB3	F10	VCC	
A15	GBA1/IO77RSB0	D5	GNDQ	F11	GND	
A16	GND	D6	IO23RSB0	F12	VCCIB1	
B1	GAB2/IO224PDB3	D7	IO29RSB0	F13	IO83NPB1	
B2	GAA2/IO225PDB3	D8	IO33RSB0	F14	IO86NPB1	
B3	GNDQ	D9	IO46RSB0	F15	IO90PPB1	
B4	GAB1/IO03RSB0	D10	IO52RSB0	F16	IO87NDB1	
B5	IO17RSB0	D11	IO60RSB0	G1	IO210PSB3	
B6	IO21RSB0	D12	GNDQ	G2	IO213NDB3	
B7	IO27RSB0	D13	IO80NDB1	G3	IO213PDB3	
B8	IO34RSB0	D14	GBB2/IO79PDB1	G4	GFC1/IO209PPB3	
B9	IO44RSB0	D15	IO79NDB1	G5	VCCIB3	
B10	IO51RSB0	D16	IO82NSB1	G6	VCC	
B11	IO57RSB0	E1	IO217PDB3	G7	GND	
B12	GBC1/IO73RSB0	E2	IO218PDB3	G8	GND	
B13	GBB0/IO74RSB0	E3	IO221NDB3	G9	GND	
B14	IO71RSB0	E4	IO221PDB3	G10	GND	
B15	GBA2/IO78PDB1	E5	VMV0	G11	VCC	
B16	IO81PDB1	E6	VCCIB0	G12	VCCIB1	
C1	IO224NDB3	E7	VCCIB0	G13	GCC1/IO91PPB1	
C2	IO225NDB3	E8	IO38RSB0	G14	IO90NPB1	
C3	VMV3	E9	IO47RSB0	G15	IO88PDB1	
C4	IO11RSB0	E10	VCCIB0	G16	IO88NDB1	
C5	GAC0/IO04RSB0	E11	VCCIB0	H1	GFB0/IO208NPB3	
C6	GAC1/IO05RSB0	E12	VMV1	H2	GFA0/IO207NDB3	



Revision	Changes	Page		
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV		
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	2-2		
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).			
	Libero Integrated Design Environment (IDE) was changed to Libero System-on- Chip (SoC) throughout the document (SAR 40284).	NA		
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1		
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2		
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933).	2-31		
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68		
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99		
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1		