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### Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

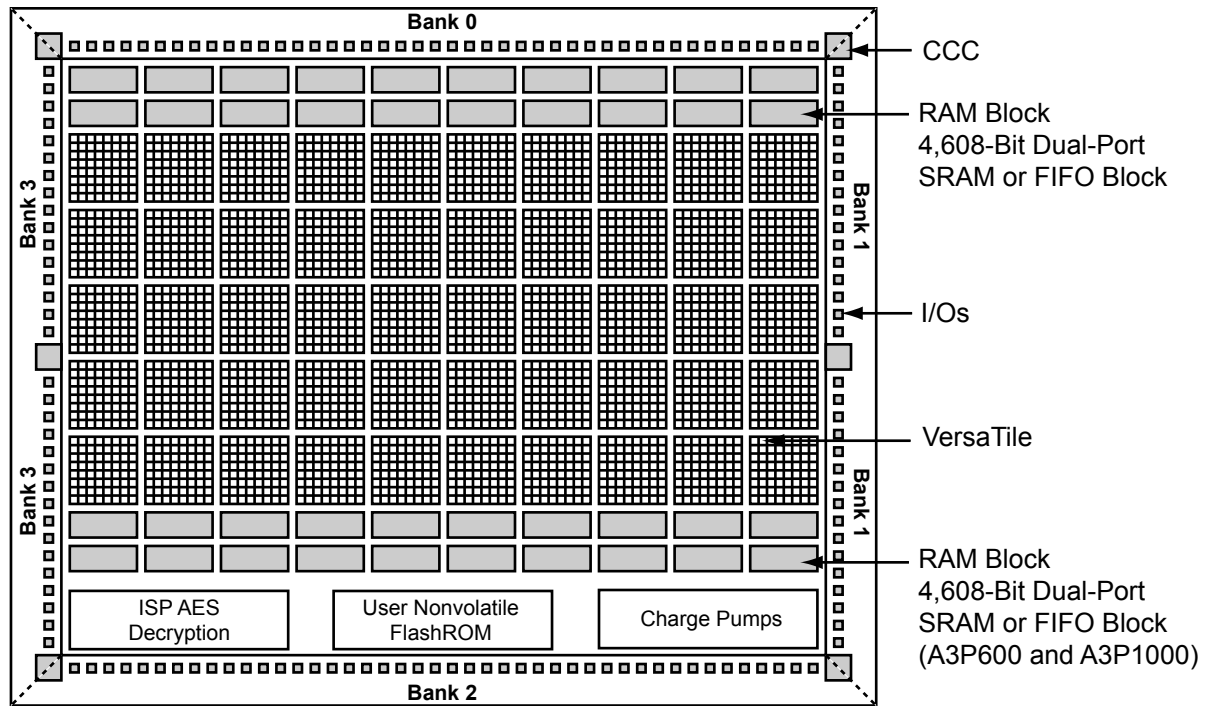
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

#### Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	18432
Number of I/O	96
Number of Gates	60000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a3p060-2fgg144">https://www.e-xfl.com/product-detail/microchip-technology/a3p060-2fgg144</a>



**Figure 1-2 • ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P600, and A3P1000)**

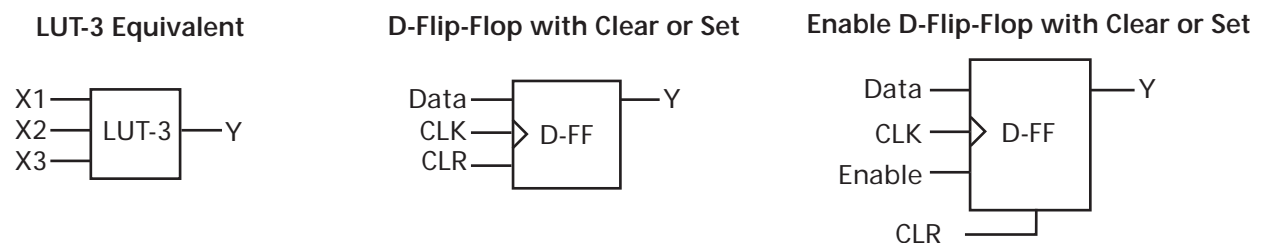
The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

### VersaTiles

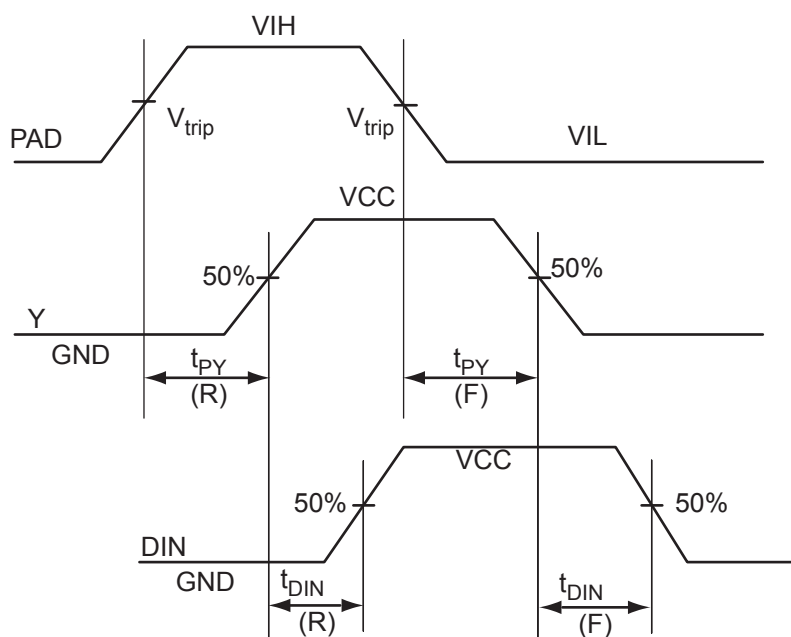
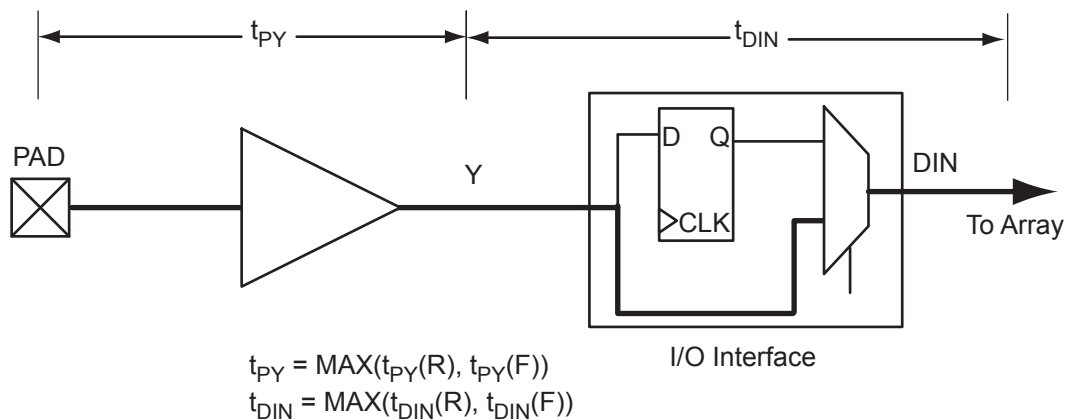
The ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC<sup>PLUS</sup>® core tiles. The ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.



**Figure 1-3 • VersaTile Configurations**



**Figure 2-4 • Input Buffer Timing Model and Delays (Example)**

## Single-Ended I/O Characteristics

### 3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

**Table 2-37 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Advanced I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA <sup>3</sup>	Max mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-38 • Minimum and Maximum DC Input and Output Levels**  
Applicable to Standard Plus I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA <sup>3</sup>	Max mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where  $-0.3\text{ V} < V_{IN} < V_{IL}$ .
2. IIH is the input leakage current per I/O pin over recommended operating conditions  $V_{IH} < V_{IN} < V_{CCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

**Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 3.0\text{ V}$**   
**Applicable to Standard Plus I/O Banks**

Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
100 $\mu\text{A}$	2 mA	Std.	0.60	11.14	0.04	1.52	0.43	11.14	9.54	3.51	3.61	14.53	12.94	ns
		–1	0.51	9.48	0.04	1.29	0.36	9.48	8.12	2.99	3.07	12.36	11.00	ns
		–2	0.45	8.32	0.03	1.14	0.32	8.32	7.13	2.62	2.70	10.85	9.66	ns
100 $\mu\text{A}$	4 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 $\mu\text{A}$	6 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 $\mu\text{A}$	8 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
100 $\mu\text{A}$	16 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100\text{ }\mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-72 • 1.8 V LVC MOS High Slew****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.7\text{ V}$** **Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	11.33	0.04	1.20	0.43	8.72	11.33	2.24	1.52	10.96	13.57	ns
	–1	0.56	9.64	0.04	1.02	0.36	7.42	9.64	1.91	1.29	9.32	11.54	ns
	–2	0.49	8.46	0.03	0.90	0.32	6.51	8.46	1.68	1.14	8.18	10.13	ns
4 mA	Std.	0.66	6.48	0.04	1.20	0.43	5.48	6.48	2.65	2.60	7.72	8.72	ns
	–1	0.56	5.51	0.04	1.02	0.36	4.66	5.51	2.25	2.21	6.56	7.42	ns
	–2	0.49	4.84	0.03	0.90	0.32	4.09	4.84	1.98	1.94	5.76	6.51	ns
6 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
8 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## Timing Characteristics

**Table 2-80 • 1.5 V LVCMOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$ , Worst-Case  $V_{CCI} = 1.4\text{ V}$   
 Applicable to Advanced I/O Banks

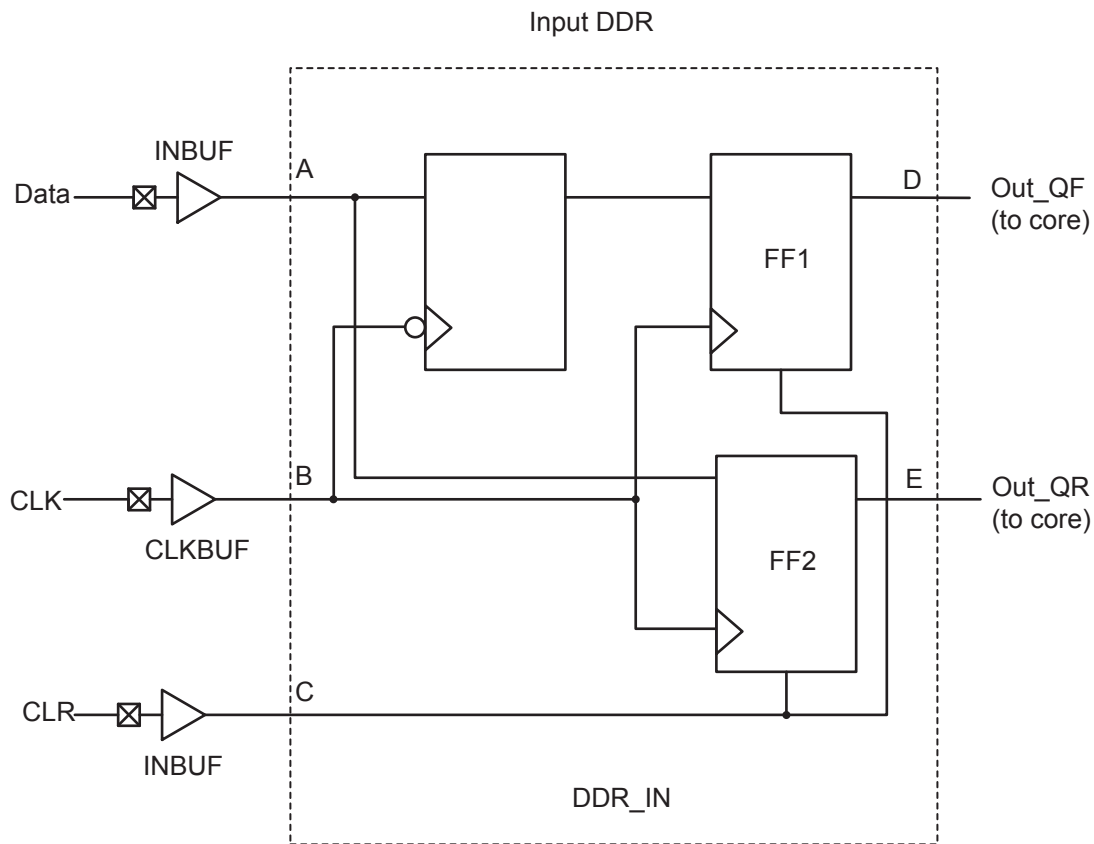
Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	–1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	–2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	–1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	–2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
6 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	–1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	–2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
8 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	–1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	–2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	–1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	–2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

### Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## DDR Module Specifications

### Input DDR Module



**Figure 2-20 • Input DDR Timing Model**

**Table 2-101 • Parameter Definitions**

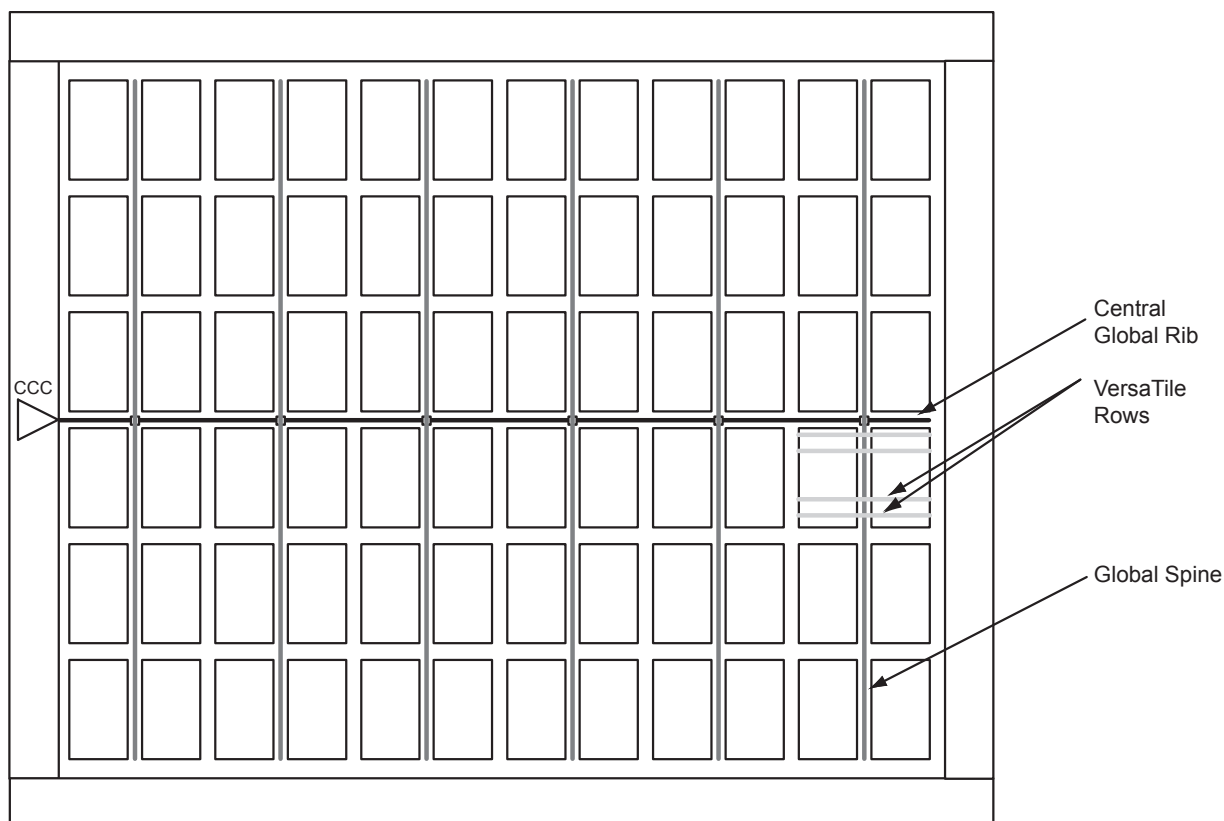
Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{\text{DDRCLKQ1}}$	Clock-to-Out Out_QR	B, D
$t_{\text{DDRCLKQ2}}$	Clock-to-Out Out_QF	B, E
$t_{\text{DDRISUD}}$	Data Setup Time of DDR input	A, B
$t_{\text{DDR IHD}}$	Data Hold Time of DDR input	A, B
$t_{\text{DDRICLR2Q1}}$	Clear-to-Out Out_QR	C, D
$t_{\text{DDRICLR2Q2}}$	Clear-to-Out Out_QF	C, E
$t_{\text{DDRIREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRIRECCLR}}$	Clear Recovery	C, B



## Global Resource Characteristics

### A3P250 Clock Tree Topology

Clock delays are device-specific. [Figure 2-28](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-28](#) is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.



**Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing**

### Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-90](#). [Table 2-108](#) to [Table 2-114 on page 2-89](#) present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

**Table 2-113 • A3P600 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
$t_{RCKH}$	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-114 • A3P1000 Global Resource**  
**Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425\text{ V}$**

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
$t_{RCKH}$	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## Clock Conditioning Circuits

### CCC Electrical Specifications

#### Timing Characteristics

**Table 2-115 • ProASIC3 CCC/PLL Specification**

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency $f_{IN\_CCC}$	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency $f_{OUT\_CCC}$	0.75		350	MHz
Serial Clock (SCLK) for Dynamic PLL <sup>1</sup>			125	MHz
Delay Increments in Programmable Delay Blocks <sup>2, 3</sup>		200 <sup>4</sup>		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter $F_{CCC\_OUT}$	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
(A3P250 and A3P1000 only) LockControl = 0			300	μs
LockControl = 1			300	μs
(all other dies) LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter <sup>5</sup>				
(A3P250 and A3P1000 only) LockControl = 0			1.6	ns
LockControl = 1			1.6	ns
(all other dies) LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay <sup>1, 2, 3</sup>	0.6		5.56	ns
Delay Range in Block: Programmable Delay <sup>2, 3</sup>	0.225		5.56	ns
Delay Range in Block: Fixed Delay <sup>2, 3</sup>		2.2		ns

**Notes:**

- Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
- This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) for deratings.
- $T_J = 25^\circ\text{C}$ ,  $V_{CC} = 1.5\text{ V}$
- When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.
- Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
- The A3P030 device does not contain a PLL.

**Table 2-117 • RAM512X18****Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425\text{ V}$** 

Parameter	Description	-2	-1	Std.	Units
$t_{AS}$	Address setup time	0.25	0.28	0.33	ns
$t_{AH}$	Address hold time	0.00	0.00	0.00	ns
$t_{ENS}$	REN, WEN setup time	0.13	0.15	0.17	ns
$t_{ENH}$	REN, WEN hold time	0.10	0.11	0.13	ns
$t_{DS}$	Input data (WD) setup time	0.18	0.21	0.25	ns
$t_{DH}$	Input data (WD) hold time	0.00	0.00	0.00	ns
$t_{CKQ1}$	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
$t_{CKQ2}$	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
$t_{C2CRWH}^1$	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
$t_{C2CWRH}^1$	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
$t_{RSTBQ}$	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
$t_{CYC}$	Clock cycle time	3.23	3.68	4.32	ns
$F_{MAX}$	Maximum frequency	310	272	231	MHz

**Notes:**

1. For more information, refer to the application note [Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs](#).
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

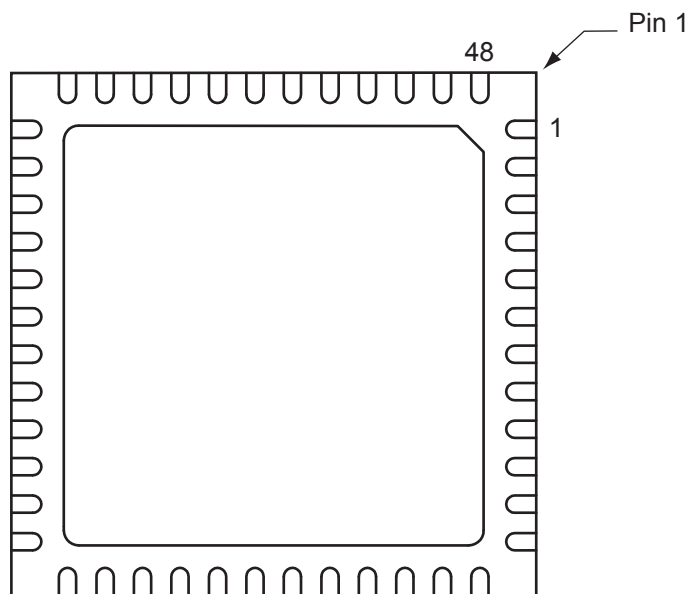
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## 4 – Package Pin Assignments

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### QN48 – Bottom View

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*Note:* The die attach paddle center of the package is tied to ground (GND).

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#### **Note**

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

QN68	
Pin Number	A3P030 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

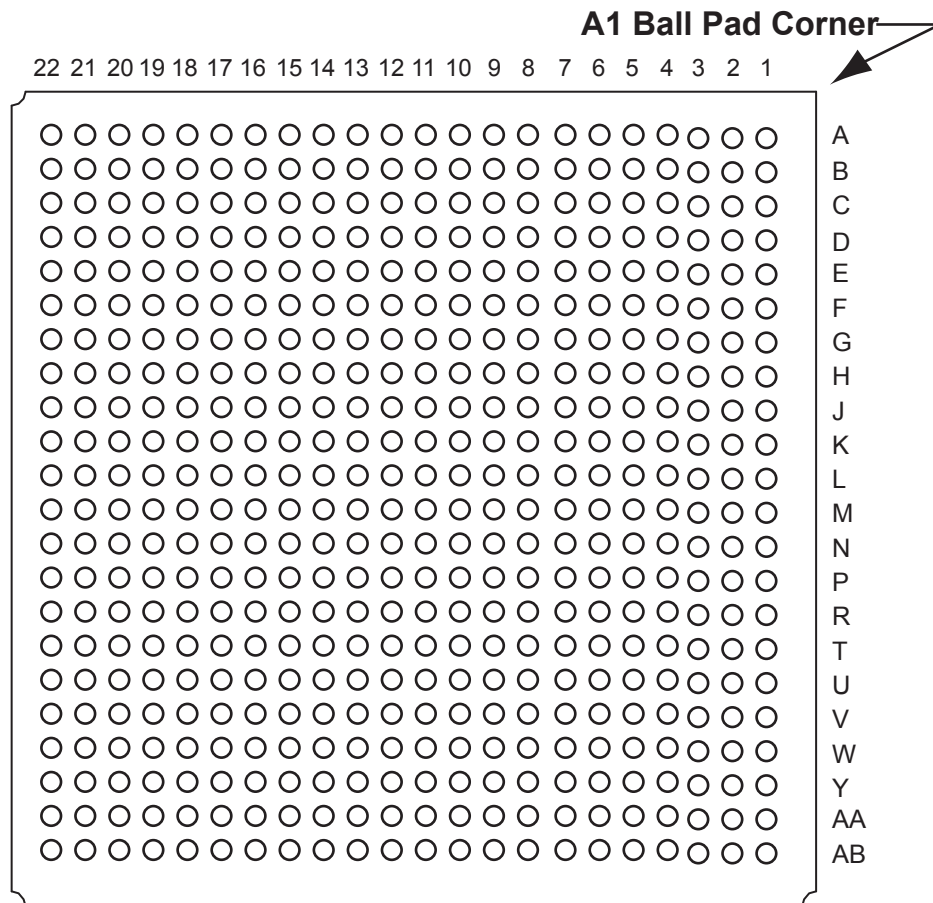
QN68	
Pin Number	A3P030 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

PQ208	
Pin Number	A3P600 Function
109	TRST
110	VJTAG
111	GDA0/IO88NDB1
112	GDA1/IO88PDB1
113	GDB0/IO87NDB1
114	GDB1/IO87PDB1
115	GDC0/IO86NDB1
116	GDC1/IO86PDB1
117	IO84NDB1
118	IO84PDB1
119	IO82NDB1
120	IO82PDB1
121	IO81PSB1
122	GND
123	VCCIB1
124	IO77NDB1
125	IO77PDB1
126	NC
127	IO74NDB1
128	GCC2/IO74PDB1
129	GCB2/IO73PSB1
130	GND
131	GCA2/IO72PSB1
132	GCA1/IO71PDB1
133	GCA0/IO71NDB1
134	GCB0/IO70NDB1
135	GCB1/IO70PDB1
136	GCC0/IO69NDB1
137	GCC1/IO69PDB1
138	IO67NDB1
139	IO67PDB1
140	VCCIB1
141	GND
142	VCC
143	IO65PSB1
144	IO64NDB1

PQ208	
Pin Number	A3P600 Function
145	IO64PDB1
146	IO63NDB1
147	IO63PDB1
148	IO62NDB1
149	GBC2/IO62PDB1
150	IO61NDB1
151	GBB2/IO61PDB1
152	IO60NDB1
153	GBA2/IO60PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO59RSB0
159	GBA0/IO58RSB0
160	GBB1/IO57RSB0
161	GBB0/IO56RSB0
162	GND
163	GBC1/IO55RSB0
164	GBC0/IO54RSB0
165	IO52RSB0
166	IO50RSB0
167	IO48RSB0
168	IO46RSB0
169	IO44RSB0
170	VCCIB0
171	VCC
172	IO36RSB0
173	IO35RSB0
174	IO34RSB0
175	IO33RSB0
176	IO32RSB0
177	IO31RSB0
178	GND
179	IO29RSB0
180	IO28RSB0

PQ208	
Pin Number	A3P600 Function
181	IO27RSB0
182	IO26RSB0
183	IO25RSB0
184	IO24RSB0
185	IO23RSB0
186	VCCIB0
187	VCC
188	IO20RSB0
189	IO19RSB0
190	IO18RSB0
191	IO17RSB0
192	IO16RSB0
193	IO14RSB0
194	IO12RSB0
195	GND
196	IO10RSB0
197	IO09RSB0
198	IO08RSB0
199	IO07RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

## FG484 – Bottom View



### Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).



## 5 – Datasheet Information

### List of Changes

The following table lists critical changes that were made in each version of the ProASIC3 datasheet.

Revision	Changes	Page
Revision 18 (March 2016)	Updated 3.3 V DC supply voltage's maximum Commercial and Industrial values from 3.3 V to 3.6 V in <a href="#">Table 2-2</a> (SAR 72693).	<a href="#">2-2</a>
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833).	NA
Revision 17 (June 2015)	Removed PQFP embedded heat spreader info. from <a href="#">Table 2-5</a> (SAR 52320).	<a href="#">2-6</a>
	Updated " <a href="#">VCCIBx I/O Supply Voltage</a> " (SAR 43323).	<a href="#">3-1</a>
Revision 16 (December 2014)	Updated " <a href="#">ProASIC3 Ordering Information</a> ". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079). Added Note "Only devices with package size greater than or equal to 5x5 are supported".	<a href="#">1-IV</a>
	Updated Table Note (2) in <a href="#">Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature</a> so that the Table Note is not applicable for Maximum Storage Temperature T <sub>STG</sub> (SAR 54297).	<a href="#">2-3</a>
	Added values for Drive strength 2 mA in <a href="#">Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew</a> , <a href="#">Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew</a> , <a href="#">Table 2-43 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew</a> , and <a href="#">Table 2-44 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew</a> (SAR 57184).	<a href="#">2-34, 2-35, 2-36, 2-37</a>
	Added <a href="#">Figure 2-1 • High-Temperature Data Retention (HTR)</a> (SAR 45466).	<a href="#">2-3</a>
	Updates made to maintain the style and consistency of the document.	NA
Revision 15 (July 2014)	Added corner pad table note (3) to " <a href="#">QN132 – Bottom View</a> " (SAR 47442).	<a href="#">4-6</a>
	Ambient temperature removed in <a href="#">Table 2-2</a> , table notes and " <a href="#">ProASIC3 Ordering Information</a> " figure were modified (SAR 48343).	<a href="#">2-2</a> <a href="#">1-IV</a>
	Other updates were made to maintain the style and consistency of the datasheet.	NA
Revision 14 (April 2014)	Note added for the discontinuance of QN132 package to the following tables and section: " <a href="#">ProASIC3 Devices</a> ", " <a href="#">I/Os Per Package 1</a> ", " <a href="#">ProASIC3 FPGAs Package Sizes Dimensions</a> " and " <a href="#">QN132 – Bottom View</a> " section (SAR 55118).	<a href="#">I, III, 4-6</a>

Revision	Changes	Page
Revision 10 (continued)	"TBD" for 3.3 V LVCMOS Wide Range in <a href="#">Table 2-28 • I/O Output Buffer Maximum Resistances</a> <sup>1</sup> through <a href="#">Table 2-30 • I/O Output Buffer Maximum Resistances</a> <sup>1</sup> was replaced by "Same as regular 3.3 V" (SAR 33852).	2-26 to 2-28
	The equations in the notes for <a href="#">Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances</a> were corrected (SAR 32470).	2-28
	"TBD" for 3.3 V LVCMOS Wide Range in <a href="#">Table 2-32 • I/O Short Currents IOSH/IOSL</a> through <a href="#">Table 2-34 • I/O Short Currents IOSH/IOSL</a> was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33852).	2-29 to 2-31
	In the " <a href="#">3.3 V LVCMOS Wide Range</a> " section, values were added to <a href="#">Table 2-47</a> through <a href="#">Table 2-49</a> for IOSL and IOSH, replacing "TBD" (SAR 33852).	2-39 to 2-40
	The following sentence was deleted from the " <a href="#">2.5 V LVCMOS</a> " section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer."	2-47
	The table notes were revised for <a href="#">Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels</a> (SAR 33859).	2-66
	Values were added for $F_{DDRIMAX}$ and $F_{DDOMAX}$ in <a href="#">Table 2-102 • Input DDR Propagation Delays</a> and <a href="#">Table 2-104 • Output DDR Propagation Delays</a> (SAR 23919).	2-78, 2-80
	<a href="#">Table 2-115 • ProASIC3 CCC/PLL Specification</a> was updated. A note was added to indicate that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 25705).	2-90
	The following figures were deleted (SAR 29991). Reference was made to a new application note, <i>Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs</i> , which covers these cases in detail (SAR 21770). Figure 2-34 • Write Access after Write onto Same Address Figure 2-35 • Read Access after Write onto Same Address Figure 2-35 • Read Access after Write onto Same Address The port names in the SRAM " <a href="#">Timing Waveforms</a> ", SRAM " <a href="#">Timing Characteristics</a> " tables, <a href="#">Figure 2-39 • FIFO Reset</a> , and the FIFO " <a href="#">Timing Characteristics</a> " tables were revised to ensure consistency with the software names (SARs 29991, 30510).	2-92, 2-94, 2-99 2-102
	The " <a href="#">Pin Descriptions</a> " chapter has been added (SAR 21642).	3-1
	Package names used in the " <a href="#">Package Pin Assignments</a> " section were revised to match standards given in <a href="#">Package Mechanical Drawings</a> (SAR 27395).	4-1
July 2010	The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The " <a href="#">ProASIC3 Device Status</a> " table on page IV indicates the status for each device in the device family.	N/A

Revision	Changes	Page
<b>Revision 2 (cont'd)</b>	The "ProASIC3 FPGAs Package Sizes Dimensions" table is new.	III
	In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm.	IV
	In the General Description section the number of I/Os was updated from 288 to 300.	1-1
	The "QN68 – Bottom View" section is new.	4-3
Packaging v1.2		
<b>Revision 1 (Feb 2008)</b> DC and Switching Characteristics v1.1	In Table 2-2 • Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$ .	2-2
	In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades.	2-3
	The "PLL Behavior at Brownout Condition" section is new.	2-4
	In the "PLL Contribution—PPLL" section, the following was deleted: FCLKIN is the input clock frequency.	2-14
	In Table 2-21 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$ .	2-21
	In Table 2-115 • ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new.	2-90
	Table 2-125 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document.	2-108
	In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0.	4-19
Packaging v1.1		
<b>Revision 0 (Jan 2008)</b>	This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers.	N/A
v2.2 (July 2007)	The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix".	i, ii, iii, iii, iv
	The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections.	iii, iv
	The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$ , ambient temperature, and table notes 4–6 were added.	3-2
v2.1 (May 2007)	In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz).	i
	The "Clock Conditioning Circuit (CCC) and PLL" section was updated.	i
	In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated.	ii
	Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new.	3-5

Revision	Changes	Page								
Advance v0.6 (continued)	The "Programming" section was updated to include information concerning serialization.	2-53								
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54								
	"DC and Switching Characteristics" chapter was updated with new information.	3-1								
	The A3P060 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P125 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P060 "144-Pin TQFP" pin table was updated.	4-16								
	The A3P125 "144-Pin TQFP" pin table was updated.	4-18								
	The A3P125 "208-Pin PQFP" pin table was updated.	4-21								
	The A3P400 "208-Pin PQFP" pin table was updated.	4-25								
	The A3P060 "144-Pin FBGA" pin table was updated.	4-32								
	The A3P125 "144-Pin FBGA" pin table is new.	4-34								
	The A3P400 "144-Pin FBGA" is new.	4-38								
	The A3P400 "256-Pin FBGA" was updated.	4-48								
	The A3P1000 "256-Pin FBGA" was updated.	4-54								
	The A3P400 "484-Pin FBGA" was updated.	4-58								
	The A3P1000 "484-Pin FBGA" was updated.	4-68								
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14								
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23								
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29								
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36								
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32								
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45								
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54								
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68								
Advance v0.5 (November 2005)	The "I/Os Per Package" table was updated for the following devices and packages: <table><tr><td>Device</td><td>Package</td></tr><tr><td>A3P250/M7ACP250</td><td>VQ100</td></tr><tr><td>A3P250/M7ACP250</td><td>FG144</td></tr><tr><td>A3P1000</td><td>FG256</td></tr></table>	Device	Package	A3P250/M7ACP250	VQ100	A3P250/M7ACP250	FG144	A3P1000	FG256	ii
Device	Package									
A3P250/M7ACP250	VQ100									
A3P250/M7ACP250	FG144									
A3P1000	FG256									
Advance v0.4	M7 device information is new.	N/A								
	The I/O counts in the "I/Os Per Package" table were updated.	ii								
Advance v0.3	The "I/Os Per Package" table was updated.	ii								
	M7 device information is new.	N/A								
	Table 2-4 • ProASIC3 Globals/Spines/Rows by Device was updated to include the number of rows in each top or bottom spine.	2-16								
	EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options.	2-24								

Revision	Changes	Page
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68