# Microchip Technology - A3P060-2TQ144 Datasheet

**Welcome to** E-XFL.COM

## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Obsolete |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 18432 |
| Number of I/O | 91 |
| Number of Gates | 60000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LQFP |
| Supplier Device Package | 144-TQFP (20x20) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p060-2tq144 |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges.

In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

**VCCI Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

**VCC Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

### Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

## Thermal Characteristics

### Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

$T_J$ = Junction Temperature = $\Delta T + T_A$

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

*Table 2-29 •* **I/O Output Buffer Maximum Resistances [1]**
**Applicable to Standard Plus I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| | 12 mA | 25 | 75 |
| | 16 mA | 25 | 75 |
| 3.3 V LVCMOS Wide Range[4] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| | 12 mA | 25 | 50 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| | 6 mA | 50 | 56 |
| | 8 mA | 50 | 56 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |
| | 4 mA | 100 | 112 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 25 | 75 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / IOLspec$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

*Table 2-42 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
**Commercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 10.93 | 0.04 | 1.52 | 0.43 | 10.93 | 9.46 | 3.20 | 3.32 | ns |
| | | –1 | 0.51 | 9.29 | 0.04 | 1.29 | 0.36 | 9.29 | 8.04 | 2.72 | 2.82 | ns |
| | | –2 | 0.45 | 8.16 | 0.03 | 1.13 | 0.32 | 8.16 | 7.06 | 2.39 | 2.48 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 10.93 | 0.04 | 1.52 | 0.43 | 10.93 | 9.46 | 3.20 | 3.32 | ns |
| | | –1 | 0.51 | 9.29 | 0.04 | 1.29 | 0.36 | 9.29 | 8.04 | 2.72 | 2.82 | ns |
| | | –2 | 0.45 | 8.16 | 0.03 | 1.13 | 0.32 | 8.16 | 7.06 | 2.39 | 2.48 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 6.82 | 0.04 | 1.52 | 0.43 | 6.82 | 5.70 | 3.70 | 4.16 | ns |
| | | –1 | 0.51 | 5.80 | 0.04 | 1.29 | 0.36 | 5.80 | 4.85 | 3.15 | 3.54 | ns |
| | | –2 | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 6.82 | 0.04 | 1.52 | 0.43 | 6.82 | 5.70 | 3.70 | 4.16 | ns |
| | | –1 | 0.51 | 5.80 | 0.04 | 1.29 | 0.36 | 5.80 | 4.85 | 3.15 | 3.54 | ns |
| | | –2 | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-73 •*** **1.8 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 14.80 | 0.04 | 1.20 | 0.43 | 13.49 | 14.80 | 2.25 | 1.46 | 15.73 | 17.04 | ns |
| | –1 | 0.56 | 12.59 | 0.04 | 1.02 | 0.36 | 11.48 | 12.59 | 1.91 | 1.25 | 13.38 | 14.49 | ns |
| | –2 | 0.49 | 11.05 | 0.03 | 0.90 | 0.32 | 10.08 | 11.05 | 1.68 | 1.09 | 11.75 | 12.72 | ns |
| 4 mA | Std. | 0.66 | 9.90 | 0.04 | 1.20 | 0.43 | 9.73 | 9.90 | 2.65 | 2.50 | 11.97 | 12.13 | ns |
| | –1 | 0.56 | 8.42 | 0.04 | 1.02 | 0.36 | 8.28 | 8.42 | 2.26 | 2.12 | 10.18 | 10.32 | ns |
| | –2 | 0.49 | 7.39 | 0.03 | 0.90 | 0.32 | 7.27 | 7.39 | 1.98 | 1.86 | 8.94 | 9.06 | ns |
| 6 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | –1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | –2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |
| 8 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | –1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | –2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-74 •*** **1.8 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 11.21 | 0.04 | 1.20 | 0.43 | 8.53 | 11.21 | 1.99 | 1.21 | ns |
| | –1 | 0.56 | 9.54 | 0.04 | 1.02 | 0.36 | 7.26 | 9.54 | 1.69 | 1.03 | ns |
| | –2 | 0.49 | 8.37 | 0.03 | 0.90 | 0.32 | 6.37 | 8.37 | 1.49 | 0.90 | ns |
| 4 mA | Std. | 0.66 | 6.34 | 0.04 | 1.20 | 0.43 | 5.38 | 6.34 | 2.41 | 2.48 | ns |
| | –1 | 0.56 | 5.40 | 0.04 | 1.02 | 0.36 | 4.58 | 5.40 | 2.05 | 2.11 | ns |
| | –2 | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### Timing Characteristics

***Table 2-80*** **• 1.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
|  | –1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
|  | –2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
|  | –1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
|  | –2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 6 mA | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
|  | –1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
|  | –2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 8 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
|  | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
|  | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 12 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
|  | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
|  | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Output DDR Module

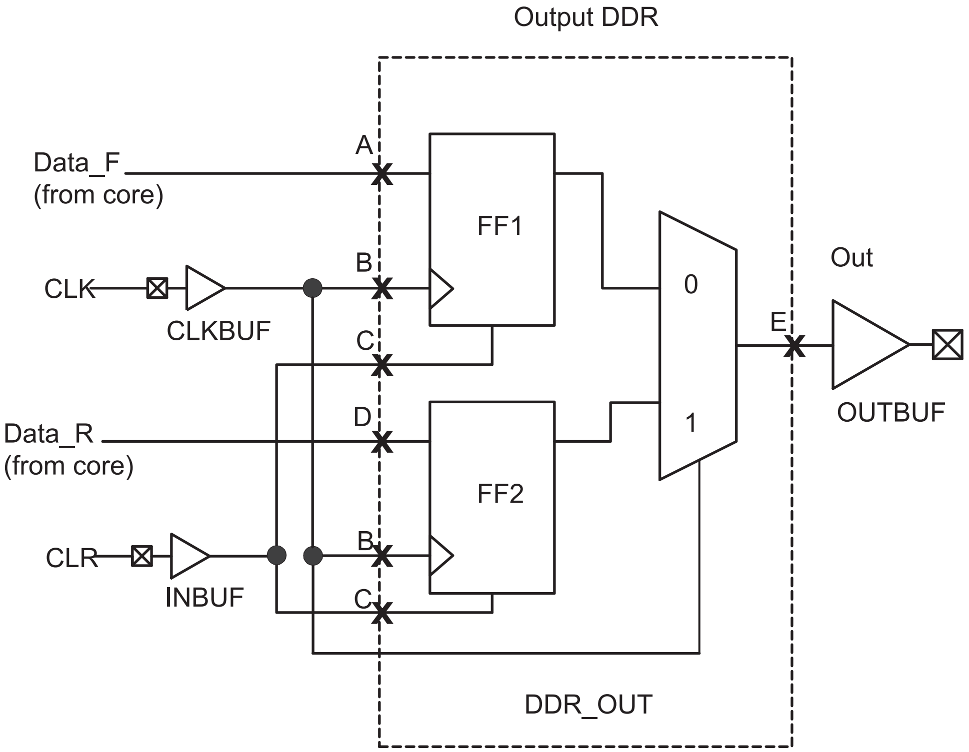


*Figure 2-22* **• Output DDR Timing Model**

***Table 2-103* • Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.

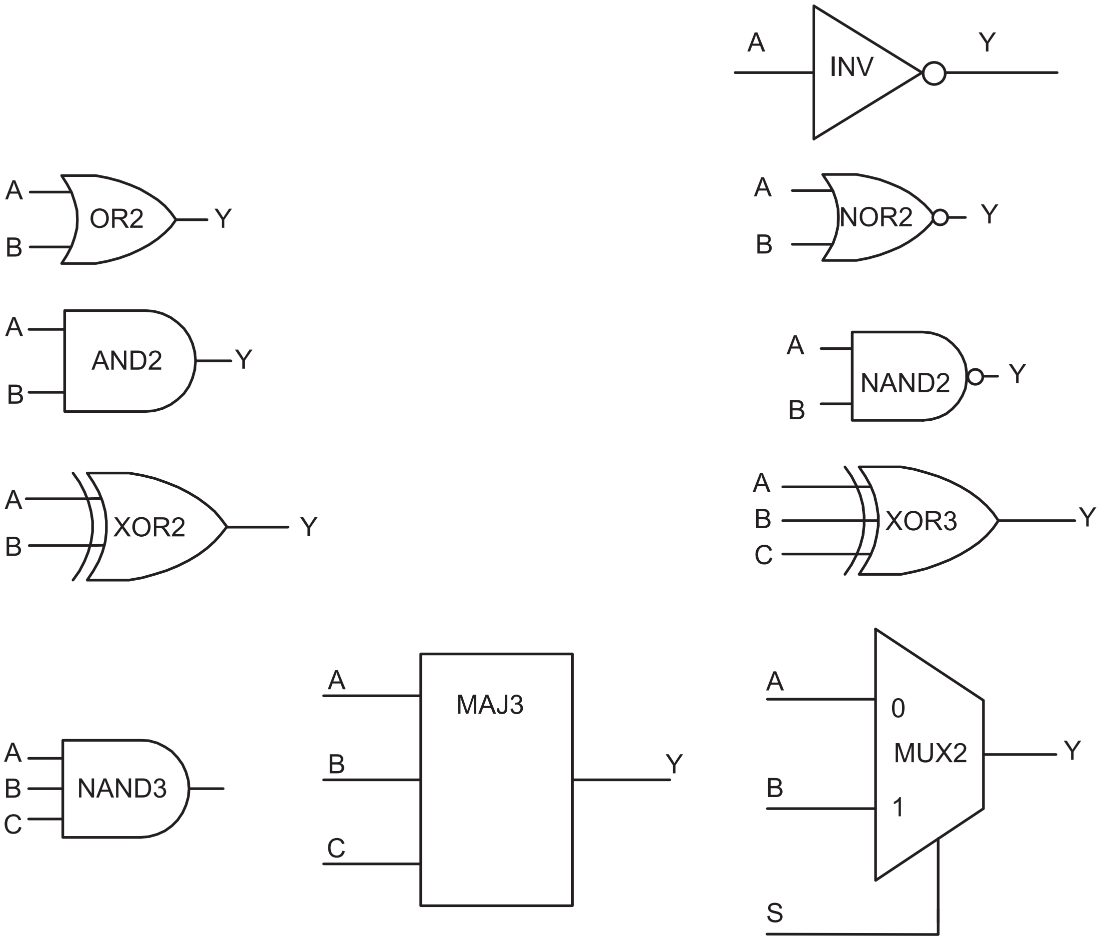


***Figure 2-24 •*** **Sample of Combinatorial Cells**

***Table 2-111* • A3P250 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.80 | 1.01 | 0.91 | 1.15 | 1.07 | 1.36 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.78 | 1.04 | 0.89 | 1.18 | 1.04 | 1.39 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-112* • A3P400 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.87 | 1.09 | 0.99 | 1.24 | 1.17 | 1.46 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.86 | 1.11 | 0.98 | 1.27 | 1.15 | 1.49 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.26 | | 0.29 | | 0.34 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

# Embedded SRAM and FIFO Characteristics

## SRAM

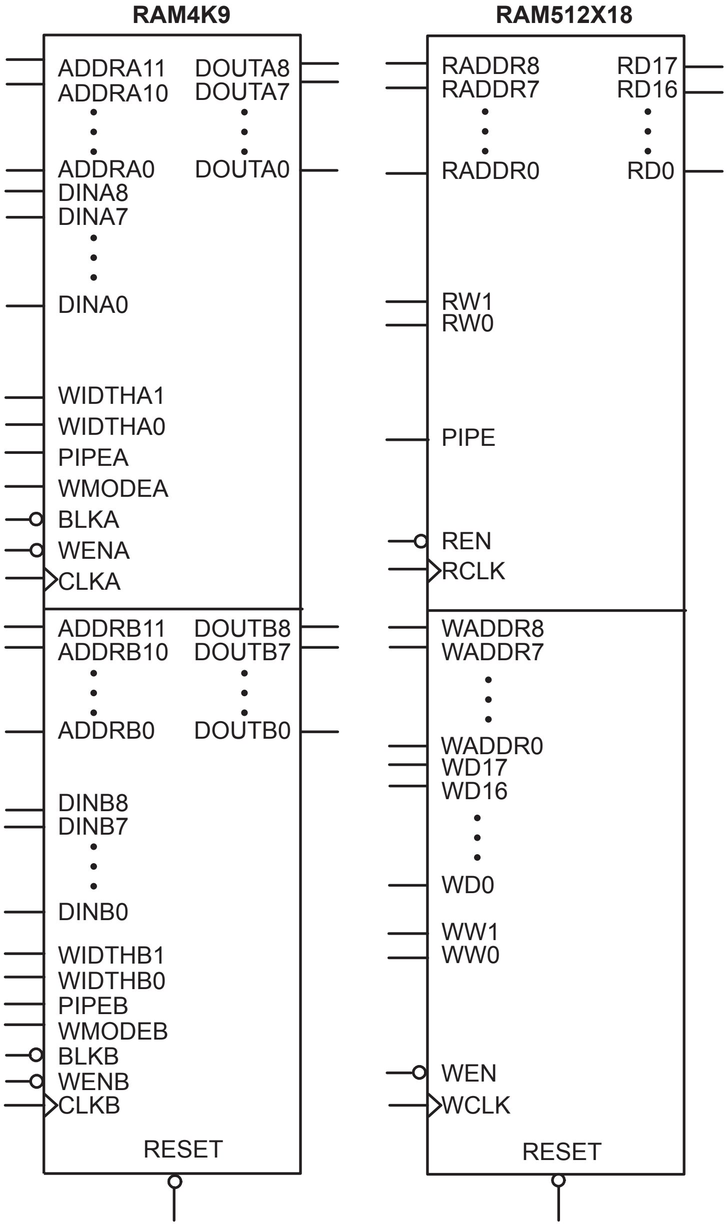


*Figure 2-30* • **RAM Models**

## Timing Characteristics

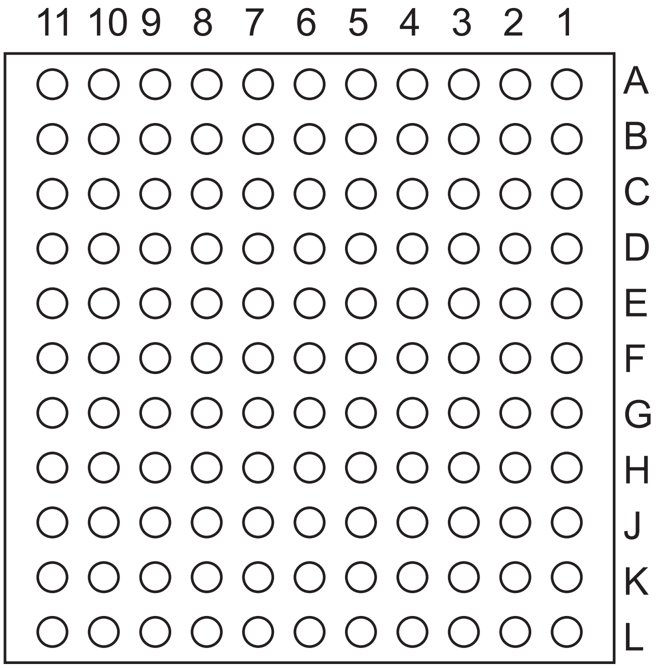
***Table 2-116* • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BLK hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.36 | 2.68 | 3.15 | ns |
|  | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 1.79 | 2.03 | 2.39 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge | 0.33 | 0.28 | 0.25 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
|  | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

# CS121 – Bottom View



*Note: The die attach paddle center of the package is tied to ground (GND).*

## Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

# PQ208 – Top View

## *Note*

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| PQ208 | |
|---|---|
| **Pin Number** | **A3P125 Function** |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO66RSB0 |
| 112 | GDA1/IO65RSB0 |
| 113 | GDB0/IO64RSB0 |
| 114 | GDB1/IO63RSB0 |
| 115 | GDC0/IO62RSB0 |
| 116 | GDC1/IO61RSB0 |
| 117 | NC |
| 118 | NC |
| 119 | NC |
| 120 | NC |
| 121 | NC |
| 122 | GND |
| 123 | VCCIB0 |
| 124 | NC |
| 125 | NC |
| 126 | VCC |
| 127 | IO60RSB0 |
| 128 | GCC2/IO59RSB0 |
| 129 | GCB2/IO58RSB0 |
| 130 | GND |
| 131 | GCA2/IO57RSB0 |
| 132 | GCA0/IO56RSB0 |
| 133 | GCA1/IO55RSB0 |
| 134 | GCB0/IO54RSB0 |
| 135 | GCB1/IO53RSB0 |
| 136 | GCC0/IO52RSB0 |
| 137 | GCC1/IO51RSB0 |
| 138 | IO50RSB0 |
| 139 | IO49RSB0 |
| 140 | VCCIB0 |
| 141 | GND |
| 142 | VCC |
| 143 | IO48RSB0 |
| 144 | IO47RSB0 |
| 145 | IO46RSB0 |
| 146 | NC |
| 147 | NC |
| 148 | NC |
| 149 | GBC2/IO45RSB0 |
| 150 | IO44RSB0 |
| 151 | GBB2/IO43RSB0 |
| 152 | IO42RSB0 |
| 153 | GBA2/IO41RSB0 |
| 154 | VMV0 |
| 155 | GNDQ |
| 156 | GND |
| 157 | NC |
| 158 | GBA1/IO40RSB0 |
| 159 | GBA0/IO39RSB0 |
| 160 | GBB1/IO38RSB0 |
| 161 | GBB0/IO37RSB0 |
| 162 | GND |
| 163 | GBC1/IO36RSB0 |
| 164 | GBC0/IO35RSB0 |
| 165 | IO34RSB0 |
| 166 | IO33RSB0 |
| 167 | IO32RSB0 |
| 168 | IO31RSB0 |
| 169 | IO30RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO29RSB0 |
| 173 | IO28RSB0 |
| 174 | IO27RSB0 |
| 175 | IO26RSB0 |
| 176 | IO25RSB0 |
| 177 | IO24RSB0 |
| 178 | GND |
| 179 | IO23RSB0 |
| 180 | IO22RSB0 |
| 181 | IO21RSB0 |
| 182 | IO20RSB0 |
| 183 | IO19RSB0 |
| 184 | IO18RSB0 |
| 185 | IO17RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO16RSB0 |
| 189 | IO15RSB0 |
| 190 | IO14RSB0 |
| 191 | IO13RSB0 |
| 192 | IO12RSB0 |
| 193 | IO11RSB0 |
| 194 | IO10RSB0 |
| 195 | GND |
| 196 | IO09RSB0 |
| 197 | IO08RSB0 |
| 198 | IO07RSB0 |
| 199 | IO06RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| 1 | GND |
| 2 | GAA2/IO174PDB3 |
| 3 | IO174NDB3 |
| 4 | GAB2/IO173PDB3 |
| 5 | IO173NDB3 |
| 6 | GAC2/IO172PDB3 |
| 7 | IO172NDB3 |
| 8 | IO171PDB3 |
| 9 | IO171NDB3 |
| 10 | IO170PDB3 |
| 11 | IO170NDB3 |
| 12 | IO169PDB3 |
| 13 | IO169NDB3 |
| 14 | IO168PDB3 |
| 15 | IO168NDB3 |
| 16 | VCC |
| 17 | GND |
| 18 | VCCIB3 |
| 19 | IO166PDB3 |
| 20 | IO166NDB3 |
| 21 | GFC1/IO164PDB3 |
| 22 | GFC0/IO164NDB3 |
| 23 | GFB1/IO163PDB3 |
| 24 | GFB0/IO163NDB3 |
| 25 | VCOMPLF |
| 26 | GFA0/IO162NPB3 |
| 27 | VCCPLF |
| 28 | GFA1/IO162PPB3 |
| 29 | GND |
| 30 | GFA2/IO161PDB3 |
| 31 | IO161NDB3 |
| 32 | GFB2/IO160PDB3 |
| 33 | IO160NDB3 |
| 34 | GFC2/IO159PDB3 |
| 35 | IO159NDB3 |
| 36 | VCC |
| 37 | IO152PDB3 |
| 38 | IO152NDB3 |
| 39 | IO150PSB3 |
| 40 | VCCIB3 |
| 41 | GND |
| 42 | IO147PDB3 |
| 43 | IO147NDB3 |
| 44 | GEC1/IO146PDB3 |
| 45 | GEC0/IO146NDB3 |
| 46 | GEB1/IO145PDB3 |
| 47 | GEB0/IO145NDB3 |
| 48 | GEA1/IO144PDB3 |
| 49 | GEA0/IO144NDB3 |
| 50 | VMV3 |
| 51 | GNDQ |
| 52 | GND |
| 53 | VMV2 |
| 54 | GEA2/IO143RSB2 |
| 55 | GEB2/IO142RSB2 |
| 56 | GEC2/IO141RSB2 |
| 57 | IO140RSB2 |
| 58 | IO139RSB2 |
| 59 | IO138RSB2 |
| 60 | IO137RSB2 |
| 61 | IO136RSB2 |
| 62 | VCCIB2 |
| 63 | IO135RSB2 |
| 64 | IO133RSB2 |
| 65 | GND |
| 66 | IO131RSB2 |
| 67 | IO129RSB2 |
| 68 | IO127RSB2 |
| 69 | IO125RSB2 |
| 70 | IO123RSB2 |
| 71 | VCC |
| 72 | VCCIB2 |
| 73 | IO120RSB2 |
| 74 | IO119RSB2 |
| 75 | IO118RSB2 |
| 76 | IO117RSB2 |
| 77 | IO116RSB2 |
| 78 | IO115RSB2 |
| 79 | IO114RSB2 |
| 80 | IO112RSB2 |
| 81 | GND |
| 82 | IO111RSB2 |
| 83 | IO110RSB2 |
| 84 | IO109RSB2 |
| 85 | IO108RSB2 |
| 86 | IO107RSB2 |
| 87 | IO106RSB2 |
| 88 | VCC |
| 89 | VCCIB2 |
| 90 | IO104RSB2 |
| 91 | IO102RSB2 |
| 92 | IO100RSB2 |
| 93 | IO98RSB2 |
| 94 | IO96RSB2 |
| 95 | IO92RSB2 |
| 96 | GDC2/IO91RSB2 |
| 97 | GND |
| 98 | GDB2/IO90RSB2 |
| 99 | GDA2/IO89RSB2 |
| 100 | GNDQ |
| 101 | TCK |
| 102 | TDI |
| 103 | TMS |
| 104 | VMV2 |
| 105 | GND |
| 106 | VPUMP |
| 107 | GNDQ |
| 108 | TDO |

| FG144 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| K1 | GEB0/IO99NDB3 |
| K2 | GEA1/IO98PDB3 |
| K3 | GEA0/IO98NDB3 |
| K4 | GEA2/IO97RSB2 |
| K5 | IO90RSB2 |
| K6 | IO84RSB2 |
| K7 | GND |
| K8 | IO66RSB2 |
| K9 | GDC2/IO63RSB2 |
| K10 | GND |
| K11 | GDA0/IO60VDB1 |
| K12 | GDB0/IO59VDB1 |
| L1 | GND |
| L2 | VMV3 |
| L3 | GEB2/IO96RSB2 |
| L4 | IO91RSB2 |
| L5 | VCCIB2 |
| L6 | IO82RSB2 |
| L7 | IO80RSB2 |
| L8 | IO72RSB2 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV2 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO95RSB2 |
| M3 | IO92RSB2 |
| M4 | IO89RSB2 |
| M5 | IO87RSB2 |
| M6 | IO85RSB2 |
| M7 | IO78RSB2 |
| M8 | IO76RSB2 |
| M9 | TDI |
| M10 | VCCIB2 |
| M11 | VPUMP |
| M12 | GNDQ |

| FG144 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO16RSB0 |
| A6 | GND |
| A7 | IO30RSB0 |
| A8 | VCC |
| A9 | IO34RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO154UDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO14RSB0 |
| B6 | IO19RSB0 |
| B7 | IO23RSB0 |
| B8 | IO31RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO154VDB3 |
| C2 | GFA2/IO144PPB3 |
| C3 | GAC2/IO153UDB3 |
| C4 | VCC |
| C5 | IO12RSB0 |
| C6 | IO17RSB0 |
| C7 | IO25RSB0 |
| C8 | IO32RSB0 |
| C9 | IO53RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| D1 | IO149NDB3 |
| D2 | IO149PDB3 |
| D3 | IO153VDB3 |
| D4 | GAA2/IO155UPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO68PPB1 |
| E1 | VCC |
| E2 | GFC0/IO147NDB3 |
| E3 | GFC1/IO147PDB3 |
| E4 | VCCIB3 |
| E5 | IO155VPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO67PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO69NDB1 |
| E12 | IO70NDB1 |
| F1 | GFB0/IO146NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO146PPB3 |
| F4 | IO144NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO67NDB1 |
| F9 | GCB0/IO68NPB1 |
| F10 | GND |
| F11 | GCA1/IO69PDB1 |
| F12 | GCA2/IO70PDB1 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| G1 | GFA1/IO145PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO145NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO77UPB1 |
| G9 | IO72NDB1 |
| G10 | GCC2/IO72PDB1 |
| G11 | IO71NDB1 |
| G12 | GCB2/IO71PDB1 |
| H1 | VCC |
| H2 | GFB2/IO143PDB3 |
| H3 | GFC2/IO142PSB3 |
| H4 | GEC1/IO137PDB3 |
| H5 | VCC |
| H6 | IO75PDB1 |
| H7 | IO75NDB1 |
| H8 | GDB2/IO81RSB2 |
| H9 | GDC0/IO77VPB1 |
| H10 | VCCIB1 |
| H11 | IO73PSB1 |
| H12 | VCC |
| J1 | GEB1/IO136PDB3 |
| J2 | IO143NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO137NDB3 |
| J5 | IO125RSB2 |
| J6 | IO116RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO80RSB2 |
| J10 | TDO |
| J11 | GDA1/IO79UDB1 |
| J12 | GDB1/IO78UDB1 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| P9 | IO98RSB2 |
| P10 | IO95RSB2 |
| P11 | IO88RSB2 |
| P12 | IO84RSB2 |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO79VDB1 |
| R1 | GEA1/IO135PDB3 |
| R2 | GEA0/IO135NDB3 |
| R3 | IO127RSB2 |
| R4 | GEC2/IO132RSB2 |
| R5 | IO123RSB2 |
| R6 | IO118RSB2 |
| R7 | IO112RSB2 |
| R8 | IO106RSB2 |
| R9 | IO100RSB2 |
| R10 | IO96RSB2 |
| R11 | IO89RSB2 |
| R12 | IO85RSB2 |
| R13 | GDB2/IO81RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO126RSB2 |
| T3 | GEB2/IO133RSB2 |
| T4 | IO124RSB2 |
| T5 | IO116RSB2 |
| T6 | IO113RSB2 |
| T7 | IO107RSB2 |
| T8 | IO105RSB2 |
| T9 | IO102RSB2 |
| T10 | IO97RSB2 |
| T11 | IO92RSB2 |
| T12 | GDC2/IO82RSB2 |
| T13 | IO86RSB2 |
| T14 | GDA2/IO80RSB2 |
| T15 | TMS |
| T16 | GND |

| FG256 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| G13 | GCC1/IO69PPB1 |
| G14 | IO65NPB1 |
| G15 | IO75PDB1 |
| G16 | IO75NDB1 |
| H1 | GFB0/IO163NPB3 |
| H2 | GFA0/IO162NDB3 |
| H3 | GFB1/IO163PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO164NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO69NPB1 |
| H13 | GCB1/IO70PPB1 |
| H14 | GCA0/IO71NPB1 |
| H15 | IO67NPB1 |
| H16 | GCB0/IO70NPB1 |
| J1 | GFA2/IO161PPB3 |
| J2 | GFA1/IO162PDB3 |
| J3 | VCCPLF |
| J4 | IO160NDB3 |
| J5 | GFB2/IO160PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO73PPB1 |
| J13 | GCA1/IO71PPB1 |
| J14 | GCC2/IO74PPB1 |
| J15 | IO80PPB1 |
| J16 | GCA2/IO72PDB1 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| K1 | GFC2/IO159PDB3 |
| K2 | IO161NPB3 |
| K3 | IO156PPB3 |
| K4 | IO129RSB2 |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO73NPB1 |
| K14 | IO80NPB1 |
| K15 | IO74NPB1 |
| K16 | IO72NDB1 |
| L1 | IO159NDB3 |
| L2 | IO156NPB3 |
| L3 | IO151PPB3 |
| L4 | IO158PSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO87NPB1 |
| L14 | IO85NDB1 |
| L15 | IO85PDB1 |
| L16 | IO84PDB1 |
| M1 | IO150PDB3 |
| M2 | IO151NPB3 |
| M3 | IO147NPB3 |
| M4 | GEC0/IO146NPB3 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | IO117RSB2 |
| M9 | IO110RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | IO94RSB2 |
| M14 | GDB1/IO87PPB1 |
| M15 | GDC1/IO86PDB1 |
| M16 | IO84NDB1 |
| N1 | IO150NDB3 |
| N2 | IO147PPB3 |
| N3 | GEC1/IO146PPB3 |
| N4 | IO140RSB2 |
| N5 | GNDQ |
| N6 | GEA2/IO143RSB2 |
| N7 | IO126RSB2 |
| N8 | IO120RSB2 |
| N9 | IO108RSB2 |
| N10 | IO103RSB2 |
| N11 | IO99RSB2 |
| N12 | GNDQ |
| N13 | IO92RSB2 |
| N14 | VJTAG |
| N15 | GDC0/IO86NDB1 |
| N16 | GDA1/IO88PDB1 |
| P1 | GEB1/IO145PDB3 |
| P2 | GEB0/IO145NDB3 |
| P3 | VMV2 |
| P4 | IO138RSB2 |
| P5 | IO136RSB2 |
| P6 | IO131RSB2 |
| P7 | IO124RSB2 |
| P8 | IO119RSB2 |

| Revision | Changes | Page |
|---|---|---|
| Revision 13 (January 2013) | The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104). | 1-IV |
| | Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C. | 2-2 |
| | The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569). | 2-90 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284).<br>Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The Security section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-1 |
| | Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321). | 2-1<br>2-2 |
| | Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933). | 2-31 |
| | In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549). | 2-68 |
| | Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371). | 2-99 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |