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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg144i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The absolute maximum junction temperature is 100°C. EQ 1 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°C) - \text{Max. ambient temp. } (°C)}{\theta_{ja}(°C/W)} = \frac{100°C - 70°C}{20.5°C/W} = 1.463\ W$$

EQ 1

Table 2-5 • **Package Thermal Resistivities**

Package Type	Device	Pin Count	θ_{jc}	θ_{ja} Still Air	θ_{ja} 200 ft/min	θ_{ja} 500 ft/min	Units
Quad Flat No Lead	A3P030	132	0.4	21.4	16.8	15.3	°C/W
	A3P060	132	0.3	21.2	16.6	15.0	°C/W
	A3P125	132	0.2	21.1	16.5	14.9	°C/W
	A3P250	132	0.1	21.0	16.4	14.8	°C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Thin Quad Flat Pack (TQFP)	All devices	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)	All devices	208	8.0	26.1	22.5	20.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

Note: *This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.*

Temperature and Voltage Derating Factors

Table 2-6 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)**

Array Voltage VCC (V)	Junction Temperature (°C) –40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.88	0.93	0.95	1.00	1.02	1.04
1.500	0.83	0.88	0.90	0.95	0.96	0.98
1.575	0.80	0.84	0.87	0.91	0.93	0.94

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1] mA	IOH[1] mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	4	4
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
–2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case VCC = 1.425 V, Worst-Case VCCI (per standard)
Standard I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
3.3 V LVCMOS Wide Range[2]	100 µA	8 mA	High	35	–	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns
2.5 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
1.8 V LVCMOS	4 mA	4 mA	High	35	–	0.45	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns
1.5 V LVCMOS	2 mA	2 mA	High	35	–	0.45	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-43 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	–1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	–2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
4 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	–1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	–2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
6 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	–1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	–2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
8 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	–1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	–2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
12 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	–1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	–2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
16 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	–1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	–2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-81 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-82 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

Table 2-88 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	ns
–1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	ns
–2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-89 • **3.3 V PCI/PCI-X**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.31	0.04	0.85	0.43	2.35	1.70	2.79	3.22	4.59	3.94	ns
–1	0.56	1.96	0.04	0.72	0.36	2.00	1.45	2.37	2.74	3.90	3.35	ns
–2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

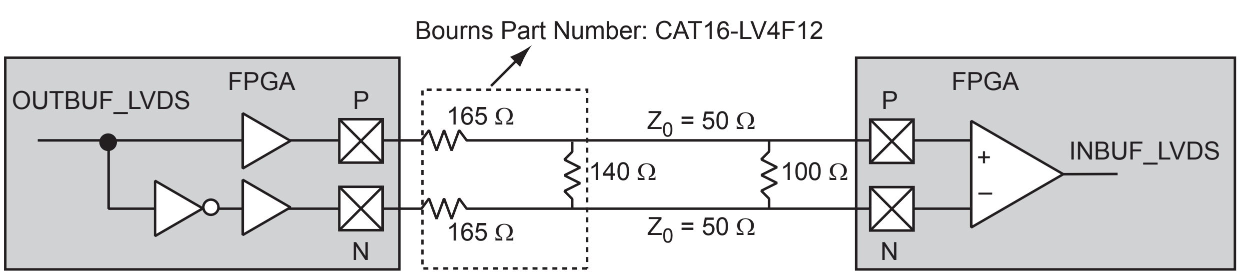


Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-97 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

*Note: *See Figure 2-16 on page 2-71 for more information.*

Timing Characteristics

Table 2-105 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

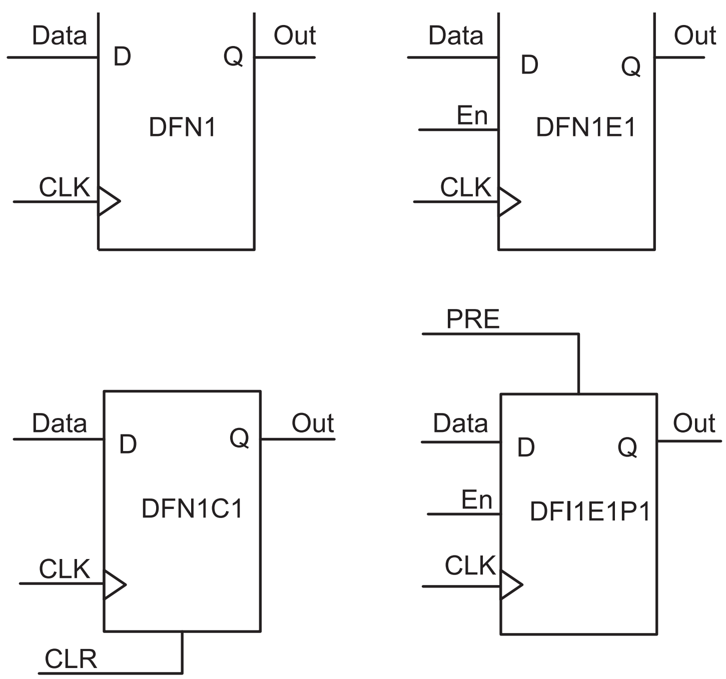
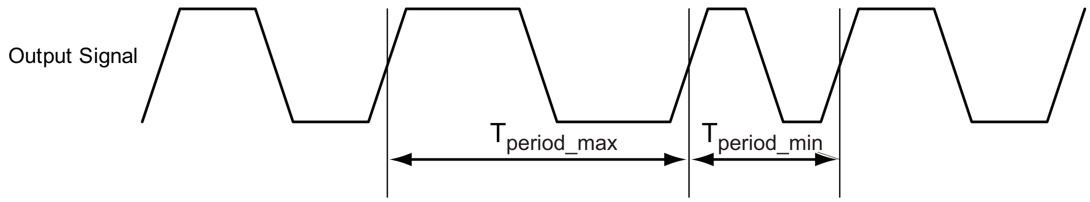


Figure 2-26 • **Sample of Sequential Cells**



Note: *Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.*

Figure 2-29 • **Peak-to-Peak Jitter Definition**

Table 2-123 • A3P250 FIFO 4k×1 (continued)
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Embedded FlashROM Characteristics

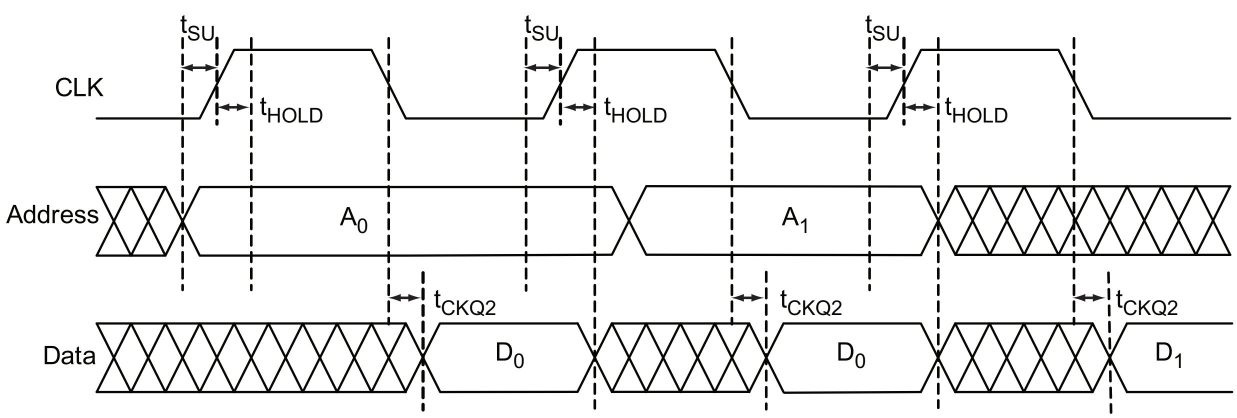


Figure 2-44 • Timing Diagram

Timing Characteristics

Table 2-124 • Embedded FlashROM Access Time

Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	21.42	24.40	28.68	ns
F_{MAX}	Maximum Clock Frequency	15	15	15	MHz

3 – Pin Descriptions

Supply Pins

GND Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on ProASIC3 devices.

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC3 devices.

QN132	
Pin Number	A3P125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	A3P125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	A3P125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

TQ144	
Pin Number	**A3P060 Function**
1	GAA2/IO51RSB1
2	IO52RSB1
3	GAB2/IO53RSB1
4	IO95RSB1
5	GAC2/IO94RSB1
6	IO93RSB1
7	IO92RSB1
8	IO91RSB1
9	VCC
10	GND
11	VCCIB1
12	IO90RSB1
13	GFC1/IO89RSB1
14	GFC0/IO88RSB1
15	GFB1/IO87RSB1
16	GFB0/IO86RSB1
17	VCOMPLF
18	GFA0/IO85RSB1
19	VCCPLF
20	GFA1/IO84RSB1
21	GFA2/IO83RSB1
22	GFB2/IO82RSB1
23	GFC2/IO81RSB1
24	IO80RSB1
25	IO79RSB1
26	IO78RSB1
27	GND
28	VCCIB1
29	GEC1/IO77RSB1
30	GEC0/IO76RSB1
31	GEB1/IO75RSB1
32	GEB0/IO74RSB1
33	GEA1/IO73RSB1
34	GEA0/IO72RSB1
35	VMV1
36	GNDQ

TQ144	
Pin Number	**A3P060 Function**
37	NC
38	GEA2/IO71RSB1
39	GEB2/IO70RSB1
40	GEC2/IO69RSB1
41	IO68RSB1
42	IO67RSB1
43	IO66RSB1
44	IO65RSB1
45	VCC
46	GND
47	VCCIB1
48	NC
49	IO64RSB1
50	NC
51	IO63RSB1
52	NC
53	IO62RSB1
54	NC
55	IO61RSB1
56	NC
57	NC
58	IO60RSB1
59	IO59RSB1
60	IO58RSB1
61	IO57RSB1
62	NC
63	GND
64	NC
65	GDC2/IO56RSB1
66	GDB2/IO55RSB1
67	GDA2/IO54RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1

TQ144	
Pin Number	**A3P060 Function**
73	VPUMP
74	NC
75	TDO
76	TRST
77	VJTAG
78	GDA0/IO50RSB0
79	GDB0/IO48RSB0
80	GDB1/IO47RSB0
81	VCCIB0
82	GND
83	IO44RSB0
84	GCC2/IO43RSB0
85	GCB2/IO42RSB0
86	GCA2/IO41RSB0
87	GCA0/IO40RSB0
88	GCA1/IO39RSB0
89	GCB0/IO38RSB0
90	GCB1/IO37RSB0
91	GCC0/IO36RSB0
92	GCC1/IO35RSB0
93	IO34RSB0
94	IO33RSB0
95	NC
96	NC
97	NC
98	VCCIB0
99	GND
100	VCC
101	IO30RSB0
102	GBC2/IO29RSB0
103	IO28RSB0
104	GBB2/IO27RSB0
105	IO26RSB0
106	GBA2/IO25RSB0
107	VMV0
108	GNDQ

PQ208	
Pin Number	A3P600 Function
1	GND
2	GAA2/IO174PDB3
3	IO174NDB3
4	GAB2/IO173PDB3
5	IO173NDB3
6	GAC2/IO172PDB3
7	IO172NDB3
8	IO171PDB3
9	IO171NDB3
10	IO170PDB3
11	IO170NDB3
12	IO169PDB3
13	IO169NDB3
14	IO168PDB3
15	IO168NDB3
16	VCC
17	GND
18	VCCIB3
19	IO166PDB3
20	IO166NDB3
21	GFC1/IO164PDB3
22	GFC0/IO164NDB3
23	GFB1/IO163PDB3
24	GFB0/IO163NDB3
25	VCOMPLF
26	GFA0/IO162NPB3
27	VCCPLF
28	GFA1/IO162PPB3
29	GND
30	GFA2/IO161PDB3
31	IO161NDB3
32	GFB2/IO160PDB3
33	IO160NDB3
34	GFC2/IO159PDB3
35	IO159NDB3
36	VCC

PQ208	
Pin Number	A3P600 Function
37	IO152PDB3
38	IO152NDB3
39	IO150PSB3
40	VCCIB3
41	GND
42	IO147PDB3
43	IO147NDB3
44	GEC1/IO146PDB3
45	GEC0/IO146NDB3
46	GEB1/IO145PDB3
47	GEB0/IO145NDB3
48	GEA1/IO144PDB3
49	GEA0/IO144NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO143RSB2
55	GEB2/IO142RSB2
56	GEC2/IO141RSB2
57	IO140RSB2
58	IO139RSB2
59	IO138RSB2
60	IO137RSB2
61	IO136RSB2
62	VCCIB2
63	IO135RSB2
64	IO133RSB2
65	GND
66	IO131RSB2
67	IO129RSB2
68	IO127RSB2
69	IO125RSB2
70	IO123RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P600 Function
73	IO120RSB2
74	IO119RSB2
75	IO118RSB2
76	IO117RSB2
77	IO116RSB2
78	IO115RSB2
79	IO114RSB2
80	IO112RSB2
81	GND
82	IO111RSB2
83	IO110RSB2
84	IO109RSB2
85	IO108RSB2
86	IO107RSB2
87	IO106RSB2
88	VCC
89	VCCIB2
90	IO104RSB2
91	IO102RSB2
92	IO100RSB2
93	IO98RSB2
94	IO96RSB2
95	IO92RSB2
96	GDC2/IO91RSB2
97	GND
98	GDB2/IO90RSB2
99	GDA2/IO89RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG144	
Pin Number	A3P400 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO30RSB0
A8	VCC
A9	IO34RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO154UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO23RSB0
B8	IO31RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO154VDB3
C2	GFA2/IO144PPB3
C3	GAC2/IO153UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO25RSB0
C8	IO32RSB0
C9	IO53RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1
D1	IO149NDB3
D2	IO149PDB3
D3	IO153VDB3
D4	GAA2/IO155UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO68PPB1
E1	VCC
E2	GFC0/IO147NDB3
E3	GFC1/IO147PDB3
E4	VCCIB3
E5	IO155VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO67PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO69NDB1
E12	IO70NDB1
F1	GFB0/IO146NPB3
F2	VCOMPLF
F3	GFB1/IO146PPB3
F4	IO144NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO67NDB1
F9	GCB0/IO68NPB1
F10	GND
F11	GCA1/IO69PDB1
F12	GCA2/IO70PDB1
G1	GFA1/IO145PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO145NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO77UPB1
G9	IO72NDB1
G10	GCC2/IO72PDB1
G11	IO71NDB1
G12	GCB2/IO71PDB1
H1	VCC
H2	GFB2/IO143PDB3
H3	GFC2/IO142PSB3
H4	GEC1/IO137PDB3
H5	VCC
H6	IO75PDB1
H7	IO75NDB1
H8	GDB2/IO81RSB2
H9	GDC0/IO77VPB1
H10	VCCIB1
H11	IO73PSB1
H12	VCC
J1	GEB1/IO136PDB3
J2	IO143NDB3
J3	VCCIB3
J4	GEC0/IO137NDB3
J5	IO125RSB2
J6	IO116RSB2
J7	VCC
J8	TCK
J9	GDA2/IO80RSB2
J10	TDO
J11	GDA1/IO79UDB1
J12	GDB1/IO78UDB1

FG144	
Pin Number	A3P1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	**A3P1000 Function**
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P400 Function
R17	GDB1/IO78UPB1
R18	GDC1/IO77UDB1
R19	IO75NDB1
R20	VCC
R21	NC
R22	NC
T1	NC
T2	NC
T3	NC
T4	IO140NDB3
T5	IO138PPB3
T6	GEC1/IO137PPB3
T7	IO131RSB2
T8	GNDQ
T9	GEA2/IO134RSB2
T10	IO117RSB2
T11	IO111RSB2
T12	IO99RSB2
T13	IO94RSB2
T14	IO87RSB2
T15	GNDQ
T16	IO93RSB2
T17	VJTAG
T18	GDC0/IO77VDB1
T19	GDA1/IO79UDB1
T20	NC
T21	NC
T22	NC
U1	NC
U2	NC
U3	NC
U4	GEB1/IO136PDB3
U5	GEB0/IO136NDB3
U6	VMV2
U7	IO129RSB2
U8	IO128RSB2

FG484	
Pin Number	A3P400 Function
U9	IO122RSB2
U10	IO115RSB2
U11	IO110RSB2
U12	IO98RSB2
U13	IO95RSB2
U14	IO88RSB2
U15	IO84RSB2
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO79VDB1
U20	NC
U21	NC
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO135PDB3
V5	GEA0/IO135NDB3
V6	IO127RSB2
V7	GEC2/IO132RSB2
V8	IO123RSB2
V9	IO118RSB2
V10	IO112RSB2
V11	IO106RSB2
V12	IO100RSB2
V13	IO96RSB2
V14	IO89RSB2
V15	IO85RSB2
V16	GDB2/IO81RSB2
V17	TDI
V18	NC
V19	TDO
V20	GND
V21	NC
V22	NC

FG484	
Pin Number	A3P400 Function
W1	NC
W2	NC
W3	NC
W4	GND
W5	IO126RSB2
W6	GEB2/IO133RSB2
W7	IO124RSB2
W8	IO116RSB2
W9	IO113RSB2
W10	IO107RSB2
W11	IO105RSB2
W12	IO102RSB2
W13	IO97RSB2
W14	IO92RSB2
W15	GDC2/IO82RSB2
W16	IO86RSB2
W17	GDA2/IO80RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	NC
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC

Revision	Changes	Page
Revision 5 (Aug 2008) DC and Switching Characteristics v1.3	TJ, Maximum Junction Temperature, was changed to 100° from 110º in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.	2-6
	Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics.	2-7
	Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new.	2-11, 2-12
	The "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	Both fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 • Input DDR Propagation Delays.	2-78
	Table 2-107 • A3P015 Global Resource is new.	2-86
	The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
Revision 4 (Jun 2008) DC and Switching Characteristics v1.2	Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed.	2-2
	The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power.	2-7
	Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X.	2-27
	Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-66
Revision 3 (Jun 2008) Packaging v1.3	Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram.	4-3
	The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
Revision 2 (Feb 2008) Product Brief v1.0	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Flash Family FPGAs" "A3P015 and A3P030" note Introduction and Overview (NA)	N/A