

Welcome to [E-XFL.COM](#)

### Understanding **Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg256">https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fg256</a>

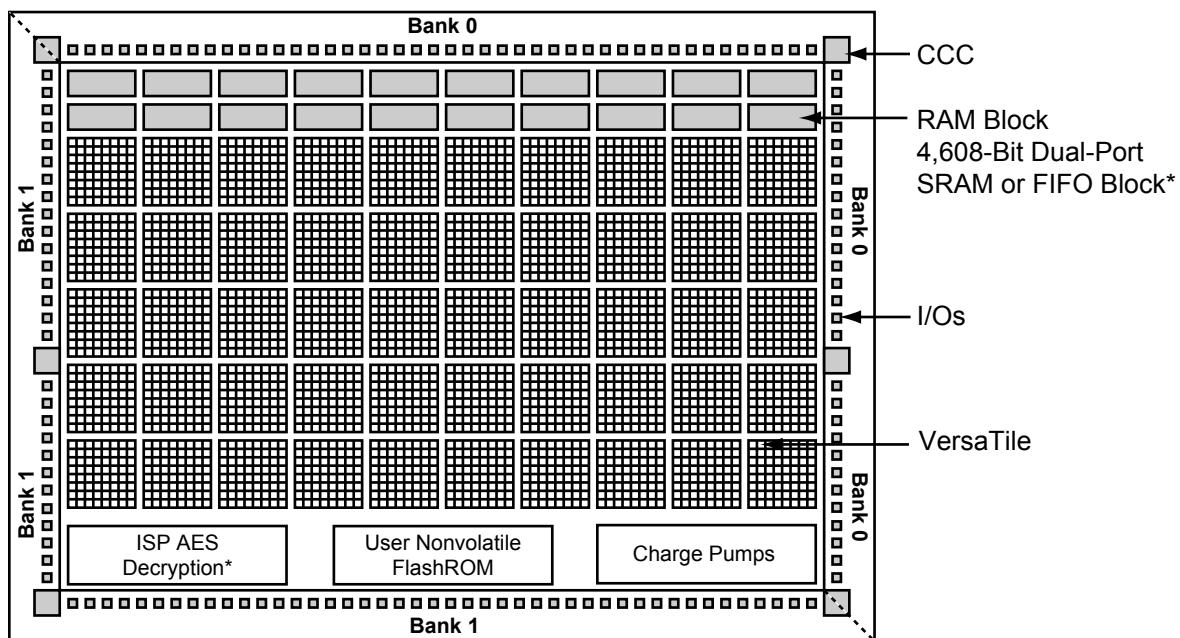
## Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features ([Figure 1-1](#) and [Figure 1-2 on page 1-4](#)):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory<sup>†</sup>
- Extensive CCCs and PLLs<sup>†</sup>
- Advanced I/O structure



*Note:* \*Not supported by A3P015 and A3P030 devices

**Figure 1-1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)**

<sup>†</sup> The A3P015 and A3P030 do not support PLL or SRAM.

## User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

**Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings**

–2 Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst Case VCC = 1.425 V,  
 Worst-Case VCCI (per standard)  
 Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor	t <sub>DOUT</sub> (ns)	t <sub>DP</sub> (ns)	t <sub>DIN</sub> (ns)	t <sub>PR</sub> (ns)	t <sub>EOUT</sub> (ns)	t <sub>ZL</sub> (ns)	t <sub>ZH</sub> (ns)	t <sub>LZ</sub> (ns)	t <sub>HZ</sub> (ns)	t <sub>ZLs</sub> (ns)	t <sub>ZHs</sub> (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 µA	12 mA	High	35	–	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns
1.8 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
1.5 V LVCMOS	4 mA	4 mA	High	35	–	0.45	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>4</sup>	0.45	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>4</sup>	0.45	1.72	0.03	0.62	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-64](#) for connectivity. This resistor is not required during normal operation.

## Timing Characteristics

**Table 2-41 • 3.3 V LVTTL / 3.3 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
4 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	-1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	-2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	-1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	-2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	-1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	-2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

### 3.3 V LVC MOS Wide Range

**Table 2-47 • Minimum and Maximum DC Input and Output Levels  
Applicable to Advanced I/O Banks**

3.3 V LVC MOS Wide Range	Equiv. Software Default Drive Strength Option <sup>1</sup>	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
		Min V	Max V	Min V	Max V								
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	25	27	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	25	27	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	51	54	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	51	54	10	10
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	103	109	10	10
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	132	127	10	10
100 μA	24 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	268	181	10	10

**Notes:**

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 85°C junction temperature.
5. All LVMCOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.
6. Software default selection highlighted in gray.

**Table 2-48 • Minimum and Maximum DC Input and Output Levels  
Applicable to Standard Plus I/O Banks**

3.3 V LVC MOS Wide Range	Equiv. Software Default Drive Strength Option <sup>1</sup>	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
		Min V	Max V	Min V	Max V								
100 μA	2 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	25	27	10	10
100 μA	4 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	25	27	10	10
100 μA	6 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	51	54	10	10
100 μA	8 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	51	54	10	10
100 μA	12 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	103	109	10	10
100 μA	16 mA	-0.3	0.8	2	3.6	0.2	VDD - 0.2	100	100	103	109	10	10

**Notes:**

1. The minimum drive strength for any LVC MOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
4. Currents are measured at 85°C junction temperature.
5. All LVMCOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.
6. Software default selection highlighted in gray.

## 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

**Table 2-66 • Minimum and Maximum DC Input and Output Levels  
Applicable to Advanced I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA <sup>3</sup>	Max mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI - 0.45	16	16	74	91	10	10

*Notes:*

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature ( $100^\circ\text{C}$  junction temperature) and maximum voltage.
4. Currents are measured at  $85^\circ\text{C}$  junction temperature.
5. Software default selection highlighted in gray.

**Table 2-67 • Minimum and Maximum DC Input and Output Levels  
Applicable to Standard Plus I/O I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA <sup>3</sup>	Max mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	8	8	44	35	10	10

*Notes:*

1. *IIL* is the input leakage current per I/O pin over recommended operation conditions where  $-0.3 \text{ V} < \text{VIN} < \text{VIL}$ .
2. *IIH* is the input leakage current per I/O pin over recommended operating conditions  $\text{VIH} < \text{VIN} < \text{VCCI}$ . Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature ( $100^\circ\text{C}$  junction temperature) and maximum voltage.
4. Currents are measured at  $85^\circ\text{C}$  junction temperature.
5. Software default selection highlighted in gray.

**Table 2-93 • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

**Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: \*Measuring point =  $V_{trip}$ . See [Table 2-22 on page 2-22](#) for a complete table of trip points.

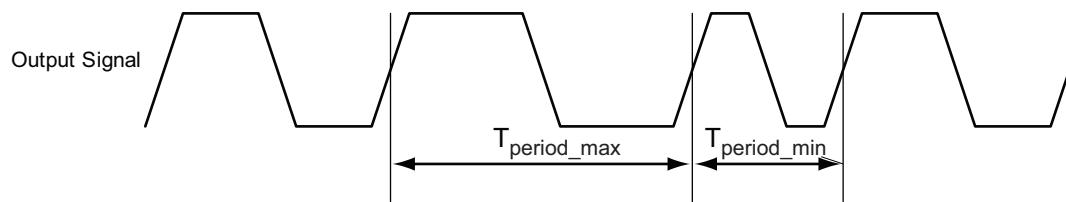
### Timing Characteristics

**Table 2-95 • LVPECL**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	Units
Std.	0.66	1.80	0.04	1.40	ns
-1	0.56	1.53	0.04	1.19	ns
-2	0.49	1.34	0.03	1.05	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.



*Note:* Peak-to-peak jitter measurements are defined by  $T_{peak-to-peak} = T_{period\_max} - T_{period\_min}$ .

**Figure 2-29 • Peak-to-Peak Jitter Definition**

## Embedded SRAM and FIFO Characteristics

### SRAM

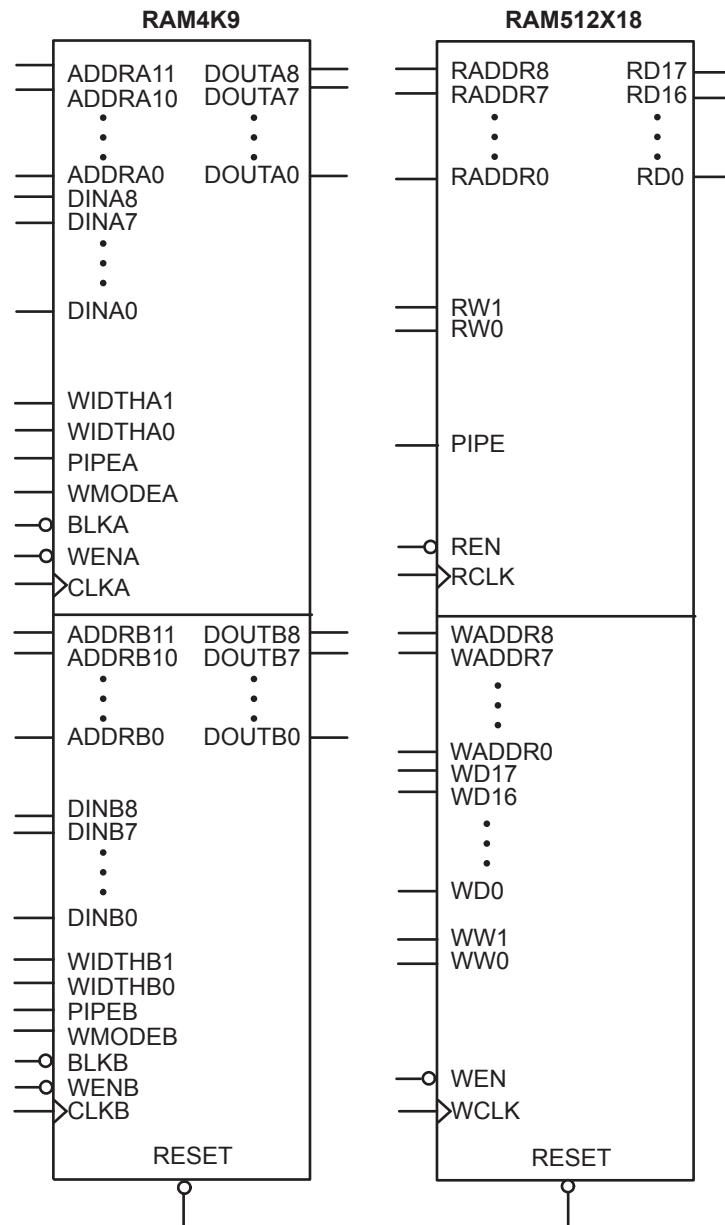


Figure 2-30 • RAM Models

**Table 2-120 • A3P250 FIFO 512×8**  
**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $V_{CC} = 1.425 \text{ V}$**

Parameter	Description	-2	-1	Std.	Units
$t_{ENS}$	REN, WEN Setup Time	3.75	4.27	5.02	ns
$t_{ENH}$	REN, WEN Hold Time	0.00	0.00	0.00	ns
$t_{BKS}$	BLK Setup Time	0.19	0.22	0.26	ns
$t_{BKH}$	BLK Hold Time	0.00	0.00	0.00	ns
$t_{DS}$	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
$t_{DH}$	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
$t_{CKQ1}$	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
$t_{CKQ2}$	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
$t_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
$t_{RSTFG}$	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
$t_{RSTAF}$	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
$t_{RSTBQ}$	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
$t_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	ns
$F_{MAX}$	Maximum Frequency for FIFO	310	272	231	MHz

**Table 2-122 • A3P250 FIFO 2k×2**  
**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , VCC = 1.425 V**

Parameter	Description	-2	-1	Std.	Units
$t_{ENS}$	REN, WEN Setup Time	4.39	5.00	5.88	ns
$t_{ENH}$	REN, WEN Hold Time	0.00	0.00	0.00	ns
$t_{BKS}$	BLK Setup Time	0.19	0.22	0.26	ns
$t_{BKH}$	BLK Hold Time	0.00	0.00	0.00	ns
$t_{DS}$	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
$t_{DH}$	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
$t_{CKQ1}$	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
$t_{CKQ2}$	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
$t_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
$t_{RSTFG}$	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
$t_{RSTAF}$	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
$t_{RSTBQ}$	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
$t_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	ns
$F_{MAX}$	Maximum Frequency for FIFO	310	272	231	MHz

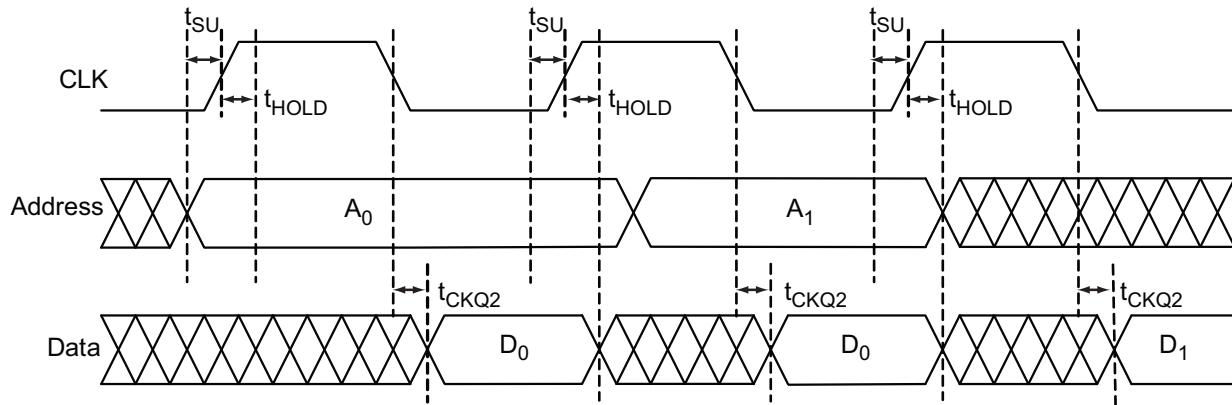
**Table 2-123 • A3P250 FIFO 4k×1**  
**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , VCC = 1.425 V**

Parameter	Description	-2	-1	Std.	Units
$t_{ENS}$	REN, WEN Setup Time	4.86	5.53	6.50	ns
$t_{ENH}$	REN, WEN Hold Time	0.00	0.00	0.00	ns
$t_{BKS}$	BLK Setup Time	0.19	0.22	0.26	ns
$t_{BKH}$	BLK Hold Time	0.00	0.00	0.00	ns
$t_{DS}$	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
$t_{DH}$	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
$t_{CKQ1}$	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
$t_{CKQ2}$	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
$t_{RCKEF}$	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
$t_{WCKFF}$	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
$t_{CKAF}$	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
$t_{RSTFG}$	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns

**Table 2-123 • A3P250 FIFO 4k×1 (continued)**  
**Worst Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , VCC = 1.425 V**

Parameter	Description	-2	-1	Std.	Units
$t_{RSTAF}$	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
$t_{RSTBQ}$	RESET Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
$t_{CYC}$	Clock Cycle Time	3.23	3.68	4.32	ns
$F_{MAX}$	Maximum Frequency	310	272	231	MHz

## Embedded FlashROM Characteristics



**Figure 2-44 • Timing Diagram**

### Timing Characteristics

**Table 2-124 • Embedded FlashROM Access Time**

Parameter	Description	-2	-1	Std.	Units
$t_{SU}$	Address Setup Time	0.53	0.61	0.71	ns
$t_{HOLD}$	Address Hold Time	0.00	0.00	0.00	ns
$t_{CKQ2}$	Clock to Out	21.42	24.40	28.68	ns
$F_{MAX}$	Maximum Clock Frequency	15	15	15	MHz

VQ100	
Pin Number	A3P030 Function
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	VCC
18	VCCIB1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1

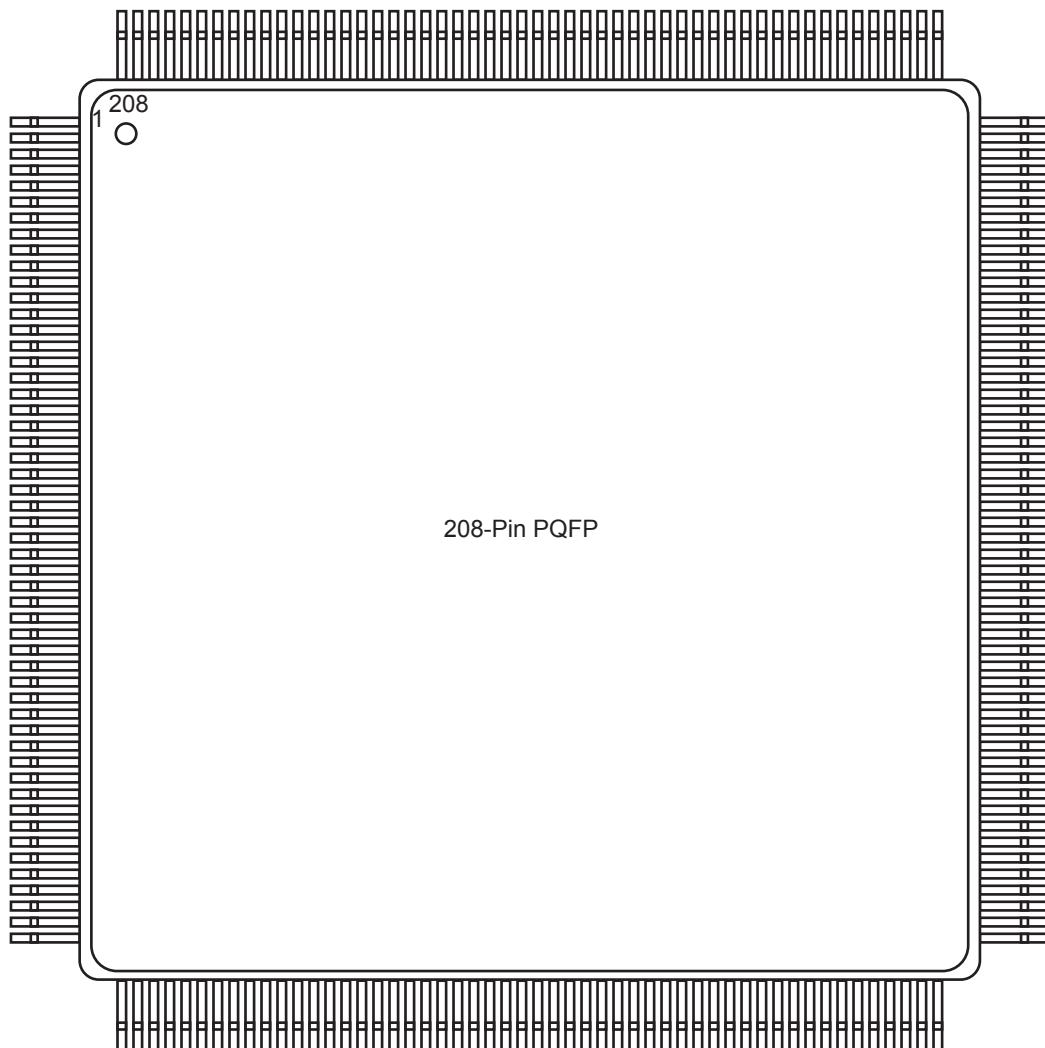
VQ100	
Pin Number	A3P030 Function
37	VCC
38	GND
39	VCCIB1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0

VQ100	
Pin Number	A3P030 Function
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	VCCIB0
88	GND
89	VCC
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

TQ144	
Pin Number	A3P125 Function
109	GBA1/IO40RSB0
110	GBA0/IO39RSB0
111	GBB1/IO38RSB0
112	GBB0/IO37RSB0
113	GBC1/IO36RSB0
114	GBC0/IO35RSB0
115	IO34RSB0
116	IO33RSB0
117	VCCIB0
118	GND
119	VCC
120	IO29RSB0
121	IO28RSB0
122	IO27RSB0
123	IO25RSB0
124	IO23RSB0
125	IO21RSB0
126	IO19RSB0
127	IO17RSB0
128	IO16RSB0
129	IO14RSB0
130	IO12RSB0
131	IO10RSB0
132	IO08RSB0
133	IO06RSB0
134	VCCIB0
135	GND
136	VCC
137	GAC1/IO05RSB0
138	GAC0/IO04RSB0
139	GAB1/IO03RSB0
140	GAB0/IO02RSB0
141	GAA1/IO01RSB0
142	GAA0/IO00RSB0
143	GNDQ
144	VMV0

## PQ208 – Top View

---



---

### Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO30RSB0
A8	VCC
A9	IO34RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO154UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO23RSB0
B8	IO31RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO154VDB3
C2	GFA2/IO144PPB3
C3	GAC2/IO153UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO25RSB0
C8	IO32RSB0
C9	IO53RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
D1	IO149NDB3
D2	IO149PDB3
D3	IO153VDB3
D4	GAA2/IO155UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO68PPB1
E1	VCC
E2	GFC0/IO147NDB3
E3	GFC1/IO147PDB3
E4	VCCIB3
E5	IO155VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO67PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO69NDB1
E12	IO70NDB1
F1	GFB0/IO146NPB3
F2	VCOMPLF
F3	GFB1/IO146PPB3
F4	IO144NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO67NDB1
F9	GCB0/IO68NPB1
F10	GND
F11	GCA1/IO69PDB1
F12	GCA2/IO70PDB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
G1	GFA1/IO145PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO145NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO77UPB1
G9	IO72NDB1
G10	GCC2/IO72PDB1
G11	IO71NDB1
G12	GCB2/IO71PDB1
H1	VCC
H2	GFB2/IO143PDB3
H3	GFC2/IO142PSB3
H4	GEC1/IO137PDB3
H5	VCC
H6	IO75PDB1
H7	IO75NDB1
H8	GDB2/IO81RSB2
H9	GDC0/IO77VPB1
H10	VCCIB1
H11	IO73PSB1
H12	VCC
J1	GEB1/IO136PDB3
J2	IO143NDB3
J3	VCCIB3
J4	GEC0/IO137NDB3
J5	IO125RSB2
J6	IO116RSB2
J7	VCC
J8	TCK
J9	GDA2/IO80RSB2
J10	TDO
J11	GDA1/IO79UDB1
J12	GDB1/IO78UDB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

<b>FG484</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	IO181RSB2
AA5	IO178RSB2
AA6	IO175RSB2
AA7	IO169RSB2
AA8	IO166RSB2
AA9	IO160RSB2
AA10	IO152RSB2
AA11	IO146RSB2
AA12	IO139RSB2
AA13	IO133RSB2
AA14	NC
AA15	NC
AA16	IO122RSB2
AA17	IO119RSB2
AA18	IO117RSB2
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	IO180RSB2
AB5	IO176RSB2
AB6	IO173RSB2

<b>FG484</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
AB7	IO167RSB2
AB8	IO162RSB2
AB9	IO156RSB2
AB10	IO150RSB2
AB11	IO145RSB2
AB12	IO144RSB2
AB13	IO132RSB2
AB14	IO127RSB2
AB15	IO126RSB2
AB16	IO123RSB2
AB17	IO121RSB2
AB18	IO118RSB2
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND