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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

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Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fgg144i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 •	Absolute	Maximum	Ratings
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Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	-0.3 to 1.65	V
VJTAG	JTAG DC voltage	-0.3 to 3.75	V
VPUMP	Programming voltage	-0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	-0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V	V
		(when I/O hot insertion mode is enabled)	
		-0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.

2. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.

3. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.



Table 2-2 • Recommended Operating Conditions¹

Symbol	Parame	eters ¹	Commercial	Industrial	Units
TJ	Junction temperature		0 to 85 ²	-40 to 100 ²	°C
VCC ³	1.5 V DC core supply volta	ge	1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation ⁴	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL))	1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV ⁵	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3. <u>6</u>	3.0 to 3. <u>6</u>	V
	3.3 V wide range DC suppl	ly voltage ⁶	2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS diff	ferential I/O	2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. All parameters representing voltages are measured with respect to GND unless otherwise specified.

- 2. Software Default Junction Temperature Range in the Libero[®] System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.
- 3. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.
- 4. VPUMP can be left floating during operation (not programming mode).
- 5. VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.
- 6. 3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.



Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹ Applicable to Advanced I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Single-Ended		•		-
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	468.67
3.3 V LVCMOS Wide Range ⁴	35	3.3	-	468.67
2.5 V LVCMOS	35	2.5	-	267.48
1.8 V LVCMOS	35	1.8	-	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	-	103.12
3.3 V PCI	10	3.3	-	201.02
3.3 V PCI-X	10	3.3	-	201.02
Differential		•		•
LVDS	-	2.5	7.74	88.92
LVPECL	_	3.3	19.54	166.52

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

2. PDC3 is the static power (where applicable) measured on VCCI.

3. PAC10 is the total dynamic power measured on VCC and VCCI.

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-12 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings¹ Applicable to Standard Plus I/O Banks

	C _{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW) ²	Dynamic Power PAC10 (µW/MHz) ³
Single-Ended				•
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	-	452.67
3.3 V LVCMOS Wide Range ⁴	35	3.3	-	452.67
2.5 V LVCMOS	35	2.5	-	258.32
1.8 V LVCMOS	35	1.8	-	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	-	92.84
3.3 V PCI	10	3.3	-	184.92
3.3 V PCI-X	10	3.3	_	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.

2. P_{DC3} is the static power (where applicable) measured on VMV.

3. P_{AC10} is the total dynamic power measured on VCC and VMV.

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.



	Definition	Device Specific Static Power (mW										
Parameter		A3P1000 A3P600 A3P400 A3P125 A3P125 A3P060 A3P030							A3P015			
PDC1	Array static power in Active mode		5	See Ta	ble 2-7	' on pa	age 2-7					
PDC2	I/O input pin static power (standard-dependent)		See	Table Table	2-8 on 2-10 c	page 3 on pag	2-7 thr e 2-8.	ough				
PDC3	I/O output pin static power (standard-dependent)		See	Table 2 Table	2-11 on 2-13 o	i page n page	2-9 thi e 2-10.	rough				
PDC4	Static PLL contribution	2.55 mW										
PDC5	Bank quiescent power (VCCI-dependent)		S	See Ta	ble 2-7	' on pa	age 2-7					

Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi Power spreadsheet calculator or SmartPower tool in Libero SoC software.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- · The number of combinatorial and sequential cells used in the design
- · The internal clock frequencies
- The number and the standard of I/O pins used in the design
- · The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-17 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—PTOTAL

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

 $P_{STAT} = P_{DC1} + N_{INPUTS} + P_{DC2} + N_{OUTPUTS} + P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

N_{OUTPUTS} is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}

Global Clock Contribution—P_{CLOCK}

 $P_{CLOCK} = (P_{AC1} + N_{SPINE}*P_{AC2} + N_{ROW}*P_{AC3} + N_{S-CELL}*P_{AC4})*F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.



User I/O Characteristics

Timing Model







Timing Characteristics

Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
4 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	-1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	-2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	-1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	-2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	-1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	-2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	-1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	-2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	-1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	-2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

and Switchi Table 2-62 •	2.5 V LV	cteristics CMOS H	igh Sle	W	T - 70	N°C Wor	et Cae		- 1 425	V Wor		Power	Matters.
	Applicat	ole to Sta	indard	Plus I/C	D Bank	s , wor	51-0456	, vcc -	- 1.423	v, wor	51-0450	VCCI - /	2.3 V
Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	-1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	-2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	-1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	-2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

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Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-63 • 2.5 V LVCMOS Low Slew Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	-2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	-1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	-2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Drive Strength 2 mA

4 mA

6 mA

8 mA

ng Chara	octeristics	5								> Mi	Power	Semi Matters.
1.8 V L\ Comme Applica	/CMOS ercial-Ca ble to S	High Sle se Cono tandard	ew litions Plus I/	: T _J = 7 O Ban	′0°C, Wo ks	orst-Cas	e VCC =	1.425	V, Woi	st-Case	VCCI =	1.7 V
Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
Std.	0.66	11.33	0.04	1.20	0.43	8.72	11.33	2.24	1.52	10.96	13.57	ns
-1	0.56	9.64	0.04	1.02	0.36	7.42	9.64	1.91	1.29	9.32	11.54	ns
-2	0.49	8.46	0.03	0.90	0.32	6.51	8.46	1.68	1.14	8.18	10.13	ns
Std.	0.66	6.48	0.04	1.20	0.43	5.48	6.48	2.65	2.60	7.72	8.72	ns
-1	0.56	5.51	0.04	1.02	0.36	4.66	5.51	2.25	2.21	6.56	7.42	ns
-2	0.49	4.84	0.03	0.90	0.32	4.09	4.84	1.98	1.94	5.76	6.51	ns
Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
-1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns

Table 2-72 •

Notes:

1. Software default selection highlighted in gray.

0.49

0.66

0.56

0.49

3.03

4.06

3.45

3.03

0.03 0.90

1.20

1.02

0.90

0.04

0.04

0.03

-2

Std.

-1

-2

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

0.32

0.43

0.36

0.32

2.87

3.84

3.27

2.87

3.03

4.06

3.45

3.03

2.19 2.32

3.10

2.64

2.32

2.93

2.49

2.19

4.54

6.07

5.17

4.54

4.70

6.30

5.36

4.70

ns

ns

ns

ns



Table 2-93 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.	.0	3	.3	3	V	
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: **Measuring point* = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-95 • LVPECL

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	1.80	0.04	1.40	ns
-1	0.56	1.53	0.04	1.19	ns
-2	0.49	1.34	0.03	1.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Output Register





Timing Characteristics

Table 2-99 • Output Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t _{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t _{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t _{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t _{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t _{OCKMPWH}	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
t _{OCKMPWL}	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.





Figure 2-25 • Timing Model and Waveforms



Timing Waveforms









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Package Pin Assignments

QN132 – Bottom View



Notes:

- 1. The die attach paddle center of the package is tied to ground (GND).
- 2. Option corner pads come with this device and package combination. It is optional to tie them to ground or leave them floating.
- 3. The QN132 package is discontinued and is not available for ProASIC3 devices.
- 4. For more information on package drawings, see PD3068: Package Mechanical Drawings.



QN132			
Pin Number	A3P030 Function		
C17	IO51RSB1		
C18	NC		
C19	ТСК		
C20	NC		
C21	VPUMP		
C22	VJTAG		
C23	NC		
C24	NC		
C25	NC		
C26	GDB0/IO38RSB0		
C27	NC		
C28	VCCIB0		
C29	IO32RSB0		
C30	IO29RSB0		
C31	IO28RSB0		
C32	IO25RSB0		
C33	NC		
C34	NC		
C35	VCCIB0		
C36	IO17RSB0		
C37	IO14RSB0		
C38	IO11RSB0		
C39	IO07RSB0		
C40	IO04RSB0		
D1	GND		
D2	GND		
D3	GND		
D4	GND		

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F	G144	F	FG144		G144
Pin Number	A3P125 Function	Pin Number	A3P125 Function	Pin Number	A3P125 Function
A1	GNDQ	D1	IO128RSB1	G1	GFA1/IO121RSB1
A2	VMV0	D2	IO129RSB1	G2	GND
A3	GAB0/IO02RSB0	D3	IO130RSB1	G3	VCCPLF
A4	GAB1/IO03RSB0	D4	GAA2/IO67RSB1	G4	GFA0/IO122RSB1
A5	IO11RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO18RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	VCC	D8	GBC1/IO36RSB0	G8	GDC1/IO61RSB0
A9	IO25RSB0	D9	GBB2/IO43RSB0	G9	IO48RSB0
A10	GBA0/IO39RSB0	D10	IO28RSB0	G10	GCC2/IO59RSB0
A11	GBA1/IO40RSB0	D11	IO44RSB0	G11	IO47RSB0
A12	GNDQ	D12	GCB1/IO53RSB0	G12	GCB2/IO58RSB0
B1	GAB2/IO69RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO125RSB1	H2	GFB2/IO119RSB1
B3	GAA0/IO00RSB0	E3	GFC1/IO126RSB1	H3	GFC2/IO118RSB1
B4	GAA1/IO01RSB0	E4	VCCIB1	H4	GEC1/IO112RSB1
B5	IO08RSB0	E5	IO68RSB1	H5	VCC
B6	IO14RSB0	E6	VCCIB0	H6	IO50RSB0
B7	IO19RSB0	E7	VCCIB0	H7	IO60RSB0
B8	IO22RSB0	E8	GCC1/IO51RSB0	H8	GDB2/IO71RSB1
B9	GBB0/IO37RSB0	E9	VCCIB0	H9	GDC0/IO62RSB0
B10	GBB1/IO38RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO56RSB0	H11	IO49RSB0
B12	VMV0	E12	IO46RSB0	H12	VCC
C1	IO132RSB1	F1	GFB0/IO123RSB1	J1	GEB1/IO110RSB1
C2	GFA2/IO120RSB1	F2	VCOMPLF	J2	IO115RSB1
C3	GAC2/IO131RSB1	F3	GFB1/IO124RSB1	J3	VCCIB1
C4	VCC	F4	IO127RSB1	J4	GEC0/IO111RSB1
C5	IO10RSB0	F5	GND	J5	IO116RSB1
C6	IO12RSB0	F6	GND	J6	IO117RSB1
C7	IO21RSB0	F7	GND	J7	VCC
C8	IO24RSB0	F8	GCC0/IO52RSB0	J8	ТСК
C9	IO27RSB0	F9	GCB0/IO54RSB0	J9	GDA2/IO70RSB1
C10	GBA2/IO41RSB0	F10	GND	J10	TDO
C11	IO42RSB0	F11	GCA1/IO55RSB0	J11	GDA1/IO65RSB0
C12	GBC2/IO45RSB0	F12	GCA2/IO57RSB0	J12	GDB1/IO63RSB0

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FG256			
Pin Number A3P400 Function			
P9	IO98RSB2		
P10	IO95RSB2		
P11	IO88RSB2		
P12	IO84RSB2		
P13	ТСК		
P14	VPUMP		
P15	TRST		
P16	GDA0/IO79VDB1		
R1	GEA1/IO135PDB3		
R2	GEA0/IO135NDB3		
R3	IO127RSB2		
R4	GEC2/IO132RSB2		
R5	IO123RSB2		
R6	IO118RSB2		
R7	IO112RSB2		
R8	IO106RSB2		
R9	IO100RSB2		
R10	IO96RSB2		
R11	IO89RSB2		
R12	IO85RSB2		
R13	GDB2/IO81RSB2		
R14	TDI		
R15	NC		
R16	TDO		
T1	GND		
T2	IO126RSB2		
Т3	GEB2/IO133RSB2		
T4	IO124RSB2		
T5	IO116RSB2		
Т6	IO113RSB2		
T7	IO107RSB2		
Т8	IO105RSB2		
Т9	IO102RSB2		
T10	IO97RSB2		
T11	IO92RSB2		
T12	GDC2/IO82RSB2		

FG256			
Pin Number	A3P400 Function		
T13	IO86RSB2		
T14	GDA2/IO80RSB2		
T15	TMS		
T16	GND		



FG256			
Pin Number	A3P600 Function		
P9	IO107RSB2		
P10	IO104RSB2		
P11	IO97RSB2		
P12	VMV1		
P13	ТСК		
P14	VPUMP		
P15	TRST		
P16	GDA0/IO88NDB1		
R1	GEA1/IO144PDB3		
R2	GEA0/IO144NDB3		
R3	IO139RSB2		
R4	GEC2/IO141RSB2		
R5	IO132RSB2		
R6	IO127RSB2		
R7	IO121RSB2		
R8	IO114RSB2		
R9	IO109RSB2		
R10	IO105RSB2		
R11	IO98RSB2		
R12	IO96RSB2		
R13	GDB2/IO90RSB2		
R14	TDI		
R15	GNDQ		
R16	TDO		
T1	GND		
T2	IO137RSB2		
Т3	GEB2/IO142RSB2		
T4	IO134RSB2		
T5	IO125RSB2		
Т6	IO123RSB2		
T7	IO118RSB2		
Т8	IO115RSB2		
Т9	IO111RSB2		
T10	IO106RSB2		
T11	IO102RSB2		
T12	GDC2/IO91RSB2		

FG256		
Pin Number	A3P600 Function	
T13	IO93RSB2	
T14	GDA2/IO89RSB2	
T15	TMS	
T16	GND	



	FG256	FG256		FG256	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GND	C7	IO25RSB0	E13	GBC2/IO80PDB1
A2	GAA0/IO00RSB0	C8	IO36RSB0	E14	IO83PPB1
A3	GAA1/IO01RSB0	C9	IO42RSB0	E15	IO86PPB1
A4	GAB0/IO02RSB0	C10	IO49RSB0	E16	IO87PDB1
A5	IO16RSB0	C11	IO56RSB0	F1	IO217NDB3
A6	IO22RSB0	C12	GBC0/IO72RSB0	F2	IO218NDB3
A7	IO28RSB0	C13	IO62RSB0	F3	IO216PDB3
A8	IO35RSB0	C14	VMV0	F4	IO216NDB3
A9	IO45RSB0	C15	IO78NDB1	F5	VCCIB3
A10	IO50RSB0	C16	IO81NDB1	F6	GND
A11	IO55RSB0	D1	IO222NDB3	F7	VCC
A12	IO61RSB0	D2	IO222PDB3	F8	VCC
A13	GBB1/IO75RSB0	D3	GAC2/IO223PDB3	F9	VCC
A14	GBA0/IO76RSB0	D4	IO223NDB3	F10	VCC
A15	GBA1/IO77RSB0	D5	GNDQ	F11	GND
A16	GND	D6	IO23RSB0	F12	VCCIB1
B1	GAB2/IO224PDB3	D7	IO29RSB0	F13	IO83NPB1
B2	GAA2/IO225PDB3	D8	IO33RSB0	F14	IO86NPB1
B3	GNDQ	D9	IO46RSB0	F15	IO90PPB1
B4	GAB1/IO03RSB0	D10	IO52RSB0	F16	IO87NDB1
B5	IO17RSB0	D11	IO60RSB0	G1	IO210PSB3
B6	IO21RSB0	D12	GNDQ	G2	IO213NDB3
B7	IO27RSB0	D13	IO80NDB1	G3	IO213PDB3
B8	IO34RSB0	D14	GBB2/IO79PDB1	G4	GFC1/IO209PPB3
B9	IO44RSB0	D15	IO79NDB1	G5	VCCIB3
B10	IO51RSB0	D16	IO82NSB1	G6	VCC
B11	IO57RSB0	E1	IO217PDB3	G7	GND
B12	GBC1/IO73RSB0	E2	IO218PDB3	G8	GND
B13	GBB0/IO74RSB0	E3	IO221NDB3	G9	GND
B14	IO71RSB0	E4	IO221PDB3	G10	GND
B15	GBA2/IO78PDB1	E5	VMV0	G11	VCC
B16	IO81PDB1	E6	VCCIB0	G12	VCCIB1
C1	IO224NDB3	E7	VCCIB0	G13	GCC1/IO91PPB1
C2	IO225NDB3	E8	IO38RSB0	G14	IO90NPB1
C3	VMV3	E9	IO47RSB0	G15	IO88PDB1
C4	IO11RSB0	E10	VCCIB0	G16	IO88NDB1
C5	GAC0/IO04RSB0	E11	VCCIB0	H1	GFB0/IO208NPB3
C6	GAC1/IO05RSB0	E12	VMV1	H2	GFA0/IO207NDB3

Revision	Changes	Page
Revision 9 (Oct 2009) Product Brief v1.3	The CS121 package was added to table under "Features and Benefits" section, the "I/Os Per Package 1" table, Table 1 • ProASIC3 FPGAs Package Sizes Dimensions, "ProASIC3 Ordering Information", and the "Temperature Grade Offerings" table.	I – IV
	"ProASIC3 Ordering Information" was revised to include the fact that some RoHS compliant packages are halogen-free.	IV
Packaging v1.5	The "CS121 – Bottom View" figure and pin table for A3P060 are new.	4-15
Revision 8 (Aug 2009) Product Brief v1.2	All references to M7 devices (CoreMP7) and speed grade –F were removed from this document.	N/A
	Table 1-1 I/O Standards supported is new.	1-7
	The I/Os with Advanced I/O Standards section was revised to add definitions of hot-swap and cold-sparing.	1-7
DC and Switching Characteristics v1.4	$3.3~\rm V$ LVCMOS and $1.2~\rm V$ LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained $3.3~\rm V$ LVCMOS and $1.2~\rm V$ LVCMOS data.	N/A
	${\rm I}_{\rm IL}$ and ${\rm I}_{\rm IH}$ input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	-F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	2-6
	In Table 2-116 • RAM4K9, the following specifications were removed: t _{WRO} t _{CCKH}	2-96
	In Table 2-117 • RAM512X18, the following specifications were removed: t _{WRO} t _{CCKH}	2-97
	In the title of Table 2-74 • 1.8 V LVCMOS High Slew, VCCI had a typo. It was changed from 3.0 V to 1.7 V.	2-58
Revision 7 (Feb 2009) Product Brief v1.1	The "Advanced I/O" section was revised to add a bullet regarding wide range power supply voltage support.	I
	The table under "Features and Benefits" section, was updated to include a value for typical equivalent macrocells for A3P250.	I
	The QN48 package was added to the following tables: the table under "Features and Benefits" section, "I/Os Per Package 1" "ProASIC3 FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings". The number of singled-ended I/Os for QN68 was added to the "I/Os Per Package 1" table.	N/A
	The Wide Range I/O Support section is new.	1-7
Revision 6 (Dec 2008)	The "QN48 – Bottom View" section is new.	4-1
Packaging v1.4	The "QN68" pin table for A3P030 is new.	4-5



Datasheet Information

Revision	Changes	Page
Advance v0.3	The "PLL Macro" section was updated. EXTFB information was removed from this section.	2-15
	The CCC Output Peak-to-Peak Period Jitter F _{CCC_OUT} was updated in Table 2- 11 • ProASIC3 CCC/PLL Specification	2-29
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Hot-Swap Support" section was updated.	2-33
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to VCC ₁ B1.	2-97
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "JTAG Pins" section was updated.	2-51
	"128-Bit AES Decryption" section was updated to include M7 device information.	2-53
	Table 3-6 was updated.	3-6
	Table 3-7 was updated.	3-6
	In Table 3-11, PAC4 was updated.	3-93-8
	Table 3-20 was updated.	3-20
	The note in Table 3-32 was updated.	3-27
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-31 to 3- 73
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-85 to 3-90
	F _{TCKMAX} was updated in Table 3-110.	3-97
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-13 was updated.	2-30
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34