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#### Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

#### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

## Details

E·XFI

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1fgg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



ProASIC3 Devices	A3P015 <sup>1</sup>	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex-M1 Devices <sup>2</sup>					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
Package Pins QFN CS VQFP TQFP PQFP FBGA	QN68	QN48, QN68, QN132 <sup>7</sup> VQ100	QN132 <sup>7</sup> CS121 VQ100 TQ144 FG144	QN132 <sup>7</sup> VQ100 TQ144 PQ208 FG144	QN132 <sup>7</sup> VQ100 PQ208 FG144/256 <sup>5</sup>	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484

Notes:

- A3P015 is not recommended for new designs.
   Refer to the Cortex-M1 product brief for more information.
   AES is not available for Cortex-M1 ProASIC3 devices.
   Six chip (main) and three quadrant global networks are available for A3P060 and above.
   The M1A3P250 device does not support this package.
   For higher densities and support of additional features, refer to the ProASIC3E Flash Family FPGAs datasheet.
   Package not available.



# **Advanced Flash Technology**

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flashbased, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

# **Advanced Architecture**

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory<sup>†</sup>
- Extensive CCCs and PLLs<sup>†</sup>
- Advanced I/O structure



*Note:* \*Not supported by A3P015 and A3P030 devices



*†* The A3P015 and A3P030 do not support PLL or SRAM.



#### Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings

-2 Speed Grade, Commercial-Case Conditions:  $T_J = 70^{\circ}$ C, Worst Case VCC = 1.425 V, Worst-Case VCCI (per standard)

Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor	t <sub>bour</sub> (ns)	t <sub>DP</sub> (ns)	t <sub>DIN</sub> (ns)	t <sub>pΥ</sub> (ns)	t <sub>EOUT</sub> (ns)	t <sub>ZL</sub> (ns)	t <sub>zH</sub> (ns)	t <sub>LZ</sub> (ns)	t <sub>HZ</sub> (ns)	t <sub>ZLS</sub> (ns)	t <sub>zHS</sub> (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	-	0.45	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 µA	12 mA	High	35	-	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	-	0.45	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns
1.8 V LVCMOS	8 mA	8 mA	High	35	-	0.45	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
1.5 V LVCMOS	4 mA	4 mA	High	35	-	0.45	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns
3.3 V PCI	Per PCI spec	-	High	10	25 <sup>4</sup>	0.45	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns
3.3 V PCI-X	Per PCI-X spec	-	High	10	25 <sup>4</sup>	0.45	1.72	0.03	0.62	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-64 for connectivity. This resistor is not required during normal operation.



### Table 2-43 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Commercial-Case Conditions:  $T_J = 70^{\circ}$ C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard Plus I/O Banks

Drive	Speed												
Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>ZH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
2 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	-1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	-2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
4 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	-1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	-2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
6 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	-1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	-2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
8 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	–1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	-2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
12 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	-1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	-2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
16 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	-1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	-2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Table 2-49 •	Minimum and Maximum DC Input and Output Levels
	Applicable to Standard I/O Banks

3.3 V LVCMOS Wide Range	Equiv. Software Default	v	ΊL	v	ΊH	VOL	VOH	IOL	юн	IOSL	IOSH	IIL <sup>2</sup>	IIH <sup>3</sup>
Drive Strength	Drive Strength Option <sup>1</sup>	Min V	Max V	Min V	Max V	Max V	Min V	μA	μA	Max mA <sup>4</sup>	Max mA <sup>4</sup>	µA⁵	µA⁵
100 µA	2 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	-0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \ \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

4. Currents are measured at 85°C junction temperature.

5. All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

6. Software default selection highlighted in gray.



# 2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

2.5 V LVCMOS	V	ΊL	v	ΊH	VOL	VOH	IOL	IOH	IOSL	IOSH	IIL1	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

#### Table 2-56 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

# Table 2-57 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	v	IL.	V	IH	VOL	VOH	IOL	IOH	IOSL	IOSH	IIL <sup>1</sup>	IIH <sup>2</sup>
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA <sup>3</sup>	Max. mA <sup>3</sup>	μA <sup>4</sup>	μA <sup>4</sup>
2 mA	-0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	-0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	-0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	-0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	-0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



#### Table 2-61 • 2.5 V LVCMOS Low Slew

Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Advanced I/O Banks

Drive	Speed												
Strength	Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>ZLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	0.60	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.51	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	-2	0.45	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
6 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	-1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	-2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
8 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	-1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	-2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.60	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	-1	0.51	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	-2	0.45	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.60	5.76	0.04	1.31	0.43	5.87	5.53	3.36	3.44	8.11	7.76	ns
	-1	0.51	4.90	0.04	1.11	0.36	4.99	4.70	2.86	2.92	6.90	6.60	ns
	-2	0.45	4.30	0.03	0.98	0.32	4.38	4.13	2.51	2.57	6.05	5.80	ns
24 mA	Std.	0.60	5.51	0.04	1.31	0.43	5.50	5.51	3.43	3.87	7.74	7.74	ns
	-1	0.51	4.68	0.04	1.11	0.36	4.68	4.68	2.92	3.29	6.58	6.59	ns
	-2	0.45	4.11	0.03	0.98	0.32	4.11	4.11	2.56	2.89	5.78	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

and Switchi <b>Table 2-62 •</b>	2.5 V LV	cteristics CMOS H	igh Sle	W	T - 70	N°C Wor	et Cae		- 1 425	V Wor		Power	Matters.
	Applicat	ole to Sta	indard	Plus I/C	D Bank	s , wor	51-0456	, vcc -	- 1.423	v, wor	51-0450	VCCI - /	2.3 V
Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	-1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	-2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	-1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	-2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Microsomi

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## Table 2-63 • 2.5 V LVCMOS Low Slew Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	t <sub>EOUT</sub>	t <sub>ZL</sub>	t <sub>zH</sub>	t <sub>LZ</sub>	t <sub>HZ</sub>	t <sub>zLS</sub>	t <sub>zHS</sub>	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	-2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	-1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	-2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



# **Output DDR Module**



# Figure 2-22 • Output DDR Timing Model

# Table 2-103 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t <sub>DDROCLKQ</sub>	Clock-to-Out	B, E
t <sub>DDROCLR2Q</sub>	Asynchronous Clear-to-Out	C, E
t <sub>DDROREMCLR</sub>	Clear Removal	С, В
t <sub>DDRORECCLR</sub>	Clear Recovery	С, В
t <sub>DDROSUD1</sub>	Data Setup Data_F	А, В
t <sub>DDROSUD2</sub>	Data Setup Data_R	D, B
t <sub>DDROHD1</sub>	Data Hold Data_F	А, В
t <sub>DDROHD2</sub>	Data Hold Data_R	D, B

# **Timing Characteristics**

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	Y = !A	t <sub>PD</sub>	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t <sub>PD</sub>	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t <sub>PD</sub>	0.47	0.54	0.63	ns
OR2	Y = A + B	t <sub>PD</sub>	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t <sub>PD</sub>	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t <sub>PD</sub>	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t <sub>PD</sub>	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t <sub>PD</sub>	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t <sub>PD</sub>	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t <sub>PD</sub>	0.56	0.64	0.75	ns

## Table 2-105 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: T<sub>1</sub> = 70°C, Worst-Case VCC = 1.425 V

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

# VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.



Figure 2-26 • Sample of Sequential Cells

# Table 2-113 • A3P600 Global ResourceCommercial-Case Conditions: TJ = 70°C, VCC = 1.425 V

		-2		-1		Std.		
Parameter	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Microse

Power Matters.

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

# Table 2-114 • A3P1000 Global Resource

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V
```

		-2		-1		Std.		
Parameter	Description	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Units
t <sub>RCKL</sub>	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
t <sub>RCKH</sub>	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
t <sub>RCKMPWH</sub>	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t <sub>RCKMPWL</sub>	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t <sub>RCKSW</sub>	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



# **JTAG 1532 Characteristics**

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

# **Timing Characteristics**

## Table 2-125 • JTAG 1532

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V
```

Parameter	Description	-2	-1	Std.	Units
t <sub>DISU</sub>	Test Data Input Setup Time	0.50	0.57	0.67	ns
t <sub>DIHD</sub>	Test Data Input Hold Time	1.00	1.13	1.33	ns
t <sub>TMSSU</sub>	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t <sub>TMDHD</sub>	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t <sub>TCK2Q</sub>	Clock to Q (data out)	6.00	6.80	8.00	ns
t <sub>RSTB2Q</sub>	Reset to Q (data out)	20.00	22.67	26.67	ns
F <sub>TCKMAX</sub>	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t <sub>TRSTREM</sub>	ResetB Removal Time	0.00	0.00	0.00	ns
t <sub>TRSTREC</sub>	ResetB Recovery Time	0.20	0.23	0.27	ns
t <sub>TRSTMPW</sub>	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



# 3 – Pin Descriptions

# **Supply Pins**

## Ground

Ground supply voltage to the core, I/O outputs, and I/O logic.

## GNDQ Ground (quiet)

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

#### VCC

GND

## Core Supply Voltage

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

## VCCIBx I/O Supply Voltage

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

## VMVx I/O Supply Voltage (quiet)

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

## VCCPLA/B/C/D/E/F PLL Supply Voltage

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on ProASIC3 devices.

## VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC3 devices.



## VJTAG

## JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design.

If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

## VPUMP Programming Supply Voltage

ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in Table 2-2 on page 2-2.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01  $\mu$ F and 0.33  $\mu$ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

# **User Pins**

I/O

### User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to  $V_{CCI}$ . With  $V_{CCI}$ , VMV, and  $V_{CC}$  supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

#### GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

## FF Flash\*Freeze Mode Activation Pin

Flash\*Freeze is available on IGLOO, ProASIC3L, and RT ProASIC3 devices. It is not supported on ProASIC3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash\*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash\*Freeze



Package Pin Assignments

QN132					
Pin Number	A3P250 Function				
C17	IO74RSB2				
C18	VCCIB2				
C19	ТСК				
C20	VMV2				
C21	VPUMP				
C22	VJTAG				
C23	VCCIB1				
C24	IO53NSB1				
C25	IO51NPB1				
C26	GCA1/IO50PPB1				
C27	GCC0/IO48NDB1				
C28	VCCIB1				
C29	IO42NDB1				
C30	GNDQ				
C31	GBA1/IO40RSB0				
C32	GBB0/IO37RSB0				
C33	VCC				
C34	IO24RSB0				
C35	IO19RSB0				
C36	IO16RSB0				
C37	IO10RSB0				
C38	VCCIB0				
C39	GAB1/IO03RSB0				
C40	VMV0				
D1	GND				
D2	GND				
D3	GND				
D4	GND				



# TQ144 – Top View



# Note

For more information on package drawings, see PD3068: Package Mechanical Drawings.



Package Pin Assignments

# PQ208 – Top View



# Note

For more information on package drawings, see PD3068: Package Mechanical Drawings.

PQ208		F	PQ208	PQ208		
Pin Number	A3P400 Function	Pin Number	A3P400 Function	Pin Number	A3P400 Function	
1	GND	37	IO141PSB3	73	IO112RSB2	
2	GAA2/IO155UDB3	38	IO140PDB3	74	IO111RSB2	
3	IO155VDB3	39	IO140NDB3	75	IO110RSB2	
4	GAB2/IO154UDB3	40	VCCIB3	76	IO109RSB2	
5	IO154VDB3	41	GND	77	IO108RSB2	
6	GAC2/IO153UDB3	42	IO138PDB3	78	IO107RSB2	
7	IO153VDB3	43	IO138NDB3	79	IO106RSB2	
8	IO152UDB3	44	GEC1/IO137PDB3	80	IO104RSB2	
9	IO152VDB3	45	GEC0/IO137NDB3	81	GND	
10	IO151UDB3	46	GEB1/IO136PDB3	82	IO102RSB2	
11	IO151VDB3	47	GEB0/IO136NDB3	83	IO101RSB2	
12	IO150PDB3	48	GEA1/IO135PDB3	84	IO100RSB2	
13	IO150NDB3	49	GEA0/IO135NDB3	85	IO99RSB2	
14	IO149PDB3	50	VMV3	86	IO98RSB2	
15	IO149NDB3	51	GNDQ	87	IO97RSB2	
16	VCC	52	GND	88	VCC	
17	GND	53	VMV2	89	VCCIB2	
18	VCCIB3	54	NC	90	IO94RSB2	
19	IO148PDB3	55	GEA2/IO134RSB2	91	IO92RSB2	
20	IO148NDB3	56	GEB2/IO133RSB2	92	IO90RSB2	
21	GFC1/IO147PDB3	57	GEC2/IO132RSB2	93	IO88RSB2	
22	GFC0/IO147NDB3	58	IO131RSB2	94	IO86RSB2	
23	GFB1/IO146PDB3	59	IO130RSB2	95	IO84RSB2	
24	GFB0/IO146NDB3	60	IO129RSB2	96	GDC2/IO82RSB2	
25	VCOMPLF	61	IO128RSB2	97	GND	
26	GFA0/IO145NPB3	62	VCCIB2	98	GDB2/IO81RSB2	
27	VCCPLF	63	IO125RSB2	99	GDA2/IO80RSB2	
28	GFA1/IO145PPB3	64	IO123RSB2	100	GNDQ	
29	GND	65	GND	101	тск	
30	GFA2/IO144PDB3	66	IO121RSB2	102	TDI	
31	IO144NDB3	67	IO119RSB2	103	TMS	
32	GFB2/IO143PDB3	68	IO117RSB2	104	VMV2	
33	IO143NDB3	69	IO115RSB2	105	GND	
34	GFC2/IO142PDB3	70	IO113RSB2	106	VPUMP	
35	IO142NDB3	71	VCC	107	NC	
36	NC	72	VCCIB2	108	TDO	



FG144				
Pin Number	A3P250 Function			
K1	GEB0/IO99NDB3			
K2	GEA1/IO98PDB3			
K3	GEA0/IO98NDB3			
K4	GEA2/IO97RSB2			
K5	IO90RSB2			
K6	IO84RSB2			
K7	GND			
K8	IO66RSB2			
K9	GDC2/IO63RSB2			
K10	GND			
K11	GDA0/IO60VDB1			
K12	GDB0/IO59VDB1			
L1	GND			
L2	VMV3			
L3	GEB2/IO96RSB2			
L4	IO91RSB2			
L5	VCCIB2			
L6	IO82RSB2			
L7	IO80RSB2			
L8	IO72RSB2			
L9	TMS			
L10	VJTAG			
L11	VMV2			
L12	TRST			
M1	GNDQ			
M2	GEC2/IO95RSB2			
M3	IO92RSB2			
M4	IO89RSB2			
M5	IO87RSB2			
M6	IO85RSB2			
M7	IO78RSB2			
M8	IO76RSB2			
M9	TDI			
M10	VCCIB2			
M11	VPUMP			
M12	GNDQ			



Datasheet Information

Revision	Changes	Page
Advance v0.3	The "PLL Macro" section was updated. EXTFB information was removed from this section.	2-15
	The CCC Output Peak-to-Peak Period Jitter F <sub>CCC_OUT</sub> was updated in Table 2- 11 • ProASIC3 CCC/PLL Specification	2-29
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Hot-Swap Support" section was updated.	2-33
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to VCC <sub>1</sub> B1.	2-97
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "JTAG Pins" section was updated.	2-51
	"128-Bit AES Decryption" section was updated to include M7 device information.	2-53
	Table 3-6 was updated.	3-6
	Table 3-7 was updated.	3-6
	In Table 3-11, PAC4 was updated.	3-93-8
	Table 3-20 was updated.	3-20
	The note in Table 3-32 was updated.	3-27
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-31 to 3- 73
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-85 to 3-90
	F <sub>TCKMAX</sub> was updated in Table 3-110.	3-97
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-13 was updated.	2-30
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34