E·XFL



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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1pq208

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

		I/O Standards Supported							
I/O Bank Type	Device and Bank Location	LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS					
Advanced	East and west Banks of A3P250 and larger devices	\checkmark	\checkmark	\checkmark					
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	\checkmark	\checkmark	Not supported					
Standard	All banks of A3P015 and A3P030	\checkmark	Not supported	Not supported					

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a poweredup system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

- Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.
 - 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
 - 2. From the FlashPro GUI, click PDB Configuration. A FlashPoint Programming File Generator window appears.
 - 3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
 - 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
 - 5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 I/O is set to drive out logic High



	Definition	Device Specific Static Power (mW)											
Parameter		A3P1000	A3P600	A3P400	A3P250	A3P125	A3P060	A3P030	A3P015				
PDC1	Array static power in Active mode	See Table 2-7 on page 2-7.											
PDC2	I/O input pin static power (standard-dependent)	See Table 2-8 on page 2-7 through Table 2-10 on page 2-8.											
PDC3	I/O output pin static power (standard-dependent)	See Table 2-11 on page 2-9 through Table 2-13 on page 2-10.											
PDC4	Static PLL contribution	2.55 mW											
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-7 on page 2-7.											

Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi Power spreadsheet calculator or SmartPower tool in Libero SoC software.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- · The number of combinatorial and sequential cells used in the design
- · The internal clock frequencies
- The number and the standard of I/O pins used in the design
- · The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-17 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—PTOTAL

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

 $P_{STAT} = P_{DC1} + N_{INPUTS} + P_{DC2} + N_{OUTPUTS} + P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

N_{OUTPUTS} is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}

Global Clock Contribution—P_{CLOCK}

 $P_{CLOCK} = (P_{AC1} + N_{SPINE}*P_{AC2} + N_{ROW}*P_{AC3} + N_{S-CELL}*P_{AC4})*F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.



Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings

-2 Speed Grade, Commercial-Case Conditions: $T_J = 70^{\circ}$ C, Worst Case VCC = 1.425 V, Worst-Case VCCI (per standard)

Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor	t _{bour} (ns)	t _{DP} (ns)	t _{DIN} (ns)	t _{pΥ} (ns)	t _{EOUT} (ns)	t _{ZL} (ns)	t _{zH} (ns)	t _{LZ} (ns)	t _{HZ} (ns)	t _{ZLS} (ns)	t _{zHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	-	0.45	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
3.3 V LVCMOS Wide Range ²	100 µA	12 mA	High	35	-	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	-	0.45	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns
1.8 V LVCMOS	8 mA	8 mA	High	35	-	0.45	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
1.5 V LVCMOS	4 mA	4 mA	High	35	-	0.45	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns
3.3 V PCI	Per PCI spec	-	High	10	25 ⁴	0.45	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns
3.3 V PCI-X	Per PCI-X spec	-	High	10	25 ⁴	0.45	1.72	0.03	0.62	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 μA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-64 for connectivity. This resistor is not required during normal operation.



I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min	Мах	Units
C _{IN}	Input capacitance	VIN = 0, f = 1.0 MHz	-	8	pF
CINCLK	Input capacitance on the clock pin	VIN = 0, f = 1.0 MHz	_	8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances¹ Applicable to Advanced I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range ⁴	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

- 2. R_(PULL-DOWN-MAX) = (VOLspec) / IOLspec
- 3. R_(PULL-UP-MAX) = (VCCImax VOHspec) / IOHspec

4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

^{1.} These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.

and Switch Fable 2-62 •	2.5 V LV	cteristics CMOS H	igh Sle	W	T - 70	N°C Wor	et Cae		- 1 425	V Wor		Power	Matters.
	Applicat	ole to Sta	indard	Plus I/C	D Bank	s , wor	51-0456	, vcc -	- 1.423	v, wor	51-0450	VCCI - /	2.3 V
Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	-1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	-2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	-1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	-2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	-1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	-2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Microsomi

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-63 • 2.5 V LVCMOS Low Slew Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	-2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	-1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	-2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	–1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	-2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Timing Characteristics

Table 2-80 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	-1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	-2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	-1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	-2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
6 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	-1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	-2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
8 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{oclkq}	Clock-to-Q of the Output Data Register	H, DOUT
t _{OSUD}	Data Setup Time for the Output Data Register	F, H
t _{OHD}	Data Hold Time for the Output Data Register	F, H
t _{OSUE}	Enable Setup Time for the Output Data Register	G, H
t _{OHE}	Enable Hold Time for the Output Data Register	G, H
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	J, H
t _{OEHD}	Data Hold Time for the Output Enable Register	J, H
t _{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t _{OEHE}	Enable Hold Time for the Output Enable Register	K, H
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t _{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t _{ISUD}	Data Setup Time for the Input Data Register	C, A
t _{IHD}	Data Hold Time for the Input Data Register	C, A
t _{ISUE}	Enable Setup Time for the Input Data Register	B, A
t _{IHE}	Enable Hold Time for the Input Data Register	B, A
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
tIRECPRE	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Table 2-96 • Parameter Definition and Measuring Nodes

Note: *See Figure 2-15 on page 2-69 for more information.



Table 2-111 • A3P250 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		-	-2	-	-1	S		
Parameter	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.80	1.01	0.91	1.15	1.07	1.36	ns
t _{RCKH}	Input High Delay for Global Clock	0.78	1.04	0.89	1.18	1.04	1.39	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-112 • A3P400 Global Resource

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, VCC = 1.425 V
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		-	-2		-1		Std.	
Parameter	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t _{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



VJTAG

JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design.

If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in Table 2-2 on page 2-2.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O

User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI} . With V_{CCI} , VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze is available on IGLOO, ProASIC3L, and RT ProASIC3 devices. It is not supported on ProASIC3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze



Package Pin Assignments

QN132			
Pin Number	A3P060 Function		
C17	IO57RSB1		
C18	NC		
C19	ТСК		
C20	VMV1		
C21	VPUMP		
C22	VJTAG		
C23	VCCIB0		
C24	NC		
C25	NC		
C26	GCA1/IO42RSB0		
C27	GCC0/IO39RSB0		
C28	VCCIB0		
C29	IO29RSB0		
C30	GNDQ		
C31	GBA1/IO27RSB0		
C32	GBB0/IO24RSB0		
C33	VCC		
C34	IO19RSB0		
C35	IO16RSB0		
C36	IO13RSB0		
C37	GAC1/IO10RSB0		
C38	NC		
C39	GAA0/IO05RSB0		
C40	VMV0		
D1	GND		
D2	GND		
D3	GND		
D4	GND		



, N	VQ100	\ \	/Q100	VQ100	
Pin Number	A3P030 Function	Pin Number	A3P030 Function	Pin Number	A3P030 Function
1	GND	37	VCC	73	IO27RSB0
2	IO82RSB1	38	GND	74	IO26RSB0
3	IO81RSB1	39	VCCIB1	75	IO25RSB0
4	IO80RSB1	40	IO49RSB1	76	IO24RSB0
5	IO79RSB1	41	IO47RSB1	77	IO23RSB0
6	IO78RSB1	42	IO46RSB1	78	IO22RSB0
7	IO77RSB1	43	IO45RSB1	79	IO21RSB0
8	IO76RSB1	44	IO44RSB1	80	IO20RSB0
9	GND	45	IO43RSB1	81	IO19RSB0
10	IO75RSB1	46	IO42RSB1	82	IO18RSB0
11	IO74RSB1	47	ТСК	83	IO17RSB0
12	GEC0/IO73RSB1	48	TDI	84	IO16RSB0
13	GEA0/IO72RSB1	49	TMS	85	IO15RSB0
14	GEB0/IO71RSB1	50	NC	86	IO14RSB0
15	IO70RSB1	51	GND	87	VCCIB0
16	IO69RSB1	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB1	54	TDO	90	IO12RSB0
19	IO68RSB1	55	TRST	91	IO10RSB0
20	IO67RSB1	56	VJTAG	92	IO08RSB0
21	IO66RSB1	57	IO41RSB0	93	IO07RSB0
22	IO65RSB1	58	IO40RSB0	94	IO06RSB0
23	IO64RSB1	59	IO39RSB0	95	IO05RSB0
24	IO63RSB1	60	IO38RSB0	96	IO04RSB0
25	IO62RSB1	61	IO37RSB0	97	IO03RSB0
26	IO61RSB1	62	IO36RSB0	98	IO02RSB0
27	IO60RSB1	63	GDB0/IO34RSB0	99	IO01RSB0
28	IO59RSB1	64	GDA0/IO33RSB0	100	IO00RSB0
29	IO58RSB1	65	GDC0/IO32RSB0		
30	IO57RSB1	66	VCCIB0		
31	IO56RSB1	67	GND		
32	IO55RSB1	68	VCC		
33	IO54RSB1	69	IO31RSB0		
34	IO53RSB1	70	IO30RSB0		
35	IO52RSB1	71	IO29RSB0		
36	IO51RSB1	72	IO28RSB0		

Р	Q208	F	Q208	PQ208	
Pin Number	A3P400 Function	Pin Number	A3P400 Function	Pin Number	A3P400 Function
1	GND	37	IO141PSB3	73	IO112RSB2
2	GAA2/IO155UDB3	38	IO140PDB3	74	IO111RSB2
3	IO155VDB3	39	IO140NDB3	75	IO110RSB2
4	GAB2/IO154UDB3	40	VCCIB3	76	IO109RSB2
5	IO154VDB3	41	GND	77	IO108RSB2
6	GAC2/IO153UDB3	42	IO138PDB3	78	IO107RSB2
7	IO153VDB3	43	IO138NDB3	79	IO106RSB2
8	IO152UDB3	44	GEC1/IO137PDB3	80	IO104RSB2
9	IO152VDB3	45	GEC0/IO137NDB3	81	GND
10	IO151UDB3	46	GEB1/IO136PDB3	82	IO102RSB2
11	IO151VDB3	47	GEB0/IO136NDB3	83	IO101RSB2
12	IO150PDB3	48	GEA1/IO135PDB3	84	IO100RSB2
13	IO150NDB3	49	GEA0/IO135NDB3	85	IO99RSB2
14	IO149PDB3	50	VMV3	86	IO98RSB2
15	IO149NDB3	51	GNDQ	87	IO97RSB2
16	VCC	52	GND	88	VCC
17	GND	53	VMV2	89	VCCIB2
18	VCCIB3	54	NC	90	IO94RSB2
19	IO148PDB3	55	GEA2/IO134RSB2	91	IO92RSB2
20	IO148NDB3	56	GEB2/IO133RSB2	92	IO90RSB2
21	GFC1/IO147PDB3	57	GEC2/IO132RSB2	93	IO88RSB2
22	GFC0/IO147NDB3	58	IO131RSB2	94	IO86RSB2
23	GFB1/IO146PDB3	59	IO130RSB2	95	IO84RSB2
24	GFB0/IO146NDB3	60	IO129RSB2	96	GDC2/IO82RSB2
25	VCOMPLF	61	IO128RSB2	97	GND
26	GFA0/IO145NPB3	62	VCCIB2	98	GDB2/IO81RSB2
27	VCCPLF	63	IO125RSB2	99	GDA2/IO80RSB2
28	GFA1/IO145PPB3	64	IO123RSB2	100	GNDQ
29	GND	65	GND	101	тск
30	GFA2/IO144PDB3	66	IO121RSB2	102	TDI
31	IO144NDB3	67	IO119RSB2	103	TMS
32	GFB2/IO143PDB3	68	IO117RSB2	104	VMV2
33	IO143NDB3	69	IO115RSB2	105	GND
34	GFC2/IO142PDB3	70	IO113RSB2	106	VPUMP
35	IO142NDB3	71	VCC	107	NC
36	NC	72	VCCIB2	108	TDO

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Package Pin Assignments

F	G144	FG144		FG144	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
A1	GNDQ	D1	IO91RSB1	G1	GFA1/IO84RSB1
A2	VMV0	D2	IO92RSB1	G2	GND
A3	GAB0/IO04RSB0	D3	IO93RSB1	G3	VCCPLF
A4	GAB1/IO05RSB0	D4	GAA2/IO51RSB1	G4	GFA0/IO85RSB1
A5	IO08RSB0	D5	GAC0/IO06RSB0	G5	GND
A6	GND	D6	GAC1/IO07RSB0	G6	GND
A7	IO11RSB0	D7	GBC0/IO19RSB0	G7	GND
A8	VCC	D8	GBC1/IO20RSB0	G8	GDC1/IO45RSB0
A9	IO16RSB0	D9	GBB2/IO27RSB0	G9	IO32RSB0
A10	GBA0/IO23RSB0	D10	IO18RSB0	G10	GCC2/IO43RSB0
A11	GBA1/IO24RSB0	D11	IO28RSB0	G11	IO31RSB0
A12	GNDQ	D12	GCB1/IO37RSB0	G12	GCB2/IO42RSB0
B1	GAB2/IO53RSB1	E1	VCC	H1	VCC
B2	GND	E2	GFC0/IO88RSB1	H2	GFB2/IO82RSB1
B3	GAA0/IO02RSB0	E3	GFC1/IO89RSB1	H3	GFC2/IO81RSB1
B4	GAA1/IO03RSB0	E4	VCCIB1	H4	GEC1/IO77RSB1
B5	IO00RSB0	E5	IO52RSB1	H5	VCC
B6	IO10RSB0	E6	VCCIB0	H6	IO34RSB0
B7	IO12RSB0	E7	VCCIB0	H7	IO44RSB0
B8	IO14RSB0	E8	GCC1/IO35RSB0	H8	GDB2/IO55RSB1
В9	GBB0/IO21RSB0	E9	VCCIB0	H9	GDC0/IO46RSB0
B10	GBB1/IO22RSB0	E10	VCC	H10	VCCIB0
B11	GND	E11	GCA0/IO40RSB0	H11	IO33RSB0
B12	VMV0	E12	IO30RSB0	H12	VCC
C1	IO95RSB1	F1	GFB0/IO86RSB1	J1	GEB1/IO75RSB1
C2	GFA2/IO83RSB1	F2	VCOMPLF	J2	IO78RSB1
C3	GAC2/IO94RSB1	F3	GFB1/IO87RSB1	J3	VCCIB1
C4	VCC	F4	IO90RSB1	J4	GEC0/IO76RSB1
C5	IO01RSB0	F5	GND	J5	IO79RSB1
C6	IO09RSB0	F6	GND	J6	IO80RSB1
C7	IO13RSB0	F7	GND	J7	VCC
C8	IO15RSB0	F8	GCC0/IO36RSB0	J8	ТСК
C9	IO17RSB0	F9	GCB0/IO38RSB0	J9	GDA2/IO54RSB1
C10	GBA2/IO25RSB0	F10	GND	J10	TDO
C11	IO26RSB0	F11	GCA1/IO39RSB0	J11	GDA1/IO49RSB0
C12	GBC2/IO29RSB0	F12	GCA2/IO41RSB0	J12	GDB1/IO47RSB0

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Package Pin Assignments

	FG256		FG256	FG256	
Pin Number	A3P400 Function	Pin Number	A3P400 Function	Pin Number	A3P400 Function
A1	GND	C5	GAC0/IO04RSB0	E9	IO31RSB0
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	VCCIB0
A3	GAA1/IO01RSB0	C7	IO20RSB0	E11	VCCIB0
A4	GAB0/IO02RSB0	C8	IO24RSB0	E12	VMV1
A5	IO16RSB0	C9	IO33RSB0	E13	GBC2/IO62PDB1
A6	IO17RSB0	C10	IO39RSB0	E14	IO65RSB1
A7	IO22RSB0	C11	IO45RSB0	E15	IO52RSB0
A8	IO28RSB0	C12	GBC0/IO54RSB0	E16	IO66PDB1
A9	IO34RSB0	C13	IO48RSB0	F1	IO150NDB3
A10	IO37RSB0	C14	VMV0	F2	IO149NPB3
A11	IO41RSB0	C15	IO61NPB1	F3	IO09RSB0
A12	IO43RSB0	C16	IO63PDB1	F4	IO152UDB3
A13	GBB1/IO57RSB0	D1	IO151VDB3	F5	VCCIB3
A14	GBA0/IO58RSB0	D2	IO151UDB3	F6	GND
A15	GBA1/IO59RSB0	D3	GAC2/IO153UDB3	F7	VCC
A16	GND	D4	IO06RSB0	F8	VCC
B1	GAB2/IO154UDB3	D5	GNDQ	F9	VCC
B2	GAA2/IO155UDB3	D6	IO10RSB0	F10	VCC
B3	IO12RSB0	D7	IO19RSB0	F11	GND
B4	GAB1/IO03RSB0	D8	IO26RSB0	F12	VCCIB1
B5	IO13RSB0	D9	IO30RSB0	F13	IO62NDB1
B6	IO14RSB0	D10	IO40RSB0	F14	IO49RSB0
B7	IO21RSB0	D11	IO46RSB0	F15	IO64PPB1
B8	IO27RSB0	D12	GNDQ	F16	IO66NDB1
B9	IO32RSB0	D13	IO47RSB0	G1	IO148NDB3
B10	IO38RSB0	D14	GBB2/IO61PPB1	G2	IO148PDB3
B11	IO42RSB0	D15	IO53RSB0	G3	IO149PPB3
B12	GBC1/IO55RSB0	D16	IO63NDB1	G4	GFC1/IO147PPB3
B13	GBB0/IO56RSB0	E1	IO150PDB3	G5	VCCIB3
B14	IO44RSB0	E2	IO08RSB0	G6	VCC
B15	GBA2/IO60PDB1	E3	IO153VDB3	G7	GND
B16	IO60NDB1	E4	IO152VDB3	G8	GND
C1	IO154VDB3	E5	VMV0	G9	GND
C2	IO155VDB3	E6	VCCIB0	G10	GND
C3	IO11RSB0	E7	VCCIB0	G11	VCC
C4	IO07RSB0	E8	IO25RSB0	G12	VCCIB1

	FG256		FG256	FG256	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
H3	GFB1/IO208PPB3	K9	GND	M15	GDC1/IO111PDB1
H4	VCOMPLF	K10	GND	M16	IO107NDB1
H5	GFC0/IO209NPB3	K11	VCC	N1	IO194PSB3
H6	VCC	K12	VCCIB1	N2	IO192PPB3
H7	GND	K13	IO95NPB1	N3	GEC1/IO190PPB3
H8	GND	K14	IO100NPB1	N4	IO192NPB3
H9	GND	K15	IO102NDB1	N5	GNDQ
H10	GND	K16	IO102PDB1	N6	GEA2/IO187RSB2
H11	VCC	L1	IO202NDB3	N7	IO161RSB2
H12	GCC0/IO91NPB1	L2	IO202PDB3	N8	IO155RSB2
H13	GCB1/IO92PPB1	L3	IO196PPB3	N9	IO141RSB2
H14	GCA0/IO93NPB1	L4	IO193PPB3	N10	IO129RSB2
H15	IO96NPB1	L5	VCCIB3	N11	IO124RSB2
H16	GCB0/IO92NPB1	L6	GND	N12	GNDQ
J1	GFA2/IO206PSB3	L7	VCC	N13	IO110PDB1
J2	GFA1/IO207PDB3	L8	VCC	N14	VJTAG
J3	VCCPLF	L9	VCC	N15	GDC0/IO111NDB1
J4	IO205NDB3	L10	VCC	N16	GDA1/IO113PDB1
J5	GFB2/IO205PDB3	L11	GND	P1	GEB1/IO189PDB3
J6	VCC	L12	VCCIB1	P2	GEB0/IO189NDB3
J7	GND	L13	GDB0/IO112NPB1	P3	VMV2
J8	GND	L14	IO106NDB1	P4	IO179RSB2
J9	GND	L15	IO106PDB1	P5	IO171RSB2
J10	GND	L16	IO107PDB1	P6	IO165RSB2
J11	VCC	M1	IO197NSB3	P7	IO159RSB2
J12	GCB2/IO95PPB1	M2	IO196NPB3	P8	IO151RSB2
J13	GCA1/IO93PPB1	M3	IO193NPB3	P9	IO137RSB2
J14	GCC2/IO96PPB1	M4	GEC0/IO190NPB3	P10	IO134RSB2
J15	IO100PPB1	M5	VMV3	P11	IO128RSB2
J16	GCA2/IO94PSB1	M6	VCCIB2	P12	VMV1
K1	GFC2/IO204PDB3	M7	VCCIB2	P13	TCK
K2	IO204NDB3	M8	IO147RSB2	P14	VPUMP
K3	IO203NDB3	M9	IO136RSB2	P15	TRST
K4	IO203PDB3	M10	VCCIB2	P16	GDA0/IO113NDB1
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO188PDB3
K6	VCC	M12	VMV2	R2	GEA0/IO188NDB3
K7	GND	M13	IO110NDB1	R3	IO184RSB2
K8	GND	M14	GDB1/IO112PPB1	R4	GEC2/IO185RSB2



	FG484	FG484			
Pin Number	A3P400 Function	Pin Number	A3P400 Function		
R17	GDB1/IO78UPB1	U9	IO122RSB2		
R18	GDC1/IO77UDB1	U10	IO115RSB2		
R19	IO75NDB1	U11	IO110RSB2		
R20	VCC	U12	IO98RSB2		
R21	NC	U13	IO95RSB2		
R22	NC	U14	IO88RSB2		
T1	NC	U15	IO84RSB2		
T2	NC	U16	TCK		
Т3	NC	U17	VPUMP		
T4	IO140NDB3	U18	TRST		
Т5	IO138PPB3	U19	GDA0/IO79VDB1		
Т6	GEC1/IO137PPB3	U20	NC		
Τ7	IO131RSB2	U21	NC		
Т8	GNDQ	U22	NC		
Т9	GEA2/IO134RSB2	V1	NC		
T10	IO117RSB2	V2	NC		
T11	IO111RSB2	V3	GND		
T12	IO99RSB2	V4	GEA1/IO135PDB3		
T13	IO94RSB2	V5	GEA0/IO135NDB3		
T14	IO87RSB2	V6	IO127RSB2		
T15	GNDQ	V7	GEC2/IO132RSB2		
T16	IO93RSB2	V8	IO123RSB2		
T17	VJTAG	V9	IO118RSB2		
T18	GDC0/IO77VDB1	V10	IO112RSB2		
T19	GDA1/IO79UDB1	V11	IO106RSB2		
T20	NC	V12	IO100RSB2		
T21	NC	V13	IO96RSB2		
T22	NC	V14	IO89RSB2		
U1	NC	V15	IO85RSB2		
U2	NC	V16	GDB2/IO81RSB2		
U3	NC	V17	TDI		
U4	GEB1/IO136PDB3	V18	NC		
U5	GEB0/IO136NDB3	V19	TDO		
U6	VMV2	V20	GND		
U7	IO129RSB2	V21	NC		
U8	IO128RSB2	V22	NC		

	FG484				
Pin Number	A3P400 Function				
W1	NC				
W2	NC				
W3	NC				
W4	GND				
W5	IO126RSB2				
W6	GEB2/IO133RSB2				
W7	IO124RSB2				
W8	IO116RSB2				
W9	IO113RSB2				
W10	IO107RSB2				
W11	IO105RSB2				
W12	IO102RSB2				
W13	IO97RSB2				
W14	IO92RSB2				
W15	GDC2/IO82RSB2				
W16	IO86RSB2				
W17	GDA2/IO80RSB2				
W18	TMS				
W19	GND				
W20	NC				
W21	NC				
W22	NC				
Y1	VCCIB3				
Y2	NC				
Y3	NC				
Y4	NC				
Y5	GND				
Y6	NC				
¥7	NC				
Y8	VCC				
Y9	VCC				
Y10	NC				
Y11	NC				
Y12	NC				
Y13	NC				
Y14	VCC				



Datasheet Information

Maximum Junction Temperature, was changed to 100° from 110° in the nermal Characteristics" section and EQ 1. The calculated result of Maximum wer Allowed has thus changed to 1.463 W from 1.951 W. ues for the A3P015 device were added to Table 2-7 • Quiescent Supply rrent Characteristics. ues for the A3P015 device were added to Table 2-14 • Different Components ntributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was noved. Table 2-15 • Different Components Contributing to the Static Power nsumption in ProASIC3 Devices is new. e "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula m $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$. th fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 •	2-6 2-7 2-11, 2-12 2-14
ues for the A3P015 device were added to Table 2-7 • Quiescent Supply rrent Characteristics. ues for the A3P015 device were added to Table 2-14 • Different Components ntributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was noved. Table 2-15 • Different Components Contributing to the Static Power nsumption in ProASIC3 Devices is new. e "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula m $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$. th fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 •	2-7 2-11, 2-12 2-14
ues for the A3P015 device were added to Table 2-14 • Different Components ntributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was noved. Table 2-15 • Different Components Contributing to the Static Power nsumption in ProASIC3 Devices is new. e "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula m $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$. th fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 •	2-11, 2-12 2-14
e "PLL Contribution—PPLL" section was updated to change the P _{PLL} formula m P _{AC13} + P _{AC14} * F _{CLKOUT} to P _{DC4} + P _{AC13} * F _{CLKOUT} . th fall and rise values were included for t _{DDRISUD} and t _{DDRIHD} in Table 2-102 •	2-14
th fall and rise values were included for $t_{\mbox{DDRISUD}}$ and $t_{\mbox{DDRIHD}}$ in Table 2-102 \bullet	
ut DDR Propagation Delays.	2-78
ole 2-107 • A3P015 Global Resource is new.	2-86
e typical value for Delay Increments in Programmable Delay Blocks was anged from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
ble note references were added to Table 2-2 • Recommended Operating nditions 1, and the order of the table notes was changed.	2-2
e title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to nove "as measured on quiet I/Os." Table note 1 was revised to remove timated SSO density over cycles." Table note 2 was revised to remove "refers y to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
e "Power per I/O Pin" section was updated to include 3 additional tables taining to input buffer power and output buffer power.	2-7
ble 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include ues for 3.3 V PCI/PCI-X.	2-27
ble 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was dated.	2-66
numbers were added to the "QN68 – Bottom View" package diagram. Note 2 s added below the diagram.	4-3
e "QN132 – Bottom View" package diagram was updated to include D1 to D4. addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
s document was divided into two sections and given a version number, starting v1.0. The first section of the document includes features, benefits, ordering prmation, and temperature and speed grade offerings. The second section is a vice family overview.	N/A
s document was updated to include A3P015 device information. QN68 is a w package that was added because it is offered in the A3P015. The following ctions were updated: eatures and Benefits" oASIC3 Ordering Information" emperature Grade Offerings" oASIC3 Flash Family FPGAs" BP015 and A3P030" note	N/A
$rac{1}{2}$	t DDR Propagation Delays. a 2-107 • A3P015 Global Resource is new. typical value for Delay Increments in Programmable Delay Blocks was iged from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification. a note references were added to Table 2-2 • Recommended Operating ditions 1, and the order of the table notes was changed. title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to ove "as measured on quiet I/Os." Table note 1 was revised to remove mated SSO density over cycles." Table note 2 was revised to remove "refers to overshoot/undershoot limits for simultaneous switching I/Os." "Power per I/O Pin" section was updated to include 3 additional tables aining to input buffer power and output buffer power. a 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include as for 3.3 V PCI/PCI-X. a 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was ted. umbers were added to the "QN68 – Bottom View" package diagram. Note 2 added below the diagram. "QN132 – Bottom View" package diagram was updated to include D1 to D4. Idition, note 1 was changed from top view to bottom view, and note 2 is new. document was divided into two sections and given a version number, starting 10. The first section of the document includes features, benefits, ordering mation, and temperature and speed grade offerings. The second section is a ce family overview. document was updated to include A3P015 device information. QN68 is a package that was added because it is offered in the A3P015. The following ons were updated: tures and Benefits" ASIC3 Ordering Information" perature Grade Offerings" ASIC3 Flash Family FPGAs" 2015 and A3P030" note



Datasheet Information

Revision	Changes	Page
v2.0 (April 2007)	In the "Packaging Tables", Ambient was deleted.	ii
	The timing characteristics tables were updated.	N/A
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-11 • ProASIC3 CCC/PLL Specification was updated.	2-29
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	PCI-X 3.3 V was added to Table 2-11 • VCCI Voltages and Compatible Standards.	2-29
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 \cdot Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	V _{JTAG} was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1.	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951.	3-5
	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-6
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated.	3-17 to 3- 17



Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumptionin ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21

Revision	Changes	Page
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68