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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-1pqg208

RAM Contribution— P_{MEMORY}

$$P_{\text{MEMORY}} = P_{\text{AC11}} * N_{\text{BLOCKS}} * F_{\text{READ-CLOCK}} * \beta_2 + P_{\text{AC12}} * N_{\text{BLOCK}} * F_{\text{WRITE-CLOCK}} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{\text{READ-CLOCK}}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{\text{WRITE-CLOCK}}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-17 on page 2-14](#).

PLL Contribution— P_{PLL}

$$P_{\text{PLL}} = P_{\text{DC4}} + P_{\text{AC13}} * F_{\text{CLKOUT}}$$

F_{CLKOUT} is the output clock frequency.¹

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + ... + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-16 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-17 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{\text{AC14}} * F_{\text{CLKOUT}}$ product) to the total PLL contribution.

I/O DC Characteristics

Table 2-27 • Input Capacitance

Symbol	Definition	Conditions	Min	Max	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, $f = 1.0$ MHz	–	8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, $f = 1.0$ MHz	–	8	pF

Table 2-28 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN} (\Omega)^2$	$R_{PULL-UP} (\Omega)^3$
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
3.3 V LVCMOS Wide Range ⁴	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
 Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	15.86	0.04	1.54	0.43	15.86	13.51	4.09	3.80	19.25	16.90	ns
		–1	0.51	13.49	0.04	1.31	0.36	13.49	11.49	3.48	3.23	16.38	14.38	ns
		–2	0.45	11.84	0.03	1.15	0.32	11.84	10.09	3.05	2.84	14.38	12.62	ns
100 μA	4 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	6 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	8 mA	Std.	0.60	8.63	0.04	1.54	0.43	8.63	7.39	4.96	5.28	12.02	10.79	ns
		–1	0.51	7.34	0.04	1.31	0.36	7.34	6.29	4.22	4.49	10.23	9.18	ns
		–2	0.45	6.44	0.03	1.15	0.32	6.44	5.52	3.70	3.94	8.98	8.06	ns
100 μA	16 mA	Std.	0.60	8.05	0.04	1.54	0.43	8.05	6.93	5.03	5.43	11.44	10.32	ns
		–1	0.51	6.85	0.04	1.31	0.36	6.85	5.90	4.28	4.62	9.74	8.78	ns
		–2	0.45	6.01	0.03	1.15	0.32	6.01	5.18	3.76	4.06	8.55	7.71	ns
100 μA	24 mA	Std.	0.60	7.50	0.04	1.54	0.43	7.50	6.90	5.13	6.00	10.89	10.29	ns
		–1	0.51	6.38	0.04	1.31	0.36	6.38	5.87	4.36	5.11	9.27	8.76	ns
		–2	0.45	5.60	0.03	1.15	0.32	5.60	5.15	3.83	4.48	8.13	7.69	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Characteristics

Table 2-60 • 2.5 V LVC MOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	–1	0.51	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	–2	0.45	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
6 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
8 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.60	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.51	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.60	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	–1	0.51	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	–2	0.45	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.60	3.09	0.04	1.31	0.43	3.15	2.44	3.44	4.00	5.38	4.68	ns
	–1	0.51	2.63	0.04	1.11	0.36	2.68	2.08	2.92	3.40	4.58	3.98	ns
	–2	0.45	2.31	0.03	0.98	0.32	2.35	1.82	2.57	2.98	4.02	3.49	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-68 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

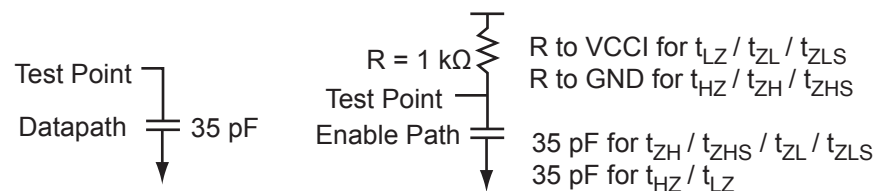


Figure 2-9 • AC Loading

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	35

Note: *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.

Table 2-81 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-82 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

- Software default selection highlighted in gray.
- For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. [Figure 2-28](#) is an example of a global tree used for clock routing. The global tree presented in [Figure 2-28](#) is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

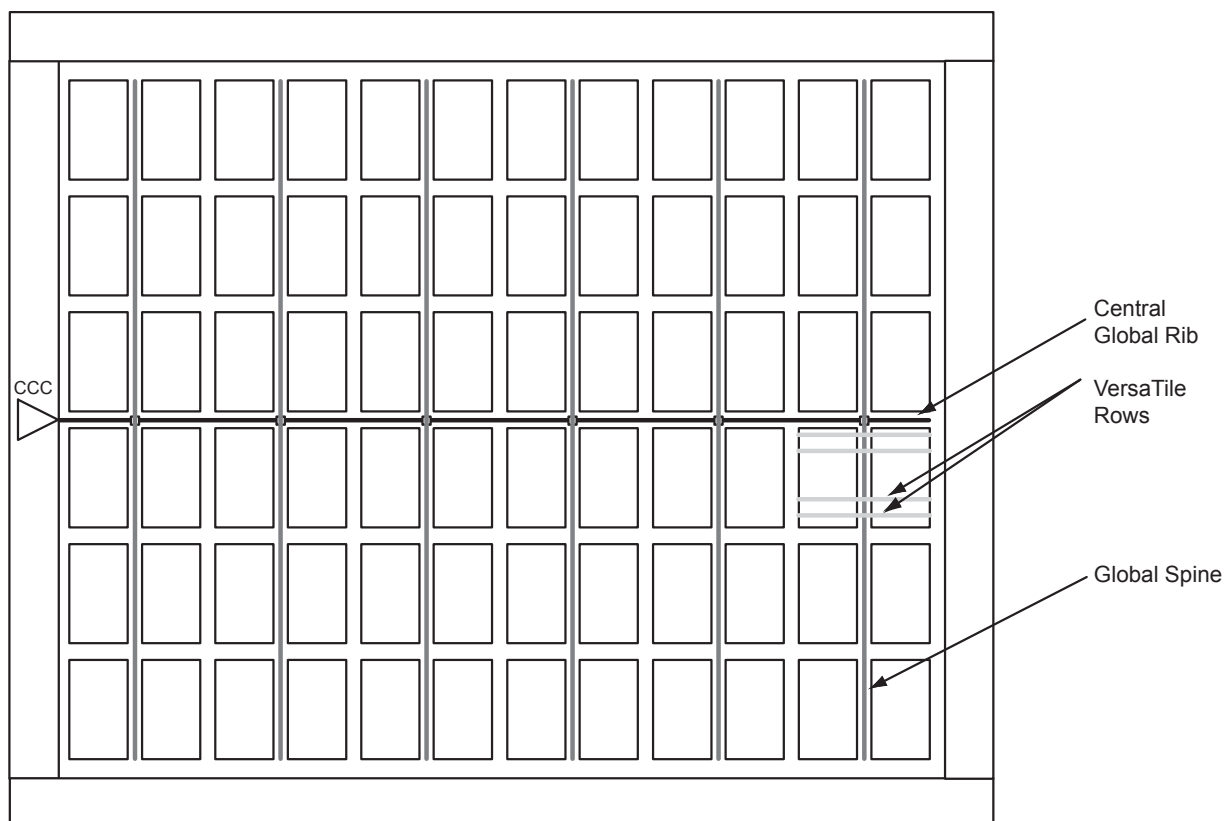


Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the ["Clock Conditioning Circuits" section on page 2-90](#). [Table 2-108](#) to [Table 2-114 on page 2-89](#) present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

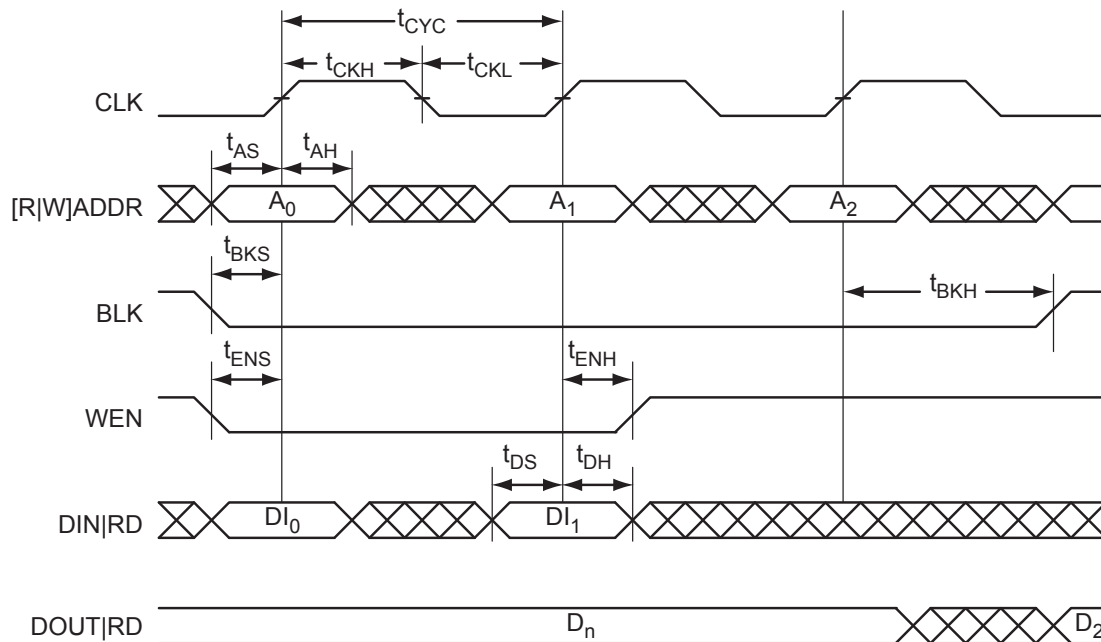


Figure 2-33 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

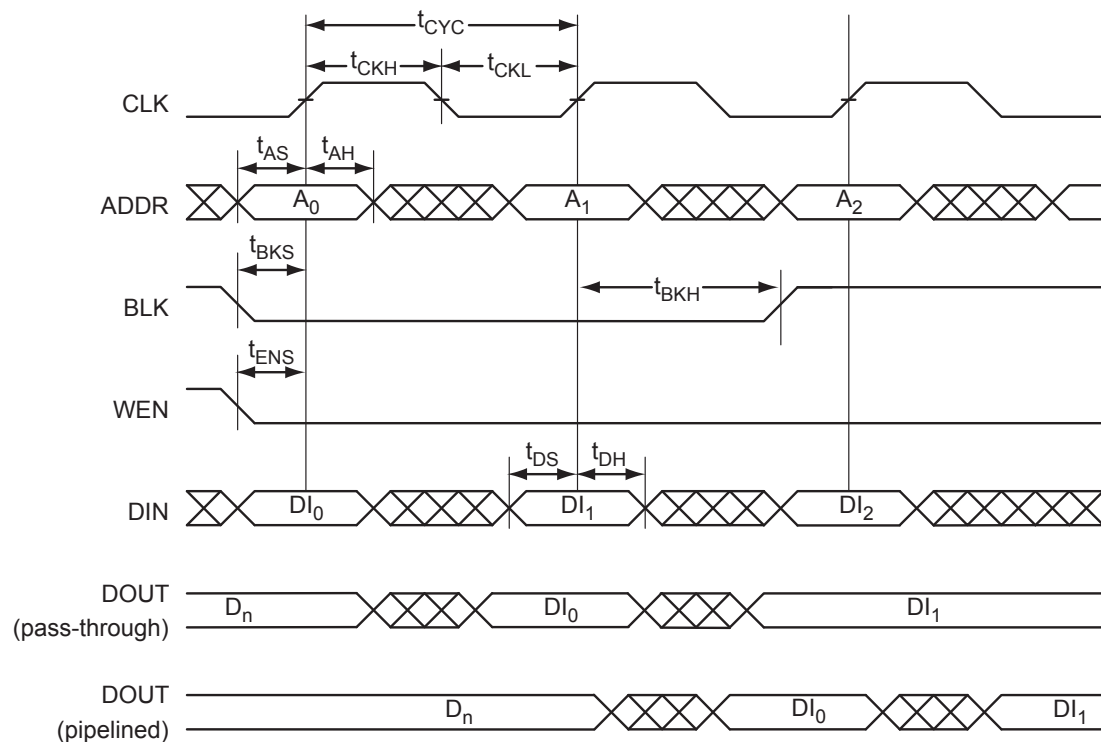


Figure 2-34 • RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.

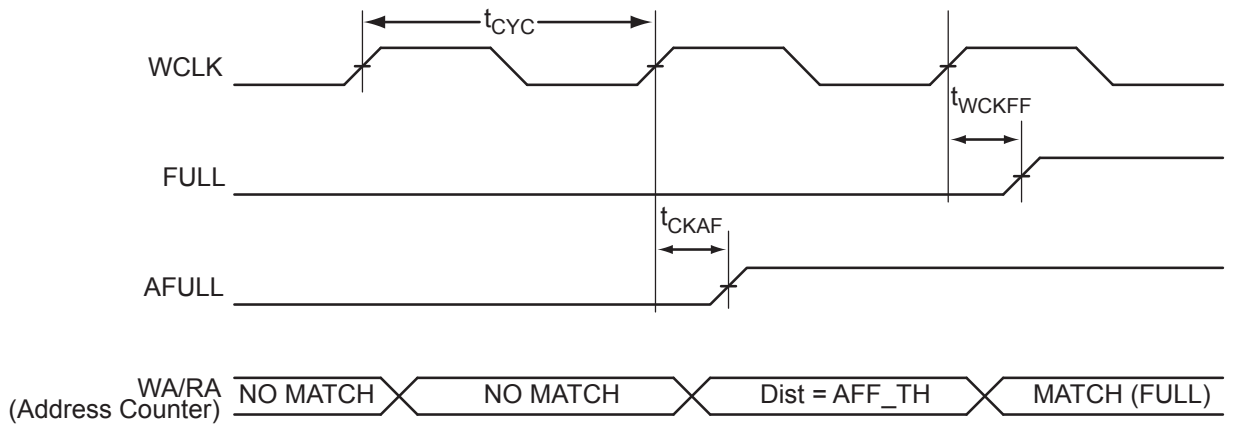


Figure 2-41 • FIFO FULL Flag and AFULL Flag Assertion

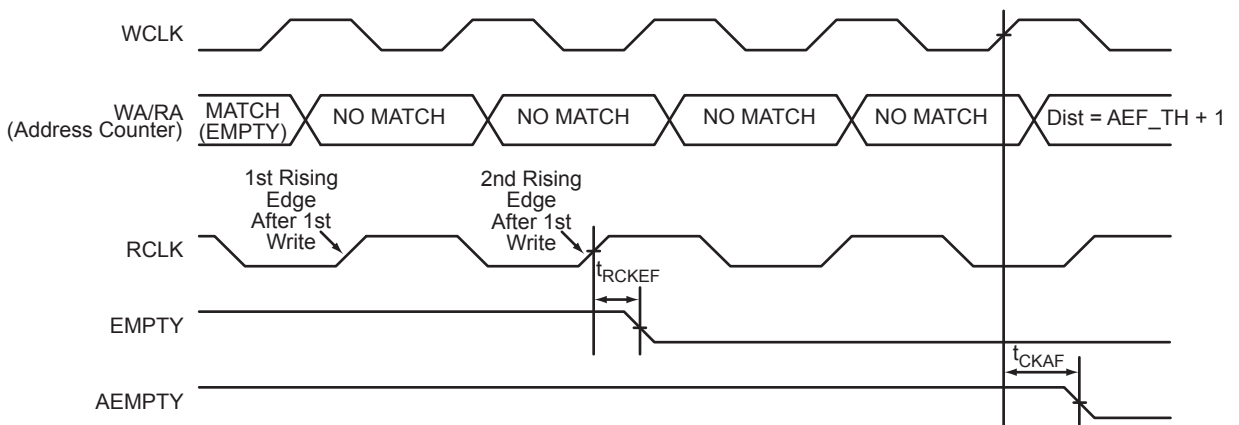


Figure 2-42 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

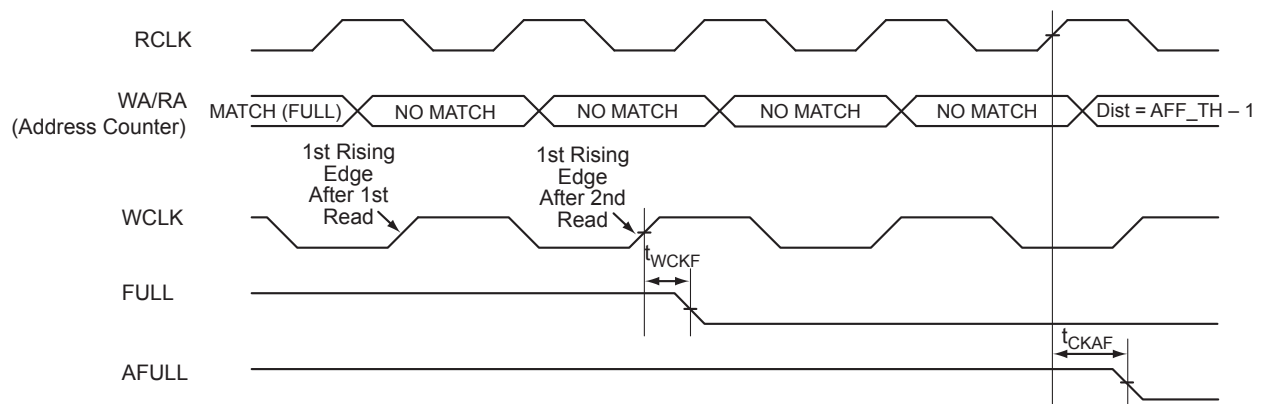


Figure 2-43 • FIFO FULL Flag and AFULL Flag Deassertion

Table 2-119 • FIFO (for A3P250 only, aspect-ratio-dependent)
Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.26	3.71	4.36	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

3 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on ProASIC3 devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC3 devices.

VQ100	
Pin Number	A3P250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO112PSB3
9	GND
10	GFB1/IO109PDB3
11	GFB0/IO109NDB3
12	VCOMPLF
13	GFA0/IO108NPB3
14	VCCPLF
15	GFA1/IO108PPB3
16	GFA2/IO107PSB3
17	VCC
18	VCCIB3
19	GFC2/IO105PSB3
20	GEC1/IO100PDB3
21	GEC0/IO100NDB3
22	GEA1/IO98PDB3
23	GEA0/IO98NDB3
24	VMV3
25	GNDQ
26	GEA2/IO97RSB2
27	GEB2/IO96RSB2
28	GEC2/IO95RSB2
29	IO93RSB2
30	IO92RSB2
31	IO91RSB2
32	IO90RSB2
33	IO88RSB2
34	IO86RSB2
35	IO85RSB2
36	IO84RSB2

VQ100	
Pin Number	A3P250 Function
37	VCC
38	GND
39	VCCIB2
40	IO77RSB2
41	IO74RSB2
42	IO71RSB2
43	GDC2/IO63RSB2
44	GDB2/IO62RSB2
45	GDA2/IO61RSB2
46	GNDQ
47	TCK
48	TDI
49	TMS
50	VMV2
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO60USB1
58	GDC0/IO58VDB1
59	GDC1/IO58UDB1
60	IO52NDB1
61	GCB2/IO52PDB1
62	GCA1/IO50PDB1
63	GCA0/IO50NDB1
64	GCC0/IO48NDB1
65	GCC1/IO48PDB1
66	VCCIB1
67	GND
68	VCC
69	IO43NDB1
70	GBC2/IO43PDB1
71	GBB2/IO42PSB1
72	IO41NDB1

VQ100	
Pin Number	A3P250 Function
73	GBA2/IO41PDB1
74	VMV1
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO29RSB0
83	IO27RSB0
84	IO25RSB0
85	IO23RSB0
86	IO21RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	GAC1/IO05RSB0
94	GAC0/IO04RSB0
95	GAB1/IO03RSB0
96	GAB0/IO02RSB0
97	GAA1/IO01RSB0
98	GAA0/IO00RSB0
99	GNDQ
100	VMV0

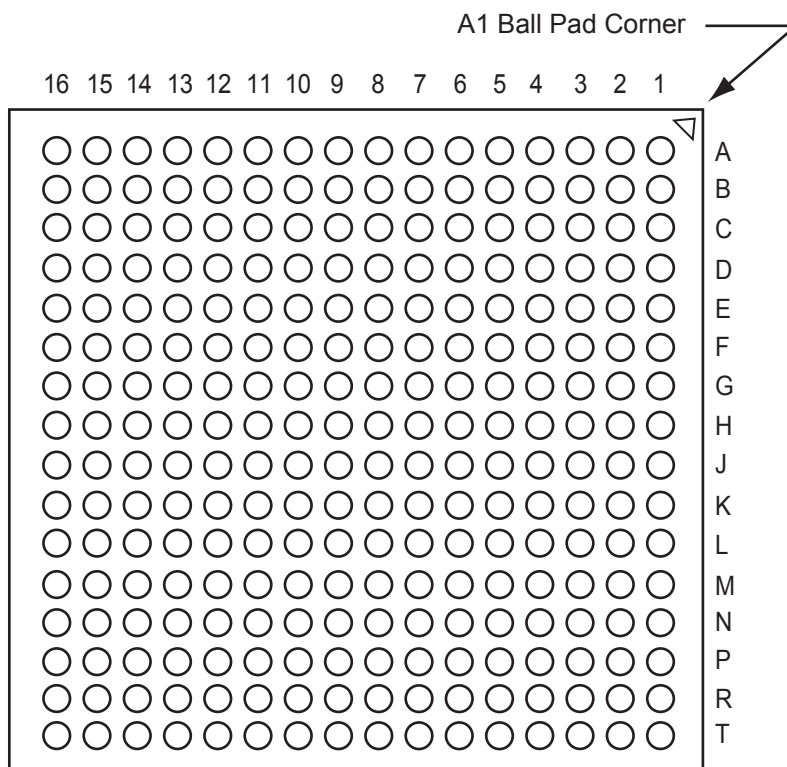
FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG144	
Pin Number	A3P250 Function
K1	GEBO/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	GEB2/IO96RSB2
L4	IO91RSB2
L5	VCCIB2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256 – Bottom View



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

FG256	
Pin Number	A3P1000 Function
H3	GFB1/IO208PPB3
H4	VCOMPLF
H5	GFC0/IO209NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO91NPB1
H13	GCB1/IO92PPB1
H14	GCA0/IO93NPB1
H15	IO96NPB1
H16	GCB0/IO92NPB1
J1	GFA2/IO206PSB3
J2	GFA1/IO207PDB3
J3	VCCPLF
J4	IO205NDB3
J5	GFB2/IO205PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO95PPB1
J13	GCA1/IO93PPB1
J14	GCC2/IO96PPB1
J15	IO100PPB1
J16	GCA2/IO94PSB1
K1	GFC2/IO204PDB3
K2	IO204NDB3
K3	IO203NDB3
K4	IO203PDB3
K5	VCCIB3
K6	VCC
K7	GND
K8	GND

FG256	
Pin Number	A3P1000 Function
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO95NPB1
K14	IO100NPB1
K15	IO102NDB1
K16	IO102PDB1
L1	IO202NDB3
L2	IO202PDB3
L3	IO196PPB3
L4	IO193PPB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO112NPB1
L14	IO106NDB1
L15	IO106PDB1
L16	IO107PDB1
M1	IO197NSB3
M2	IO196NPB3
M3	IO193NPB3
M4	GEC0/IO190NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO147RSB2
M9	IO136RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO110NDB1
M14	GDB1/IO112PPB1

FG256	
Pin Number	A3P1000 Function
M15	GDC1/IO111PDB1
M16	IO107NDB1
N1	IO194PSB3
N2	IO192PPB3
N3	GEC1/IO190PPB3
N4	IO192NPB3
N5	GNDQ
N6	GEA2/IO187RSB2
N7	IO161RSB2
N8	IO155RSB2
N9	IO141RSB2
N10	IO129RSB2
N11	IO124RSB2
N12	GNDQ
N13	IO110PDB1
N14	VJTAG
N15	GDC0/IO111NDB1
N16	GDA1/IO113PDB1
P1	GEB1/IO189PDB3
P2	GEB0/IO189NDB3
P3	VMV2
P4	IO179RSB2
P5	IO171RSB2
P6	IO165RSB2
P7	IO159RSB2
P8	IO151RSB2
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2

FG484	
Pin Number	A3P400 Function
K19	IO73NDB1
K20	NC
K21	NC
K22	NC
L1	NC
L2	NC
L3	NC
L4	GFB0/IO146NPB3
L5	GFA0/IO145NDB3
L6	GFB1/IO146PPB3
L7	VCOMPLF
L8	GFC0/IO147NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO67NPB1
L16	GCB1/IO68PPB1
L17	GCA0/IO69NPB1
L18	NC
L19	GCB0/IO68NPB1
L20	NC
L21	NC
L22	NC
M1	NC
M2	NC
M3	NC
M4	GFA2/IO144PPB3
M5	GFA1/IO145PDB3
M6	VCCPLF
M7	IO143NDB3
M8	GFB2/IO143PDB3
M9	VCC
M10	GND

FG484	
Pin Number	A3P400 Function
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO71PPB1
M16	GCA1/IO69PPB1
M17	GCC2/IO72PPB1
M18	NC
M19	GCA2/IO70PDB1
M20	NC
M21	NC
M22	NC
N1	NC
N2	NC
N3	NC
N4	GFC2/IO142PDB3
N5	IO144NPB3
N6	IO141PPB3
N7	IO120RSB2
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO71NPB1
N17	IO74RSB1
N18	IO72NPB1
N19	IO70NDB1
N20	NC
N21	NC
N22	NC
P1	NC
P2	NC

FG484	
Pin Number	A3P400 Function
P3	NC
P4	IO142NDB3
P5	IO141NPB3
P6	IO125RSB2
P7	IO139RSB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO78VPB1
P17	IO76VDB1
P18	IO76UDB1
P19	IO75PDB1
P20	NC
P21	NC
P22	NC
R1	NC
R2	NC
R3	VCC
R4	IO140PDB3
R5	IO130RSB2
R6	IO138NPB3
R7	GEC0/IO137NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO108RSB2
R12	IO101RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO83RSB2

FG484	
Pin Number	A3P600 Function
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2

FG484	
Pin Number	A3P600 Function
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND

Revision	Changes	Page
Revision 10 (September 2011)	The "In-System Programming (ISP) and Security" section and Security section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865).	I
	The value of 34 I/Os for the QN48 package in A3P030 was added to the "I/Os Per Package 1" section (SAR 33907).	III
	The Y security option and Licensed DPA Logo were added to the "ProASIC3 Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151).	IV
	The "Specifying I/O States During Programming" section is new (SAR 21281).	1-7
	In Table 2-2 • Recommended Operating Conditions 1, VPUMP programming voltage in programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45" (SAR 30666). It was corrected in v2.0 of this datasheet in April 2007 but inadvertently changed back to "3.0 to 3.6 V" in v1.4 in August 2009. The following changes were made to Table 2-2 • Recommended Operating Conditions 1: VCCPLL analog power supply (PLL) was changed from "1.4 to 1.6" to "1.425 to 1.575" (SAR 33850). For VCCI and VMV, values for 3.3 V DC and 3.3 V DC Wide Range were corrected. The correct value for 3.3 V DC is "3.0 to 3.6 V" and the correct value for 3.3 V Wide Range is "2.7 to 3.6" (SAR 33848).	2-2
	Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings was update to restore values to the correct columns. Previously the Slew Rate column was missing and data were aligned incorrectly (SAR 34034).	2-24
	The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section and "3.3 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is $\pm 100 \mu\text{A}$. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700).	2-22, 2-39