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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	100000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-2pqg208

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flashbased, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure



Note: *Not supported by A3P015 and A3P030 devices



† The A3P015 and A3P030 do not support PLL or SRAM.



I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

		I/C	O Standards	Supported
I/O Bank Type	Device and Bank Location	LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west Banks of A3P250 and larger devices	\checkmark	\checkmark	\checkmark
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	\checkmark	\checkmark	Not supported
Standard	All banks of A3P015 and A3P030	\checkmark	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a poweredup system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

- Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.
 - 1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
 - 2. From the FlashPro GUI, click PDB Configuration. A FlashPoint Programming File Generator window appears.
 - 3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
 - 4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
 - 5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:
 - 1 I/O is set to drive out logic High

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Typical (25°C)	2 mA	2 mA	2 mA	2 mA	3 mA	3 mA	5 mA	8 mA
Max. (Commercial)	10 mA	10 mA	10 mA	10 mA	20 mA	20 mA	30 mA	50 mA
Max. (Industrial)	15 mA	15 mA	15 mA	15 mA	30 mA	30 mA	45 mA	75 mA

Note: IDD Includes VCC, VPUMP, VCCI, and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-11 and Table 2-12 on page 2-9.

Power per I/O Pin

Table 2-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Advanced I/O Banks

	VMV (V)	Static Power P _{DC2} (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Single-Ended		1	
3.3 V LVTTL / 3.3 V LVCMOS	3.3	-	16.22
3.3 V LVCMOS Wide Range ³	3.3	-	16.22
2.5 V LVCMOS	2.5	-	5.12
1.8 V LVCMOS	1.8	-	2.13
1.5 V LVCMOS (JESD8-11)	1.5	-	1.45
3.3 V PCI	3.3	-	18.11
3.3 V PCI-X	3.3	-	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

- 1. PDC2 is the static power (where applicable) measured on VMV.
- 2. PAC9 is the total dynamic power measured on VCC and VMV.
- 3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (µW/MHz) ²
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	_	16.23
3.3 V LVCMOS Wide Range ³	3.3	-	16.23

Notes:

- 1. PDC2 is the static power (where applicable) measured on VMV.
- 2. PAC9 is the total dynamic power measured on VCC and VMV.
- 3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.



	Definition	Device Specific Static Power (mW)									
Parameter		A3P1000	A3P600	A3P400	A3P250	A3P125	A3P060	A3P030	A3P015		
PDC1	Array static power in Active mode	See Table 2-7 on page 2-7.									
PDC2	I/O input pin static power (standard-dependent)	See Table 2-8 on page 2-7 through Table 2-10 on page 2-8.									
PDC3	I/O output pin static power (standard-dependent)	See Table 2-11 on page 2-9 through Table 2-13 on page 2-10.									
PDC4	Static PLL contribution	2.55 mW									
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-7 on page 2-7.									

Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices

Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi Power spreadsheet calculator or SmartPower tool in Libero SoC software.

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- · The number of combinatorial and sequential cells used in the design
- · The internal clock frequencies
- The number and the standard of I/O pins used in the design
- · The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-17 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—PTOTAL

 $P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

 $P_{STAT} = P_{DC1} + N_{INPUTS} + P_{DC2} + N_{OUTPUTS} + P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

N_{OUTPUTS} is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}

Global Clock Contribution—P_{CLOCK}

 $P_{CLOCK} = (P_{AC1} + N_{SPINE}*P_{AC2} + N_{ROW}*P_{AC3} + N_{S-CELL}*P_{AC4})*F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

Table 2-55 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
100 µA	2 mA	Std.	0.60	14.64	0.04	1.52	0.43	14.64	12.97	3.21	3.15	ns
		-1	0.51	12.45	0.04	1.29	0.36	12.45	11.04	2.73	2.68	ns
		-2	0.45	10.93	0.03	1.13	0.32	10.93	9.69	2.39	2.35	ns
100 µA	4 mA	Std.	0.60	14.64	0.04	1.52	0.43	14.64	12.97	3.21	3.15	ns
		-1	0.51	12.45	0.04	1.29	0.36	12.45	11.04	2.73	2.68	ns
		-2	0.45	10.93	0.03	1.13	0.32	10.93	9.69	2.39	2.35	ns
100 µA	6 mA	Std.	0.60	10.16	0.04	1.52	0.43	10.16	9.08	3.71	3.98	ns
		-1	0.51	8.64	0.04	1.29	0.36	8.64	7.73	3.15	3.39	ns
		-2	0.45	7.58	0.03	1.13	0.32	7.58	6.78	2.77	2.97	ns
100 µA	8 mA	Std.	0.60	10.16	0.04	1.52	0.43	10.16	9.08	3.71	3.98	ns
		-1	0.51	8.64	0.04	1.29	0.36	8.64	7.73	3.15	3.39	ns
		-2	0.45	7.58	0.03	1.13	0.32	7.58	6.78	2.77	2.97	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100 \ \mu$ A. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



Table 2-58 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

2.5 V LVCMOS VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²	
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.



Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Low (V) Input High (V)		C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.



1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	8	8	51	45	10	10
12 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	12	12	74	91	10	10
16 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI-0.45	16	16	74	91	10	10

Table 2-66 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

4. Currents are measured at 85°C junction temperature.

5. Software default selection highlighted in gray.

Table 2-67 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	VIL		VIL VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI - 0.45	8	8	44	35	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.



	Applicable to otanidate i has no builds											
1.5 V LVCMOS		VIL	VIH	VIH		VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10

Table 2-77 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

Notes:

- 1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
- 2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Table 2-78 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.5 V LVCMOS		VIL	VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.



Figure 2-10 • AC Loading

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-22 for a complete table of trip points.



Timing Characteristics

Table 2-80 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{zLS}	t _{zHS}	Units
2 mA	Std.	0.66	8.36	0.04	1.44	0.43	6.82	8.36	3.39	2.77	9.06	10.60	ns
	-1	0.56	7.11	0.04	1.22	0.36	5.80	7.11	2.88	2.35	7.71	9.02	ns
	-2	0.49	6.24	0.03	1.07	0.32	5.10	6.24	2.53	2.06	6.76	7.91	ns
4 mA	Std.	0.66	5.31	0.04	1.44	0.43	4.85	5.31	3.74	3.40	7.09	7.55	ns
	-1	0.56	4.52	0.04	1.22	0.36	4.13	4.52	3.18	2.89	6.03	6.42	ns
	-2	0.49	3.97	0.03	1.07	0.32	3.62	3.97	2.79	2.54	5.29	5.64	ns
6 mA	Std.	0.66	4.67	0.04	1.44	0.43	4.55	4.67	3.82	3.56	6.78	6.90	ns
	-1	0.56	3.97	0.04	1.22	0.36	3.87	3.97	3.25	3.03	5.77	5.87	ns
	-2	0.49	3.49	0.03	1.07	0.32	3.40	3.49	2.85	2.66	5.07	5.16	ns
8 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
12 mA	Std.	0.66	4.08	0.04	1.44	0.43	4.15	3.58	3.94	4.20	6.39	5.81	ns
	-1	0.56	3.47	0.04	1.22	0.36	3.53	3.04	3.36	3.58	5.44	4.95	ns
	-2	0.49	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



DC Parameter	Description	Min.	Тур.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL ¹	Output Lower Current	0.65	0.91	1.16	mA
IOH ¹	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH ^{2,3}	Input High Leakage Current			10	μA
IIL ^{2,4}	Input Low Leakage Current			10	μA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels

Notes:

1. IOL/IOH defined by VODIFF/(Resistor Network)

2. Currents are measured at 85°C junction temperature.

- 3. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <VCCI. Input current is larger when operating outside recommended ranges.
- 4. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN <VIL.

Table 2-91 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)		
1.075	1.325	Cross point		

Note: *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-92 • LVDS

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	Units
Std.	0.66	1.83	0.04	1.60	ns
-1	0.56	1.56	0.04	1.36	ns
-2	0.49	1.37	0.03	1.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to highperformance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-92.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60 \Omega$ and $R_T = 70 \Omega$, given $Z_0 = 50 \Omega$ (2") and $Z_{stub} = 50 \Omega$ (~1.5").





LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.









Figure 2-27 • Timing Model and Waveforms

Timing Characteristics

Table 2-106 • Register Delays

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t _{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t _{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t _{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t _{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t _{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t _{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t _{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t _{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t _{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t _{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t _{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t _{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t _{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t _{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.





Figure 2-40 • FIFO EMPTY Flag and AEMPTY Flag Assertion



JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

Table 2-125 • JTAG 1532

```
Commercial-Case Conditions: T<sub>J</sub> = 70°C, Worst-Case VCC = 1.425 V
```

Parameter	Description	-2	-1	Std.	Units
t _{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t _{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t _{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t _{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t _{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t _{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F _{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t _{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t _{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t _{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.



C	CS121
Pin Number	A3P060 Function
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1



F	G256		FG256	FG256		
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function	
A1	GND	C5	GAC0/IO04RSB0	E9	IO24RSB0	
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	VCCIB0	
A3	GAA1/IO01RSB0	C7	IO13RSB0	E11	VCCIB0	
A4	GAB0/IO02RSB0	C8	IO17RSB0	E12	VMV1	
A5	IO07RSB0	C9	IO22RSB0	E13	GBC2/IO43PDB1	
A6	IO10RSB0	C10	IO27RSB0	E14	IO46RSB1	
A7	IO11RSB0	C11	IO31RSB0	E15	NC	
A8	IO15RSB0	C12	GBC0/IO35RSB0	E16	IO45PDB1	
A9	IO20RSB0	C13	IO34RSB0	F1	IO113NDB3	
A10	IO25RSB0	C14	NC	F2	IO112PPB3	
A11	IO29RSB0	C15	IO42NPB1	F3	NC	
A12	IO33RSB0	C16	IO44PDB1	F4	IO115VDB3	
A13	GBB1/IO38RSB0	D1	IO114VDB3	F5	VCCIB3	
A14	GBA0/IO39RSB0	D2	IO114UDB3	F6	GND	
A15	GBA1/IO40RSB0	D3	GAC2/IO116UDB3	F7	VCC	
A16	GND	D4	NC	F8	VCC	
B1	GAB2/IO117UDB3	D5	GNDQ	F9	VCC	
B2	GAA2/IO118UDB3	D6	IO08RSB0	F10	VCC	
B3	NC	D7	IO14RSB0	F11	GND	
B4	GAB1/IO03RSB0	D8	IO18RSB0	F12	VCCIB1	
B5	IO06RSB0	D9	IO23RSB0	F13	IO43NDB1	
B6	IO09RSB0	D10	IO28RSB0	F14	NC	
B7	IO12RSB0	D11	IO32RSB0	F15	IO47PPB1	
B8	IO16RSB0	D12	GNDQ	F16	IO45NDB1	
B9	IO21RSB0	D13	NC	G1	IO111NDB3	
B10	IO26RSB0	D14	GBB2/IO42PPB1	G2	IO111PDB3	
B11	IO30RSB0	D15	NC	G3	IO112NPB3	
B12	GBC1/IO36RSB0	D16	IO44NDB1	G4	GFC1/IO110PPB3	
B13	GBB0/IO37RSB0	E1	IO113PDB3	G5	VCCIB3	
B14	NC	E2	NC	G6	VCC	
B15	GBA2/IO41PDB1	E3	IO116VDB3	G7	GND	
B16	IO41NDB1	E4	IO115UDB3	G8	GND	
C1	IO117VDB3	E5	VMV0	G9	GND	
C2	IO118VDB3	E6	VCCIB0	G10	GND	
C3	NC	E7	VCCIB0	G11	VCC	
C.4	NIC	EQ	IO198580	G12	VCCIB1	



	FG256
Pin Number	A3P250 Function
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
Т3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
Т8	IO79RSB2
Т9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

FG256		
Pin Number	A3P250 Function	
T13	IO67RSB2	
T14	GDA2/IO61RSB2	
T15	TMS	
T16	GND	



Package Pin Assignments

FG256		
Pin Number	A3P1000 Function	
R5	IO168RSB2	
R6	IO163RSB2	
R7	IO157RSB2	
R8	IO149RSB2	
R9	IO143RSB2	
R10	IO138RSB2	
R11	IO131RSB2	
R12	IO125RSB2	
R13	GDB2/IO115RSB2	
R14	TDI	
R15	GNDQ	
R16	TDO	
T1	GND	
T2	IO183RSB2	
Т3	GEB2/IO186RSB2	
T4	IO172RSB2	
T5	IO170RSB2	
T6	IO164RSB2	
T7	IO158RSB2	
Т8	IO153RSB2	
Т9	IO142RSB2	
T10	IO135RSB2	
T11	IO130RSB2	
T12	GDC2/IO116RSB2	
T13	IO120RSB2	
T14	GDA2/IO114RSB2	
T15	TMS	
T16	GND	



FG484		FG484	
Pin Number	A3P400 Function	Pin Number	A3P400 Function
R17	GDB1/IO78UPB1	U9	IO122RSB2
R18	GDC1/IO77UDB1	U10	IO115RSB2
R19	IO75NDB1	U11	IO110RSB2
R20	VCC	U12	IO98RSB2
R21	NC	U13	IO95RSB2
R22	NC	U14	IO88RSB2
T1	NC	U15	IO84RSB2
T2	NC	U16	ТСК
Т3	NC	U17	VPUMP
T4	IO140NDB3	U18	TRST
Т5	IO138PPB3	U19	GDA0/IO79VDB1
Т6	GEC1/IO137PPB3	U20	NC
Τ7	IO131RSB2	U21	NC
Т8	GNDQ	U22	NC
Т9	GEA2/IO134RSB2	V1	NC
T10	IO117RSB2	V2	NC
T11	IO111RSB2	V3	GND
T12	IO99RSB2	V4	GEA1/IO135PDB3
T13	IO94RSB2	V5	GEA0/IO135NDB3
T14	IO87RSB2	V6	IO127RSB2
T15	GNDQ	V7	GEC2/IO132RSB2
T16	IO93RSB2	V8	IO123RSB2
T17	VJTAG	V9	IO118RSB2
T18	GDC0/IO77VDB1	V10	IO112RSB2
T19	GDA1/IO79UDB1	V11	IO106RSB2
T20	NC	V12	IO100RSB2
T21	NC	V13	IO96RSB2
T22	NC	V14	IO89RSB2
U1	NC	V15	IO85RSB2
U2	NC	V16	GDB2/IO81RSB2
U3	NC	V17	TDI
U4	GEB1/IO136PDB3	V18	NC
U5	GEB0/IO136NDB3	V19	TDO
U6	VMV2	V20	GND
U7	IO129RSB2	V21	NC
U8	IO128RSB2	V22	NC

FG484		
Pin Number	A3P400 Function	
W1	NC	
W2	NC	
W3	NC	
W4	GND	
W5	IO126RSB2	
W6	GEB2/IO133RSB2	
W7	IO124RSB2	
W8	IO116RSB2	
W9	IO113RSB2	
W10	IO107RSB2	
W11	IO105RSB2	
W12	IO102RSB2	
W13	IO97RSB2	
W14	IO92RSB2	
W15	GDC2/IO82RSB2	
W16	IO86RSB2	
W17	GDA2/IO80RSB2	
W18	TMS	
W19	GND	
W20	NC	
W21	NC	
W22	NC	
Y1	VCCIB3	
Y2	NC	
Y3	NC	
Y4	NC	
Y5	GND	
Y6	NC	
Y7	NC	
Y8	VCC	
Y9	VCC	
Y10	NC	
Y11	NC	
Y12	NC	
Y13	NC	
Y14	VCC	

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Package Pin Assignments

FG484		
Pin Number	A3P400 Function	
Y15	VCC	
Y16	NC	
Y17	NC	
Y18	GND	
Y19	NC	
Y20	NC	
Y21	NC	
Y22	VCCIB1	
AA1	GND	
AA2	VCCIB3	
AA3	NC	
AA4	NC	
AA5	NC	
AA6	NC	
AA7	NC	
AA8	NC	
AA9	NC	
AA10	NC	
AA11	NC	
AA12	NC	
AA13	NC	
AA14	NC	
AA15	NC	
AA16	NC	
AA17	NC	
AA18	NC	
AA19	NC	
AA20	NC	
AA21	VCCIB1	
AA22	GND	
AB1	GND	
AB2	GND	
AB3	VCCIB2	
AB4	NC	
AB5	NC	
AB6	IO121RSB2	

FG484		
Pin Number	A3P400 Function	
AB7	IO119RSB2	
AB8	IO114RSB2	
AB9	IO109RSB2	
AB10	NC	
AB11	NC	
AB12	IO104RSB2	
AB13	IO103RSB2	
AB14	NC	
AB15	NC	
AB16	IO91RSB2	
AB17	IO90RSB2	
AB18	NC	
AB19	NC	
AB20	VCCIB2	
AB21	GND	
AB22	GND	