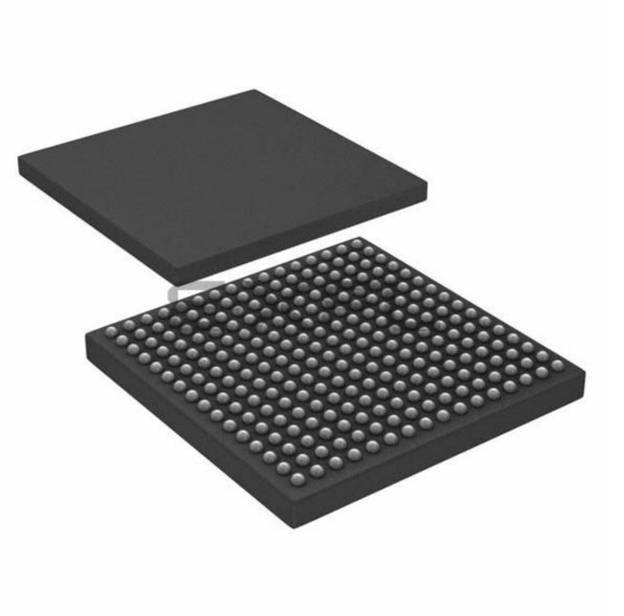
Microchip Technology - A3P1000-FGG256I Datasheet



Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

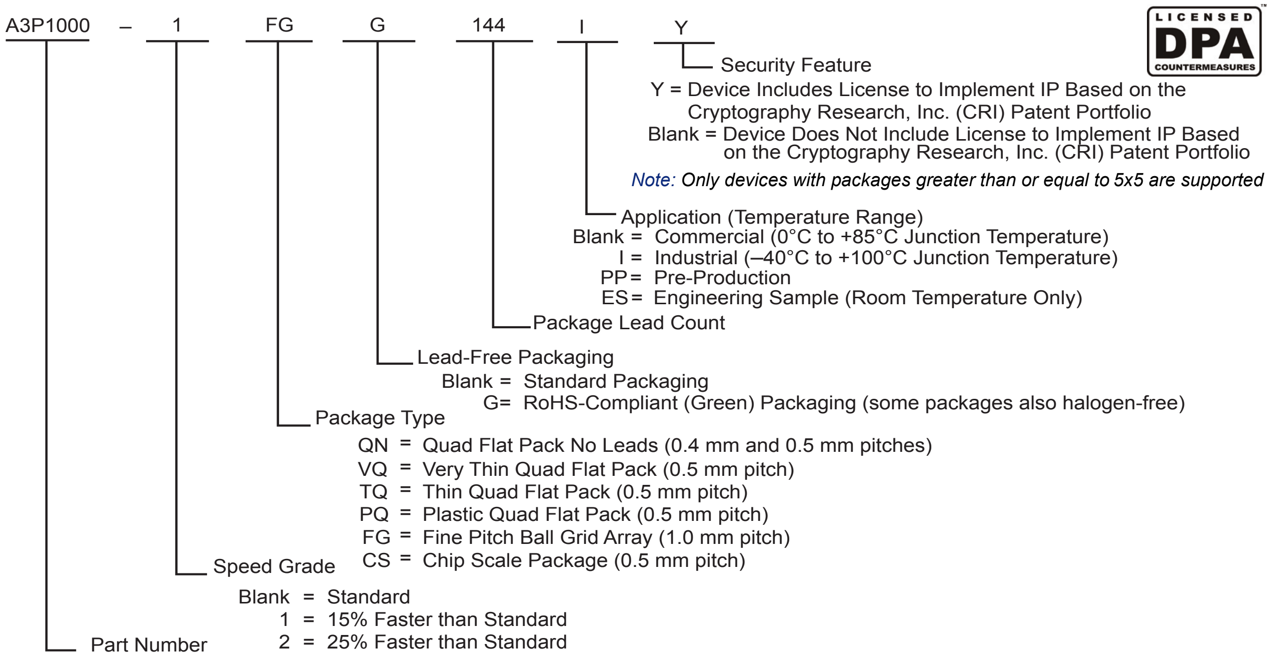
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p1000-fgg256i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

ProASIC3 Ordering Information



A3P1000 – 1 FG G 144 I Y

Security Feature

Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Blank = Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio

Note: *Only devices with packages greater than or equal to 5x5 are supported*

Application (Temperature Range)

Blank = Commercial (0°C to +85°C Junction Temperature)
I = Industrial (–40°C to +100°C Junction Temperature)
PP = Pre-Production
ES = Engineering Sample (Room Temperature Only)

Package Lead Count

Lead-Free Packaging

Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging (some packages also halogen-free)

Package Type

QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitches)
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
TQ = Thin Quad Flat Pack (0.5 mm pitch)
PQ = Plastic Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
CS = Chip Scale Package (0.5 mm pitch)

Speed Grade

Blank = Standard
1 = 15% Faster than Standard
2 = 25% Faster than Standard

Part Number

ProASIC3 Devices

A3P015 = 15,000 System Gates (A3P015 is not recommended for new designs.)
A3P030 = 30,000 System Gates
A3P060 = 60,000 System Gates
A3P125 = 125,000 System Gates
A3P250 = 250,000 System Gates
A3P400 = 400,000 System Gates
A3P600 = 600,000 System Gates
A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1

M1A3P250 = 250,000 System Gates
M1A3P400 = 400,000 System Gates
M1A3P600 = 600,000 System Gates
M1A3P1000 = 1,000,000 System Gates

ProASIC3 Device Status

ProASIC3 Devices	Status	Cortex-M1 Devices	Status
A3P015	Not recommended for new designs.		
A3P030	Production		
A3P060	Production		
A3P125	Production		
A3P250	Production	M1A3P250	Production
A3P400	Production	M1A3P400	Production
A3P600	Production	M1A3P600	Production
A3P1000	Production	M1A3P1000	Production

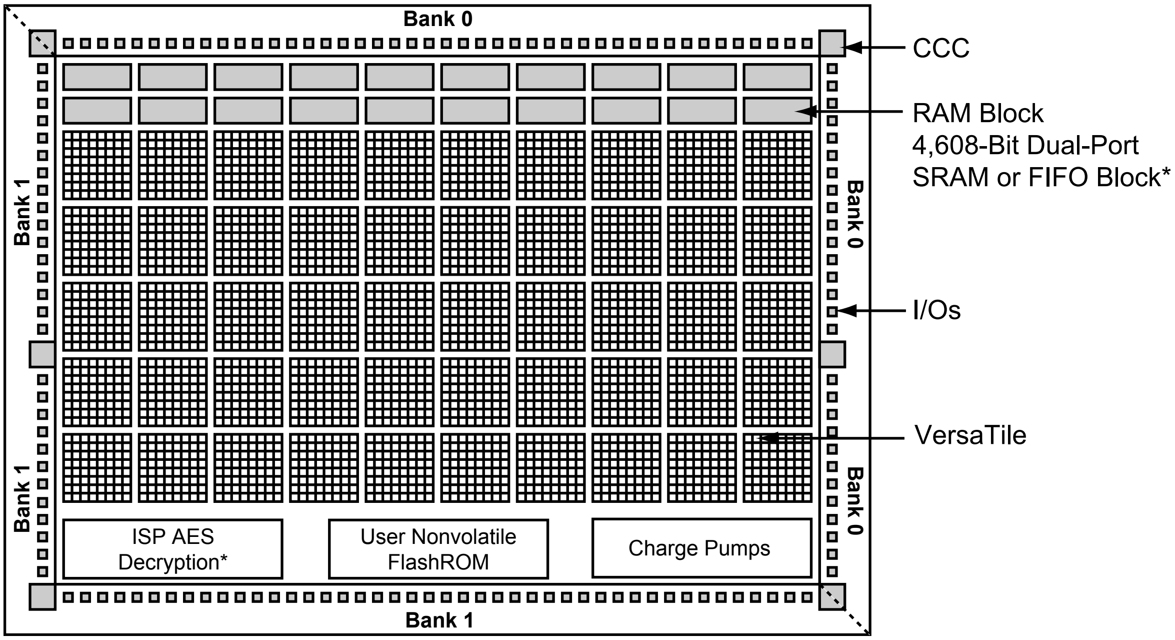
Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure



*Note: *Not supported by A3P015 and A3P030 devices*

Figure 1-1 • **ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)**

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† The A3P015 and A3P030 do not support PLL or SRAM.

Table 2-2 • Recommended Operating Conditions [1]

Symbol	Parameters [1]		Commercial	Industrial	Units
T_J	Junction temperature		0 to 85[2]	-40 to 100[2]	°C
VCC[3]	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [4]	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV [5]	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V wide range DC supply voltage [6]		2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero® System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.*
4. *VPUMP can be left floating during operation (not programming mode).*
5. *VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

Table 2-11 • **Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1]**
Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-12 • **Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1]**
Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. P_{DC3} *is the static power (where applicable) measured on VMV.*
3. P_{AC10} *is the total dynamic power measured on VCC and VMV.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ\text{-}CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE\text{-}CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-17 on page 2-14.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} *F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-16 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-17 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

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[1] The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.

Table 2-39 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min V**	**Max V**	**Min V**	**Max V**	**Max V**	**Min V**	**mA**	**mA**	**Max mA[3]**	**Max mA[3]**	**μA[4]**	**μA[4]**
2 mA	–0.3	0.8	2	3.6	0.4	2.4	2	2	25	27	10	10
4 mA	–0.3	0.8	2	3.6	0.4	2.4	4	4	25	27	10	10
6 mA	–0.3	0.8	2	3.6	0.4	2.4	6	6	51	54	10	10
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	51	54	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *I_{IH} is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at 100°C junction temperature and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

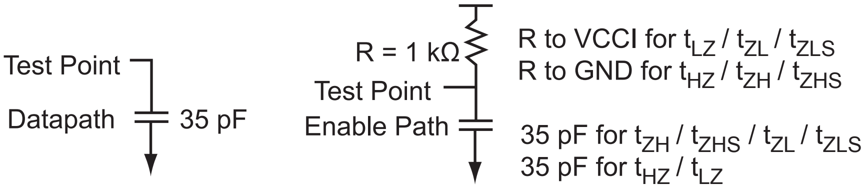


Figure 2-7 • AC Loading

Table 2-40 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-41 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
4 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	–1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	–2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	–1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	–2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-51 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks**

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.60	15.86	0.04	1.54	0.43	15.86	13.51	4.09	3.80	19.25	16.90	ns
		–1	0.51	13.49	0.04	1.31	0.36	13.49	11.49	3.48	3.23	16.38	14.38	ns
		–2	0.45	11.84	0.03	1.15	0.32	11.84	10.09	3.05	2.84	14.38	12.62	ns
100 µA	4 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 µA	6 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 µA	8 mA	Std.	0.60	8.63	0.04	1.54	0.43	8.63	7.39	4.96	5.28	12.02	10.79	ns
		–1	0.51	7.34	0.04	1.31	0.36	7.34	6.29	4.22	4.49	10.23	9.18	ns
		–2	0.45	6.44	0.03	1.15	0.32	6.44	5.52	3.70	3.94	8.98	8.06	ns
100 µA	16 mA	Std.	0.60	8.05	0.04	1.54	0.43	8.05	6.93	5.03	5.43	11.44	10.32	ns
		–1	0.51	6.85	0.04	1.31	0.36	6.85	5.90	4.28	4.62	9.74	8.78	ns
		–2	0.45	6.01	0.03	1.15	0.32	6.01	5.18	3.76	4.06	8.55	7.71	ns
100 µA	24 mA	Std.	0.60	7.50	0.04	1.54	0.43	7.50	6.90	5.13	6.00	10.89	10.29	ns
		–1	0.51	6.38	0.04	1.31	0.36	6.38	5.87	4.36	5.11	9.27	8.76	ns
		–2	0.45	5.60	0.03	1.15	0.32	5.60	5.15	3.83	4.48	8.13	7.69	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-81 **• 1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-82 **• 1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-90 • **LVDS Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Lower Current	0.65	0.91	1.16	mA
IOH [1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH [2,3]	Input High Leakage Current			10	µA
IIL [2,4]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN <VIL.*

Table 2-91 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

*Note: *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-92 • **LVDS**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.83	0.04	1.60	ns
–1	0.56	1.56	0.04	1.36	ns
–2	0.49	1.37	0.03	1.20	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

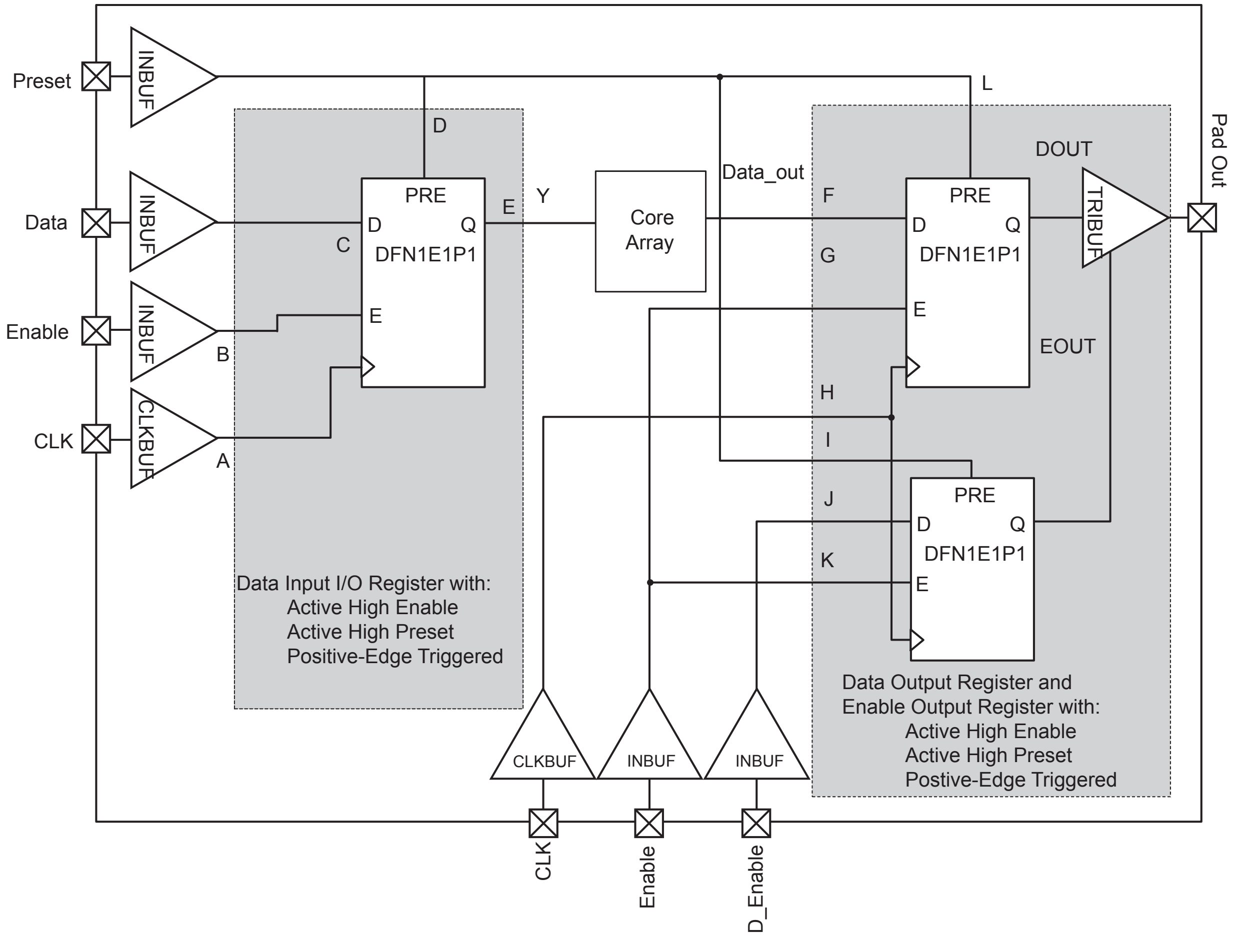


Figure 2-15 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

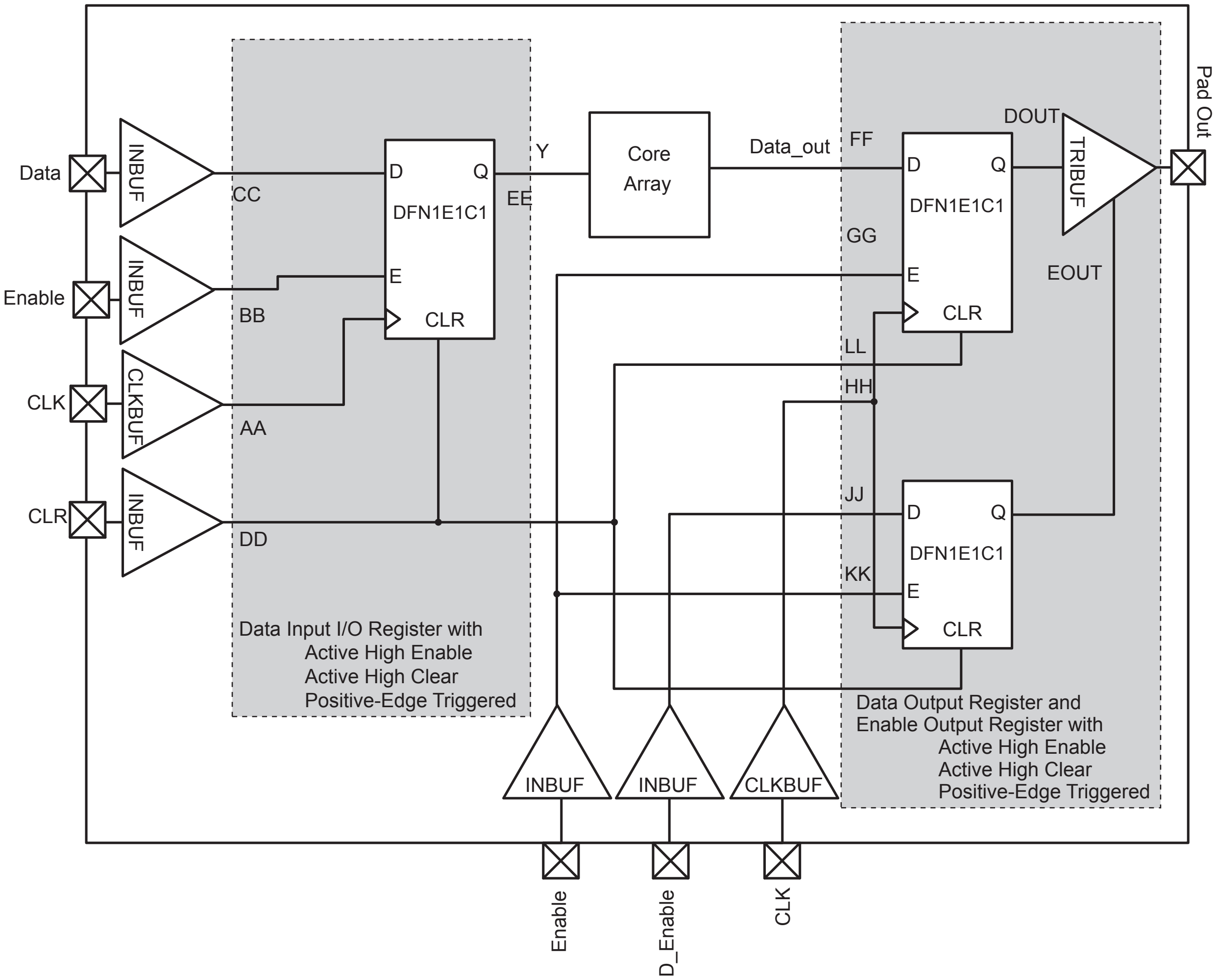


Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Timing Characteristics

Table 2-107 **• A3P015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.66	0.81	0.75	0.92	0.88	1.08	ns
t_{RCKH}	Input High Delay for Global Clock	0.67	0.84	0.76	0.96	0.89	1.13	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.25	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-108 **• A3P030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.67	0.81	0.76	0.92	0.89	1.09	ns
t_{RCKH}	Input High Delay for Global Clock	0.68	0.85	0.77	0.97	0.91	1.14	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.24	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

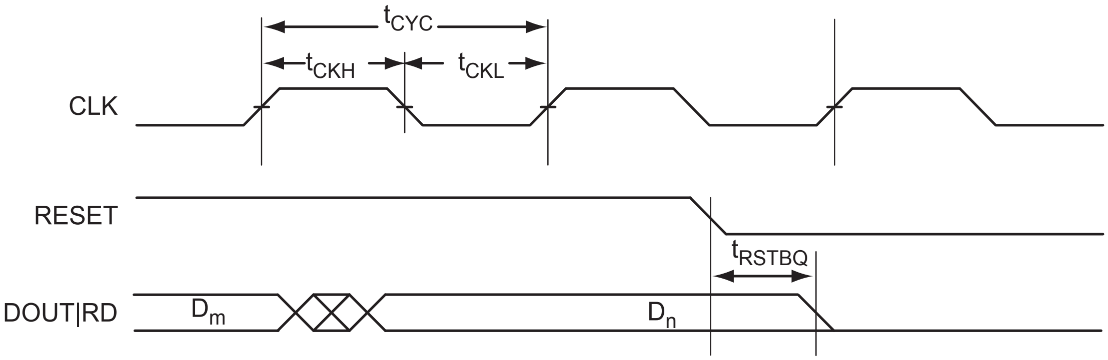
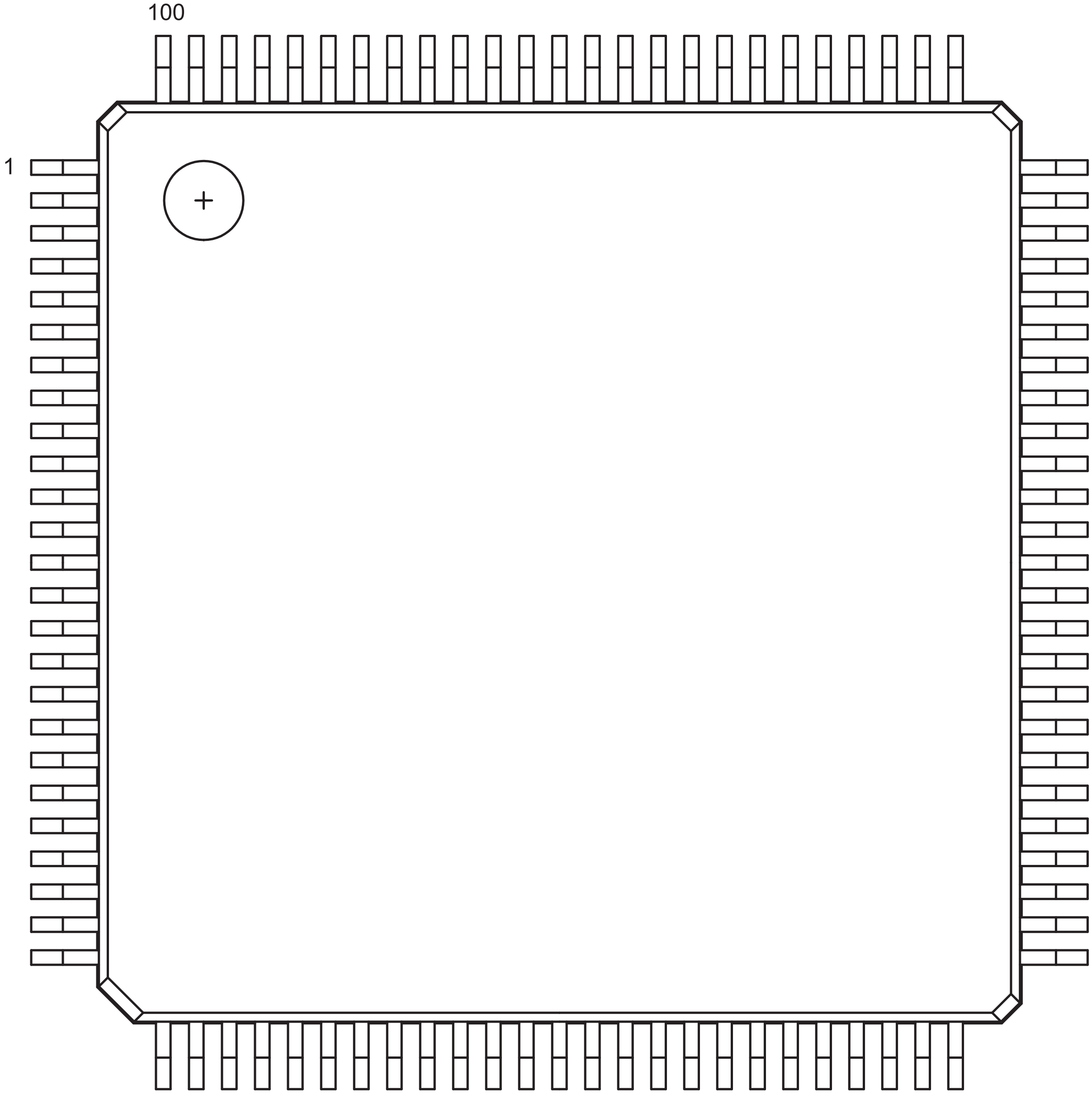


***Figure 2-35* • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

CS121	
Pin Number	**A3P060 Function**
A1	GNDQ
A2	IO01RSB0
A3	GAA1/IO03RSB0
A4	GAC1/IO07RSB0
A5	IO15RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	GBB1/IO22RSB0
A9	GBA1/IO24RSB0
A10	GNDQ
A11	VMV0
B1	GAA2/IO95RSB1
B2	IO00RSB0
B3	GAA0/IO02RSB0
B4	GAC0/IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO16RSB0
B8	GBC1/IO20RSB0
B9	GBB0/IO21RSB0
B10	GBB2/IO27RSB0
B11	GBA2/IO25RSB0
C1	IO89RSB1
C2	GAC2/IO91RSB1
C3	GAB1/IO05RSB0
C4	GAB0/IO04RSB0
C5	IO09RSB0
C6	IO14RSB0
C7	GBA0/IO23RSB0
C8	GBC0/IO19RSB0
C9	IO26RSB0
C10	IO28RSB0
C11	GBC2/IO29RSB0
D1	IO88RSB1
D2	IO90RSB1
D3	GAB2/IO93RSB1
D4	IO10RSB0
D5	IO11RSB0
D6	IO18RSB0
D7	IO32RSB0
D8	IO31RSB0
D9	GCA2/IO41RSB0
D10	IO30RSB0
D11	IO33RSB0
E1	IO87RSB1
E2	GFC0/IO85RSB1
E3	IO92RSB1
E4	IO94RSB1
E5	VCC
E6	VCCIB0
E7	GND
E8	GCC0/IO36RSB0
E9	IO34RSB0
E10	GCB1/IO37RSB0
E11	GCC1/IO35RSB0
F1	VCOMPLF
F2	GFB0/IO83RSB1
F3	GFA0/IO82RSB1
F4	GFC1/IO86RSB1
F5	VCCIB1
F6	VCC
F7	VCCIB0
F8	GCB2/IO42RSB0
F9	GCC2/IO43RSB0
F10	GCB0/IO38RSB0
F11	GCA1/IO39RSB0
G1	VCCPLF
G2	GFB2/IO79RSB1
G3	GFA1/IO81RSB1
G4	GFB1/IO84RSB1
G5	GND
G6	VCCIB1
G7	VCC
G8	GDC0/IO46RSB0
G9	GDA1/IO49RSB0
G10	GDB0/IO48RSB0
G11	GCA0/IO40RSB0
H1	IO75RSB1
H2	IO76RSB1
H3	GFC2/IO78RSB1
H4	GFA2/IO80RSB1
H5	IO77RSB1
H6	GEC2/IO66RSB1
H7	IO54RSB1
H8	GDC2/IO53RSB1
H9	VJTAG
H10	TRST
H11	IO44RSB0
J1	GEC1/IO74RSB1
J2	GEC0/IO73RSB1
J3	GEB1/IO72RSB1
J4	GEA0/IO69RSB1
J5	GEB2/IO67RSB1
J6	IO62RSB1
J7	GDA2/IO51RSB1
J8	GDB2/IO52RSB1
J9	TDI
J10	TDO
J11	GDC1/IO45RSB0
K1	GEB0/IO71RSB1
K2	GEA1/IO70RSB1
K3	GEA2/IO68RSB1
K4	IO64RSB1
K5	IO60RSB1
K6	IO59RSB1
K7	IO56RSB1
K8	TCK
K9	TMS

VQ100 – Top View



Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

PQ208	
Pin Number	**A3P600 Function**
1	GND
2	GAA2/IO174PDB3
3	IO174NDB3
4	GAB2/IO173PDB3
5	IO173NDB3
6	GAC2/IO172PDB3
7	IO172NDB3
8	IO171PDB3
9	IO171NDB3
10	IO170PDB3
11	IO170NDB3
12	IO169PDB3
13	IO169NDB3
14	IO168PDB3
15	IO168NDB3
16	VCC
17	GND
18	VCCIB3
19	IO166PDB3
20	IO166NDB3
21	GFC1/IO164PDB3
22	GFC0/IO164NDB3
23	GFB1/IO163PDB3
24	GFB0/IO163NDB3
25	VCOMPLF
26	GFA0/IO162NPB3
27	VCCPLF
28	GFA1/IO162PPB3
29	GND
30	GFA2/IO161PDB3
31	IO161NDB3
32	GFB2/IO160PDB3
33	IO160NDB3
34	GFC2/IO159PDB3
35	IO159NDB3
36	VCC
37	IO152PDB3
38	IO152NDB3
39	IO150PSB3
40	VCCIB3
41	GND
42	IO147PDB3
43	IO147NDB3
44	GEC1/IO146PDB3
45	GEC0/IO146NDB3
46	GEB1/IO145PDB3
47	GEB0/IO145NDB3
48	GEA1/IO144PDB3
49	GEA0/IO144NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO143RSB2
55	GEB2/IO142RSB2
56	GEC2/IO141RSB2
57	IO140RSB2
58	IO139RSB2
59	IO138RSB2
60	IO137RSB2
61	IO136RSB2
62	VCCIB2
63	IO135RSB2
64	IO133RSB2
65	GND
66	IO131RSB2
67	IO129RSB2
68	IO127RSB2
69	IO125RSB2
70	IO123RSB2
71	VCC
72	VCCIB2
73	IO120RSB2
74	IO119RSB2
75	IO118RSB2
76	IO117RSB2
77	IO116RSB2
78	IO115RSB2
79	IO114RSB2
80	IO112RSB2
81	GND
82	IO111RSB2
83	IO110RSB2
84	IO109RSB2
85	IO108RSB2
86	IO107RSB2
87	IO106RSB2
88	VCC
89	VCCIB2
90	IO104RSB2
91	IO102RSB2
92	IO100RSB2
93	IO98RSB2
94	IO96RSB2
95	IO92RSB2
96	GDC2/IO91RSB2
97	GND
98	GDB2/IO90RSB2
99	GDA2/IO89RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG256	
Pin Number	**A3P250 Function**
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

FG256	
Pin Number	**A3P250 Function**
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

FG256	
Pin Number	A3P400 Function
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2

FG256	
Pin Number	**A3P600 Function**
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND