# Microchip Technology - A3P125-1FG144 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 36864 |
| Number of I/O | 97 |
| Number of Gates | 125000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p125-1fg144 |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

| ProASIC3 Devices | A3P015[1] | A3P030 | A3P060 | A3P125 | A3P250 | A3P400 | A3P600 | A3P1000 |
|---|---|---|---|---|---|---|---|---|
| Cortex-M1 Devices [2] |  |  |  |  | M1A3P250 | M1A3P400 | M1A3P600 | M1A3P1000 |
| **Package Pins** |  |  |  |  |  |  |  |  |
| QFN | QN68 | QN48, QN68, QN132[7] | QN132[7] | QN132[7] | QN132[7] |  |  |  |
| CS |  |  | CS121 |  |  |  |  |  |
| VQFP |  | VQ100 | VQ100 | VQ100 | VQ100 |  |  |  |
| TQFP |  |  | TQ144 | TQ144 |  |  |  |  |
| PQFP |  |  |  | PQ208 | PQ208 | PQ208 | PQ208 | PQ208 |
| FBGA |  |  | FG144 | FG144 | FG144/256 [5] | FG144/256/484 | FG144/256/484 | FG144/256/484 |

*Notes:*

1. *A3P015 is not recommended for new designs.*
2. *Refer to the Cortex-M1 product brief for more information.*
3. *AES is not available for Cortex-M1 ProASIC3 devices.*
4. *Six chip (main) and three quadrant global networks are available for A3P060 and above.*
5. *The M1A3P250 device does not support this package.*
6. *For higher densities and support of additional features, refer to the ProASIC3E Flash Family FPGAs datasheet.*
7. *Package not available.*

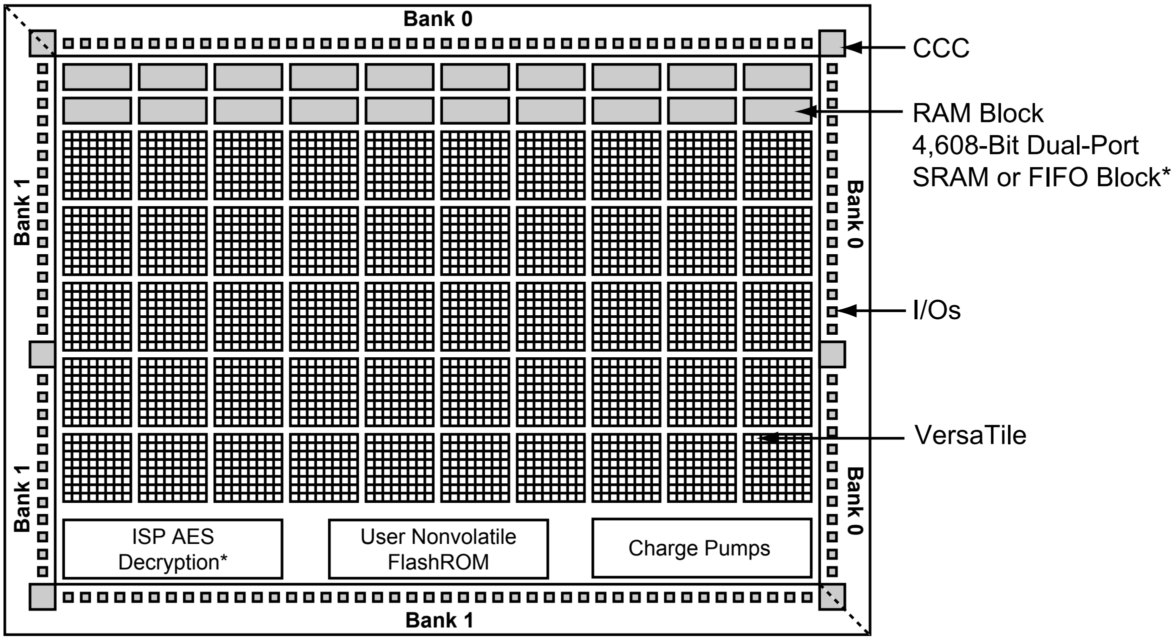
## Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure



*Note:* **Not supported by A3P015 and A3P030 devices*

***Figure 1-1 •*** **ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)**

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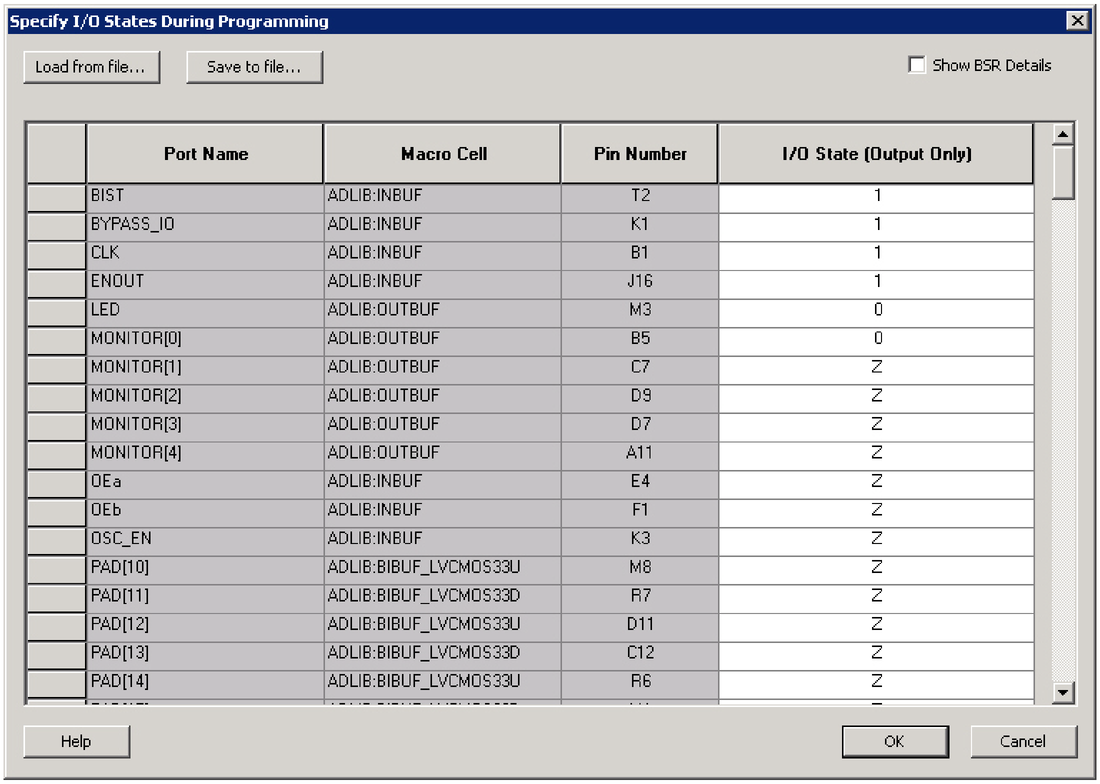
† *The A3P015 and A3P030 do not support PLL or SRAM.*

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tristate: I/O is tristated



| | Port Name | Macro Cell | Pin Number | I/O State (Output Only) |
|---|---|---|---|---|
| | BIST | ADLIB:INBUF | T2 | 1 |
| | BYPASS_IO | ADLIB:INBUF | K1 | 1 |
| | CLK | ADLIB:INBUF | B1 | 1 |
| | ENOUT | ADLIB:INBUF | J16 | 1 |
| | LED | ADLIB:OUTBUF | M3 | 0 |
| | MONITOR[0] | ADLIB:OUTBUF | B5 | 0 |
| | MONITOR[1] | ADLIB:OUTBUF | C7 | Z |
| | MONITOR[2] | ADLIB:OUTBUF | D9 | Z |
| | MONITOR[3] | ADLIB:OUTBUF | D7 | Z |
| | MONITOR[4] | ADLIB:OUTBUF | A11 | Z |
| | OEa | ADLIB:INBUF | E4 | Z |
| | OEb | ADLIB:INBUF | F1 | Z |
| | OSC_EN | ADLIB:INBUF | K3 | Z |
| | PAD[10] | ADLIB:BIBUF_LVCMOS33U | M8 | Z |
| | PAD[11] | ADLIB:BIBUF_LVCMOS33D | R7 | Z |
| | PAD[12] | ADLIB:BIBUF_LVCMOS33U | D11 | Z |
| | PAD[13] | ADLIB:BIBUF_LVCMOS33D | C12 | Z |
| | PAD[14] | ADLIB:BIBUF_LVCMOS33U | R6 | Z |

***Figure 1-4 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

## I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges.

In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

**VCCI Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

**VCC Trip Point:**
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

### *PLL Behavior at Brownout Condition*

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

### *Internal Power-Up Activation Sequence*

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

## Thermal Characteristics

### *Introduction*

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

$T_J$ = Junction Temperature = $\Delta T + T_A$

where:

$T_A$ = Ambient Temperature

$\Delta T$ = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

$\theta_{ja}$ = Junction-to-ambient of the package. $\theta_{ja}$ numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

*Table 2-15 •* **Different Components Contributing to the Static Power Consumption in ProASIC3 Devices**

| Parameter | Definition | Device Specific Static Power (mW) | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | **A3P1000** | **A3P600** | **A3P400** | **A3P250** | **A3P125** | **A3P060** | **A3P030** | **A3P015** |
| PDC1 | Array static power in Active mode | See Table 2-7 on page 2-7. | | | | | | | |
| PDC2 | I/O input pin static power (standard-dependent) | See Table 2-8 on page 2-7 through Table 2-10 on page 2-8. | | | | | | | |
| PDC3 | I/O output pin static power (standard-dependent) | See Table 2-11 on page 2-9 through Table 2-13 on page 2-10. | | | | | | | |
| PDC4 | Static PLL contribution | 2.55 mW | | | | | | | |
| PDC5 | Bank quiescent power (VCCI-dependent) | See Table 2-7 on page 2-7. | | | | | | | |

Note: **For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi Power spreadsheet calculator or SmartPower tool in Libero SoC software.*

## Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-17 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

### *Methodology*

#### *Total Power Consumption—$P_{TOTAL}$*

$P_{TOTAL} = P_{STAT} + P_{DYN}$

$P_{STAT}$ is the total static power consumption.

$P_{DYN}$ is the total dynamic power consumption.

#### *Total Static Power Consumption—$P_{STAT}$*

$P_{STAT} = P_{DC1} + N_{INPUTS}{}^{*}\ P_{DC2} + N_{OUTPUTS}{}^{*}\ P_{DC3}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

#### *Total Dynamic Power Consumption—$P_{DYN}$*

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

#### *Global Clock Contribution—$P_{CLOCK}$*

$P_{CLOCK} = (P_{AC1} + N_{SPINE}{}^{*}P_{AC2} + N_{ROW}{}^{*}P_{AC3} + N_{S\text{-}CELL}{}^{*}\ P_{AC4})\ {}^{*}\ F_{CLK}$

$N_{SPINE}$ is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

$N_{ROW}$ is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

*Table 2-42 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-45* • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | –2 | 0.49 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-46* • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 4 mA | Std. | 0.66 | 9.46 | 0.04 | 1.00 | 0.43 | 9.64 | 8.54 | 2.07 | 2.04 | ns |
| | –1 | 0.56 | 8.05 | 0.04 | 0.85 | 0.36 | 8.20 | 7.27 | 1.76 | 1.73 | ns |
| | –2 | 0.49 | 7.07 | 0.03 | 0.75 | 0.32 | 7.20 | 6.38 | 1.55 | 1.52 | ns |
| 6 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |
| 8 mA | Std. | 0.66 | 6.57 | 0.04 | 1.00 | 0.43 | 6.69 | 5.98 | 2.40 | 2.57 | ns |
| | –1 | 0.56 | 5.59 | 0.04 | 0.85 | 0.36 | 5.69 | 5.09 | 2.04 | 2.19 | ns |
| | –2 | 0.49 | 4.91 | 0.03 | 0.75 | 0.32 | 5.00 | 4.47 | 1.79 | 1.92 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-55 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-81*** **• 1.5 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 12.78 | 0.04 | 1.44 | 0.43 | 12.81 | 12.78 | 3.40 | 2.64 | 15.05 | 15.02 | ns |
| | –1 | 0.56 | 10.87 | 0.04 | 1.22 | 0.36 | 10.90 | 10.87 | 2.89 | 2.25 | 12.80 | 12.78 | ns |
| | –2 | 0.49 | 9.55 | 0.03 | 1.07 | 0.32 | 9.57 | 9.55 | 2.54 | 1.97 | 11.24 | 11.22 | ns |
| 4 mA | Std. | 0.66 | 10.01 | 0.04 | 1.44 | 0.43 | 10.19 | 9.55 | 3.75 | 3.27 | 12.43 | 11.78 | ns |
| | –1 | 0.56 | 8.51 | 0.04 | 1.22 | 0.36 | 8.67 | 8.12 | 3.19 | 2.78 | 10.57 | 10.02 | ns |
| | –2 | 0.49 | 7.47 | 0.03 | 1.07 | 0.32 | 7.61 | 7.13 | 2.80 | 2.44 | 9.28 | 8.80 | ns |
| 6 mA | Std. | 0.66 | 9.33 | 0.04 | 1.44 | 0.43 | 9.51 | 8.89 | 3.83 | 3.43 | 11.74 | 11.13 | ns |
| | –1 | 0.56 | 7.94 | 0.04 | 1.22 | 0.36 | 8.09 | 7.56 | 3.26 | 2.92 | 9.99 | 9.47 | ns |
| | –2 | 0.49 | 6.97 | 0.03 | 1.07 | 0.32 | 7.10 | 6.64 | 2.86 | 2.56 | 8.77 | 8.31 | ns |
| 8 mA | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | –1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | –2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |
| 12 mA | Std. | 0.66 | 8.91 | 0.04 | 1.44 | 0.43 | 9.07 | 8.89 | 3.95 | 4.05 | 11.31 | 11.13 | ns |
| | –1 | 0.56 | 7.58 | 0.04 | 1.22 | 0.36 | 7.72 | 7.57 | 3.36 | 3.44 | 9.62 | 9.47 | ns |
| | –2 | 0.49 | 6.65 | 0.03 | 1.07 | 0.32 | 6.78 | 6.64 | 2.95 | 3.02 | 8.45 | 8.31 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-82*** **• 1.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 7.83 | 0.04 | 1.42 | 0.43 | 6.42 | 7.83 | 2.71 | 2.55 | 8.65 | 10.07 | ns |
| | –1 | 0.56 | 6.66 | 0.04 | 1.21 | 0.36 | 5.46 | 6.66 | 2.31 | 2.17 | 7.36 | 8.56 | ns |
| | –2 | 0.49 | 5.85 | 0.03 | 1.06 | 0.32 | 4.79 | 5.85 | 2.02 | 1.90 | 6.46 | 7.52 | ns |
| 4 mA | Std. | 0.66 | 4.84 | 0.04 | 1.42 | 0.43 | 4.49 | 4.84 | 3.03 | 3.13 | 6.72 | 7.08 | ns |
| | –1 | 0.56 | 4.12 | 0.04 | 1.21 | 0.36 | 3.82 | 4.12 | 2.58 | 2.66 | 5.72 | 6.02 | ns |
| | –2 | 0.49 | 3.61 | 0.03 | 1.06 | 0.32 | 3.35 | 3.61 | 2.26 | 2.34 | 5.02 | 5.28 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### Timing Characteristics

***Table 2-88 •*** **3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | ns |
| –1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | ns |
| –2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-89 •*** **3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.31 | 0.04 | 0.85 | 0.43 | 2.35 | 1.70 | 2.79 | 3.22 | 4.59 | 3.94 | ns |
| –1 | 0.56 | 1.96 | 0.04 | 0.72 | 0.36 | 2.00 | 1.45 | 2.37 | 2.74 | 3.90 | 3.35 | ns |
| –2 | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Differential I/O Characteristics

### *Physical Implementation*

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### *LVDS*

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

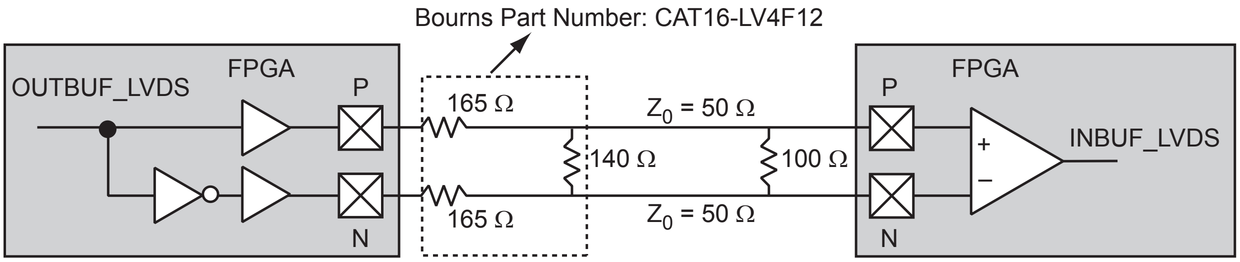


***Figure 2-12 •*** **LVDS Circuit Diagram and Board-Level Implementation**

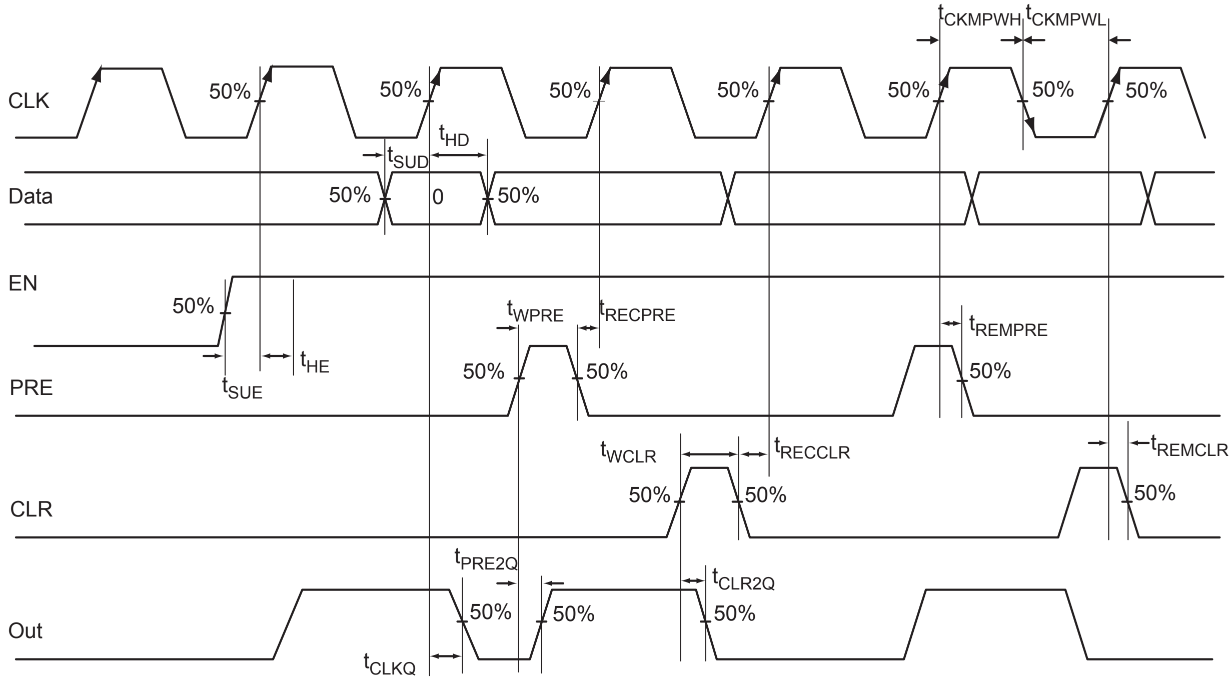


***Figure 2-27*** **• Timing Model and Waveforms**

### *Timing Characteristics*

***Table 2-106*** **• Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-121* • A3P250 FIFO 1k×4**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 4.05 | 4.61 | 5.42 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
|  | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

| QN132 | |
|---|---|
| **Pin Number** | **A3P125 Function** |
| C17 | IO83RSB1 |
| C18 | VCCIB1 |
| C19 | TCK |
| C20 | VMV1 |
| C21 | VPUMP |
| C22 | VJTAG |
| C23 | VCCIB0 |
| C24 | NC |
| C25 | NC |
| C26 | GCA1/IO55RSB0 |
| C27 | GCC0/IO52RSB0 |
| C28 | VCCIB0 |
| C29 | IO42RSB0 |
| C30 | GNDQ |
| C31 | GBA1/IO40RSB0 |
| C32 | GBB0/IO37RSB0 |
| C33 | VCC |
| C34 | IO24RSB0 |
| C35 | IO19RSB0 |
| C36 | IO16RSB0 |
| C37 | IO10RSB0 |
| C38 | VCCIB0 |
| C39 | GAB1/IO03RSB0 |
| C40 | VMV0 |
| D1 | GND |
| D2 | GND |
| D3 | GND |
| D4 | GND |

**CS121**

| Pin Number | A3P060 Function |
|---|---|
| A1 | GNDQ |
| A2 | IO01RSB0 |
| A3 | GAA1/IO03RSB0 |
| A4 | GAC1/IO07RSB0 |
| A5 | IO15RSB0 |
| A6 | IO13RSB0 |
| A7 | IO17RSB0 |
| A8 | GBB1/IO22RSB0 |
| A9 | GBA1/IO24RSB0 |
| A10 | GNDQ |
| A11 | VMV0 |
| B1 | GAA2/IO95RSB1 |
| B2 | IO00RSB0 |
| B3 | GAA0/IO02RSB0 |
| B4 | GAC0/IO06RSB0 |
| B5 | IO08RSB0 |
| B6 | IO12RSB0 |
| B7 | IO16RSB0 |
| B8 | GBC1/IO20RSB0 |
| B9 | GBB0/IO21RSB0 |
| B10 | GBB2/IO27RSB0 |
| B11 | GBA2/IO25RSB0 |
| C1 | IO89RSB1 |
| C2 | GAC2/IO91RSB1 |
| C3 | GAB1/IO05RSB0 |
| C4 | GAB0/IO04RSB0 |
| C5 | IO09RSB0 |
| C6 | IO14RSB0 |
| C7 | GBA0/IO23RSB0 |
| C8 | GBC0/IO19RSB0 |
| C9 | IO26RSB0 |
| C10 | IO28RSB0 |
| C11 | GBC2/IO29RSB0 |
| D1 | IO88RSB1 |
| D2 | IO90RSB1 |
| D3 | GAB2/IO93RSB1 |
| D4 | IO10RSB0 |
| D5 | IO11RSB0 |
| D6 | IO18RSB0 |
| D7 | IO32RSB0 |
| D8 | IO31RSB0 |
| D9 | GCA2/IO41RSB0 |
| D10 | IO30RSB0 |
| D11 | IO33RSB0 |
| E1 | IO87RSB1 |
| E2 | GFC0/IO85RSB1 |
| E3 | IO92RSB1 |
| E4 | IO94RSB1 |
| E5 | VCC |
| E6 | VCCIB0 |
| E7 | GND |
| E8 | GCC0/IO36RSB0 |
| E9 | IO34RSB0 |
| E10 | GCB1/IO37RSB0 |
| E11 | GCC1/IO35RSB0 |
| F1 | VCOMPLF |
| F2 | GFB0/IO83RSB1 |
| F3 | GFA0/IO82RSB1 |
| F4 | GFC1/IO86RSB1 |
| F5 | VCCIB1 |
| F6 | VCC |
| F7 | VCCIB0 |
| F8 | GCB2/IO42RSB0 |
| F9 | GCC2/IO43RSB0 |
| F10 | GCB0/IO38RSB0 |
| F11 | GCA1/IO39RSB0 |
| G1 | VCCPLF |
| G2 | GFB2/IO79RSB1 |
| G3 | GFA1/IO81RSB1 |
| G4 | GFB1/IO84RSB1 |
| G5 | GND |
| G6 | VCCIB1 |
| G7 | VCC |
| G8 | GDC0/IO46RSB0 |
| G9 | GDA1/IO49RSB0 |
| G10 | GDB0/IO48RSB0 |
| G11 | GCA0/IO40RSB0 |
| H1 | IO75RSB1 |
| H2 | IO76RSB1 |
| H3 | GFC2/IO78RSB1 |
| H4 | GFA2/IO80RSB1 |
| H5 | IO77RSB1 |
| H6 | GEC2/IO66RSB1 |
| H7 | IO54RSB1 |
| H8 | GDC2/IO53RSB1 |
| H9 | VJTAG |
| H10 | TRST |
| H11 | IO44RSB0 |
| J1 | GEC1/IO74RSB1 |
| J2 | GEC0/IO73RSB1 |
| J3 | GEB1/IO72RSB1 |
| J4 | GEA0/IO69RSB1 |
| J5 | GEB2/IO67RSB1 |
| J6 | IO62RSB1 |
| J7 | GDA2/IO51RSB1 |
| J8 | GDB2/IO52RSB1 |
| J9 | TDI |
| J10 | TDO |
| J11 | GDC1/IO45RSB0 |
| K1 | GEB0/IO71RSB1 |
| K2 | GEA1/IO70RSB1 |
| K3 | GEA2/IO68RSB1 |
| K4 | IO64RSB1 |
| K5 | IO60RSB1 |
| K6 | IO59RSB1 |
| K7 | IO56RSB1 |
| K8 | TCK |
| K9 | TMS |

| TQ144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| 1 | GAA2/IO51RSB1 |
| 2 | IO52RSB1 |
| 3 | GAB2/IO53RSB1 |
| 4 | IO95RSB1 |
| 5 | GAC2/IO94RSB1 |
| 6 | IO93RSB1 |
| 7 | IO92RSB1 |
| 8 | IO91RSB1 |
| 9 | VCC |
| 10 | GND |
| 11 | VCCIB1 |
| 12 | IO90RSB1 |
| 13 | GFC1/IO89RSB1 |
| 14 | GFC0/IO88RSB1 |
| 15 | GFB1/IO87RSB1 |
| 16 | GFB0/IO86RSB1 |
| 17 | VCOMPLF |
| 18 | GFA0/IO85RSB1 |
| 19 | VCCPLF |
| 20 | GFA1/IO84RSB1 |
| 21 | GFA2/IO83RSB1 |
| 22 | GFB2/IO82RSB1 |
| 23 | GFC2/IO81RSB1 |
| 24 | IO80RSB1 |
| 25 | IO79RSB1 |
| 26 | IO78RSB1 |
| 27 | GND |
| 28 | VCCIB1 |
| 29 | GEC1/IO77RSB1 |
| 30 | GEC0/IO76RSB1 |
| 31 | GEB1/IO75RSB1 |
| 32 | GEB0/IO74RSB1 |
| 33 | GEA1/IO73RSB1 |
| 34 | GEA0/IO72RSB1 |
| 35 | VMV1 |
| 36 | GNDQ |
| 37 | NC |
| 38 | GEA2/IO71RSB1 |
| 39 | GEB2/IO70RSB1 |
| 40 | GEC2/IO69RSB1 |
| 41 | IO68RSB1 |
| 42 | IO67RSB1 |
| 43 | IO66RSB1 |
| 44 | IO65RSB1 |
| 45 | VCC |
| 46 | GND |
| 47 | VCCIB1 |
| 48 | NC |
| 49 | IO64RSB1 |
| 50 | NC |
| 51 | IO63RSB1 |
| 52 | NC |
| 53 | IO62RSB1 |
| 54 | NC |
| 55 | IO61RSB1 |
| 56 | NC |
| 57 | NC |
| 58 | IO60RSB1 |
| 59 | IO59RSB1 |
| 60 | IO58RSB1 |
| 61 | IO57RSB1 |
| 62 | NC |
| 63 | GND |
| 64 | NC |
| 65 | GDC2/IO56RSB1 |
| 66 | GDB2/IO55RSB1 |
| 67 | GDA2/IO54RSB1 |
| 68 | GNDQ |
| 69 | TCK |
| 70 | TDI |
| 71 | TMS |
| 72 | VMV1 |
| 73 | VPUMP |
| 74 | NC |
| 75 | TDO |
| 76 | TRST |
| 77 | VJTAG |
| 78 | GDA0/IO50RSB0 |
| 79 | GDB0/IO48RSB0 |
| 80 | GDB1/IO47RSB0 |
| 81 | VCCIB0 |
| 82 | GND |
| 83 | IO44RSB0 |
| 84 | GCC2/IO43RSB0 |
| 85 | GCB2/IO42RSB0 |
| 86 | GCA2/IO41RSB0 |
| 87 | GCA0/IO40RSB0 |
| 88 | GCA1/IO39RSB0 |
| 89 | GCB0/IO38RSB0 |
| 90 | GCB1/IO37RSB0 |
| 91 | GCC0/IO36RSB0 |
| 92 | GCC1/IO35RSB0 |
| 93 | IO34RSB0 |
| 94 | IO33RSB0 |
| 95 | NC |
| 96 | NC |
| 97 | NC |
| 98 | VCCIB0 |
| 99 | GND |
| 100 | VCC |
| 101 | IO30RSB0 |
| 102 | GBC2/IO29RSB0 |
| 103 | IO28RSB0 |
| 104 | GBB2/IO27RSB0 |
| 105 | IO26RSB0 |
| 106 | GBA2/IO25RSB0 |
| 107 | VMV0 |
| 108 | GNDQ |

| FG484 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO154VDB3 |
| F5 | IO155VDB3 |
| F6 | IO11RSB0 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO45RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO48RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | NC |
| G2 | NC |
| G3 | NC |
| G4 | IO151VDB3 |
| G5 | IO151UDB3 |
| G6 | GAC2/IO153UDB3 |
| G7 | IO06RSB0 |
| G8 | GNDQ |
| G9 | IO10RSB0 |
| G10 | IO19RSB0 |
| G11 | IO26RSB0 |
| G12 | IO30RSB0 |
| G13 | IO40RSB0 |
| G14 | IO46RSB0 |
| G15 | GNDQ |
| G16 | IO47RSB0 |
| G17 | GBB2/IO61PPB1 |
| G18 | IO53RSB0 |
| G19 | IO63NDB1 |
| G20 | NC |
| G21 | NC |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | VCC |
| H4 | IO150PDB3 |
| H5 | IO08RSB0 |
| H6 | IO153VDB3 |
| H7 | IO152VDB3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO25RSB0 |
| H12 | IO31RSB0 |
| H13 | VCCIB0 |
| H14 | VCCIB0 |
| H15 | VMV1 |
| H16 | GBC2/IO62PDB1 |
| H17 | IO65RSB1 |
| H18 | IO52RSB0 |
| H19 | IO66PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO150NDB3 |
| J5 | IO149NPB3 |
| J6 | IO09RSB0 |
| J7 | IO152UDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO62NDB1 |
| J17 | IO49RSB0 |
| J18 | IO64PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | NC |
| J22 | NC |
| K1 | NC |
| K2 | NC |
| K3 | NC |
| K4 | IO148NDB3 |
| K5 | IO148PDB3 |
| K6 | IO149PPB3 |
| K7 | GFC1/IO147PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB1 |
| K16 | GCC1/IO67PPB1 |
| K17 | IO64NPB1 |
| K18 | IO73PDB1 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| R17 | GDB1/IO112PPB1 |
| R18 | GDC1/IO111PDB1 |
| R19 | IO107NDB1 |
| R20 | VCC |
| R21 | IO104NDB1 |
| R22 | IO105PDB1 |
| T1 | IO198PDB3 |
| T2 | IO198NDB3 |
| T3 | NC |
| T4 | IO194PPB3 |
| T5 | IO192PPB3 |
| T6 | GEC1/IO190PPB3 |
| T7 | IO192NPB3 |
| T8 | GNDQ |
| T9 | GEA2/IO187RSB2 |
| T10 | IO161RSB2 |
| T11 | IO155RSB2 |
| T12 | IO141RSB2 |
| T13 | IO129RSB2 |
| T14 | IO124RSB2 |
| T15 | GNDQ |
| T16 | IO110PDB1 |
| T17 | VJTAG |
| T18 | GDC0/IO111NDB1 |
| T19 | GDA1/IO113PDB1 |
| T20 | NC |
| T21 | IO108PDB1 |
| T22 | IO105NDB1 |
| U1 | IO195PDB3 |
| U2 | IO195NDB3 |
| U3 | IO194NPB3 |
| U4 | GEB1/IO189PDB3 |
| U5 | GEB0/IO189NDB3 |
| U6 | VMV2 |
| U7 | IO179RSB2 |
| U8 | IO171RSB2 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| U9 | IO165RSB2 |
| U10 | IO159RSB2 |
| U11 | IO151RSB2 |
| U12 | IO137RSB2 |
| U13 | IO134RSB2 |
| U14 | IO128RSB2 |
| U15 | VMV1 |
| U16 | TCK |
| U17 | VPUMP |
| U18 | TRST |
| U19 | GDA0/IO113NDB1 |
| U20 | NC |
| U21 | IO108NDB1 |
| U22 | IO109PDB1 |
| V1 | NC |
| V2 | NC |
| V3 | GND |
| V4 | GEA1/IO188PDB3 |
| V5 | GEA0/IO188NDB3 |
| V6 | IO184RSB2 |
| V7 | GEC2/IO185RSB2 |
| V8 | IO168RSB2 |
| V9 | IO163RSB2 |
| V10 | IO157RSB2 |
| V11 | IO149RSB2 |
| V12 | IO143RSB2 |
| V13 | IO138RSB2 |
| V14 | IO131RSB2 |
| V15 | IO125RSB2 |
| V16 | GDB2/IO115RSB2 |
| V17 | TDI |
| V18 | GNDQ |
| V19 | TDO |
| V20 | GND |
| V21 | NC |
| V22 | IO109NDB1 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| W1 | NC |
| W2 | IO191PDB3 |
| W3 | NC |
| W4 | GND |
| W5 | IO183RSB2 |
| W6 | GEB2/IO186RSB2 |
| W7 | IO172RSB2 |
| W8 | IO170RSB2 |
| W9 | IO164RSB2 |
| W10 | IO158RSB2 |
| W11 | IO153RSB2 |
| W12 | IO142RSB2 |
| W13 | IO135RSB2 |
| W14 | IO130RSB2 |
| W15 | GDC2/IO116RSB2 |
| W16 | IO120RSB2 |
| W17 | GDA2/IO114RSB2 |
| W18 | TMS |
| W19 | GND |
| W20 | NC |
| W21 | NC |
| W22 | NC |
| Y1 | VCCIB3 |
| Y2 | IO191NDB3 |
| Y3 | NC |
| Y4 | IO182RSB2 |
| Y5 | GND |
| Y6 | IO177RSB2 |
| Y7 | IO174RSB2 |
| Y8 | VCC |
| Y9 | VCC |
| Y10 | IO154RSB2 |
| Y11 | IO148RSB2 |
| Y12 | IO140RSB2 |
| Y13 | NC |
| Y14 | VCC |

| Revision | Changes | Page |
|---|---|---|
| Revision 13 (January 2013) | The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104). | 1-IV |
| | Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C. | 2-2 |
| | The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569). | 2-90 |
| | Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284).<br>Live at Power-Up (LAPU) has been replaced with 'Instant On'. | NA |
| Revision 12 (September 2012) | The Security section was modified to clarify that Microsemi does not support read-back of programmed data. | 1-1 |
| | Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321). | 2-1<br>2-2 |
| | Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933). | 2-31 |
| | In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549). | 2-68 |
| | Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371). | 2-99 |
| | The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement. | 3-1 |

| Revision | Changes | Page |
|---|---|---|
| **Revision 2 (cont'd)** | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | III |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | IV |
| | In the General Description section the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68 – Bottom View" section is new. | 4-3 |
| **Revision 1 (Feb 2008)**<br>DC and Switching Characteristics v1.1 | In Table 2-2 • Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$. | 2-2 |
| | In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | In the "PLL Contribution—PPLL" section, the following was deleted:<br>FCLKIN is the input clock frequency. | 2-14 |
| | In Table 2-21 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$. | 2-21 |
| | In Table 2-115 • ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new. | 2-90 |
| | Table 2-125 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-108 |
| Packaging v1.1 | In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 4-19 |
| **Revision 0 (Jan 2008)** | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. | N/A |
| v2.2<br>(July 2007) | The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |
| v2.1<br>(May 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii |
| | Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |

| Revision | Changes | Page |
|---|---|---|
| Advance v0.6 (continued) | The "RESET" section was updated. | 2-25 |
| | The "WCLK and RCLK" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-25 |
| | The "RESET" section was updated. | 2-27 |
| | The "Introduction" of the "Advanced I/Os" section was updated. | 2-28 |
| | The "I/O Banks" section is new. This section explains the following types of I/Os:<br>Advanced<br>Standard+<br>Standard<br>Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above. | 2-29 |
| | PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards | 2-29 |
| | Table 2-13 • ProASIC3 I/O Features was updated. | 2-30 |
| | The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature. | 2-32 |
| | The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information. | 2-35 |
| | Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices. | 2-64 |
| | The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated. | 2-64 |
| | The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new. | 2-41 |
| | A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected). | 2-30 |
| | Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications | 2-45 |
| | Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device) | 2-83 |
| | Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated. | 2-84 |
| | Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated. | 2-84 |
| | The "x" was updated in the "User I/O Naming Convention" section. | 2-48 |
| | The "VCC Core Supply Voltage" pin description was updated. | 2-50 |
| | The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected. | 2-50 |
| | The "VJTAG JTAG Supply Voltage" pin description was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground. | 2-50 |
| | The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused. | 2-50 |
| | The "JTAG Pins" section was updated to include information on what happens when the pin is unused. | 2-51 |