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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	133
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-2pqq208

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹ mA	IOH ¹ mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTTL / 3.3 V LVC MOS	12 mA	12 mA	High	−0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVC MOS Wide Range ³	100 μ A	12 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVC MOS	12 mA	12 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVC MOS	8 mA	8 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8
1.5 V LVC MOS	4 mA	4 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	4	4
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. Currents are measured at 85°C junction temperature.
2. 3.3 V LVC MOS wide range is applicable to 100 μ A drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
3. All LVC MOS 3.3 V software macros support LVC MOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ²	Slew Rate	VIL		VIH		VOL	VOH	IOL ¹ mA	IOH ¹ mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	−0.3	0.8	2	3.6	0.4	2.4	8	8
3.3 V LVCMOS Wide Range ³	100 μ A	8 mA	High	−0.3	0.8	2	3.6	0.2	VCCI − 0.2	0.1	0.1
2.5 V LVCMOS	8 mA	8 mA	High	−0.3	0.7	1.7	2.7	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	4 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4
1.5 V LVCMOS	2 mA	2 mA	High	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2

Notes:

1. Currents are measured at 85°C junction temperature.
2. 3.3 V LVCMOS wide range is applicable to 100 μ A drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

Table 2-21 • Summary of Maximum and Minimum DC Input Levels
Applicable to Commercial and Industrial Conditions

DC I/O Standards	Commercial ¹		Industrial ²	
	IIL ³	IIH ⁴	IIL ³	IIH ⁴
	μ A	μ A	μ A	μ A
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
3.3 V LVCMOS Wide Range	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. Commercial range (0°C < T_A < 70°C)
2. Industrial range (−40°C < T_A < 85°C)
3. IIL is the input leakage current per I/O pin over recommended operation conditions where −0.3V < V_{IN} < V_{IL}.
4. IIH is the input leakage current per I/O pin over recommended operating conditions V_{IH} < V_{IN} < V_{CCI}. Input current is larger when operating outside recommended ranges.

Table 2-32 • I/O Short Currents IOSH/IOSL
Applicable to Advanced I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS Wide Range ²	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Notes:

1. $T_J = 100^\circ\text{C}$
2. Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-34 • I/O Short Currents IOSH/IOSL
Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range ²	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

1. $T_J = 100^\circ\text{C}$
2. Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C , the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.

Timing Characteristics

Table 2-50 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	4 mA	Std.	0.60	11.84	0.04	1.02	0.43	11.84	10.00	4.10	4.04	15.23	13.40	ns
		–1	0.51	10.07	0.04	0.86	0.36	10.07	8.51	3.48	3.44	12.96	11.40	ns
		–2	0.45	8.84	0.03	0.76	0.32	8.84	7.47	3.06	3.02	11.38	10.00	ns
100 μA	6 mA	Std.	0.60	7.59	0.04	1.02	0.43	7.59	6.18	4.62	4.95	10.98	9.57	ns
		–1	0.51	6.45	0.04	0.86	0.36	6.45	5.25	3.93	4.21	9.34	8.14	ns
		–2	0.45	5.67	0.03	0.76	0.32	5.67	4.61	3.45	3.70	8.20	7.15	ns
100 μA	8 mA	Std.	0.60	7.59	0.04	1.02	0.43	7.59	6.18	4.62	4.95	10.98	9.57	ns
		–1	0.51	6.45	0.04	0.86	0.36	6.45	5.25	3.93	4.21	9.34	8.14	ns
		–2	0.45	5.67	0.03	0.76	0.32	5.67	4.61	3.45	3.70	8.20	7.15	ns
100 μA	12 mA	Std.	0.60	5.46	0.04	1.02	0.43	5.46	4.29	4.97	5.54	8.86	7.68	ns
		–1	0.51	4.65	0.04	0.86	0.36	4.65	3.65	4.22	4.71	7.53	6.54	ns
		–2	0.45	4.08	0.03	0.76	0.32	4.08	3.20	3.71	4.14	6.61	5.74	ns
100 μA	16 mA	Std.	0.60	5.15	0.04	1.02	0.43	5.15	3.89	5.04	5.69	8.55	7.29	ns
		–1	0.51	4.38	0.04	0.86	0.36	4.38	3.31	4.29	4.84	7.27	6.20	ns
		–2	0.45	3.85	0.03	0.76	0.32	3.85	2.91	3.77	4.25	6.38	5.44	ns
100 μA	24 mA	Std.	0.60	4.75	0.04	1.02	0.43	4.75	3.22	5.14	6.28	8.15	6.61	ns
		–1	0.51	4.04	0.04	0.86	0.36	4.04	2.74	4.37	5.34	6.93	5.62	ns
		–2	0.45	3.55	0.03	0.76	0.32	3.55	2.40	3.84	4.69	6.09	4.94	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-81 • 1.5 V LVC MOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-82 • 1.5 V LVC MOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-96 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-15 on page 2-69 for more information.

Table 2-97 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-16 on page 2-71 for more information.

Output DDR Module

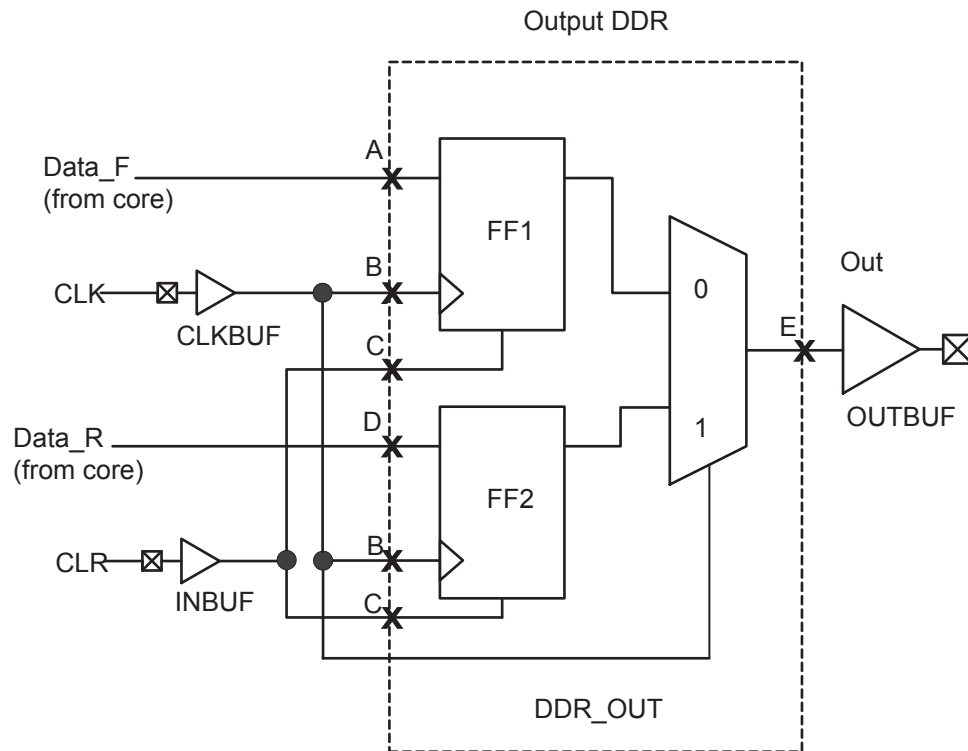


Figure 2-22 • Output DDR Timing Model

Table 2-103 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDROCLKQ}	Clock-to-Out	B, E
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out	C, E
$t_{\text{DDROREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRORECCLR}}$	Clear Recovery	C, B
t_{DDROSUD1}	Data Setup Data_F	A, B
t_{DDROSUD2}	Data Setup Data_R	D, B
t_{DDROHD1}	Data Hold Data_F	A, B
t_{DDROHD2}	Data Hold Data_R	D, B

Timing Characteristics

Table 2-105 • Combinatorial Cell Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-2	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.40	0.46	0.54	ns
AND2	$Y = A \cdot B$	t_{PD}	0.47	0.54	0.63	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.47	0.54	0.63	ns
OR2	$Y = A + B$	t_{PD}	0.49	0.55	0.65	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.49	0.55	0.65	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.74	0.84	0.99	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.87	1.00	1.17	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.51	0.58	0.68	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion](#), [IGLOO/e](#), and [ProASIC3/E Macro Library Guide](#).

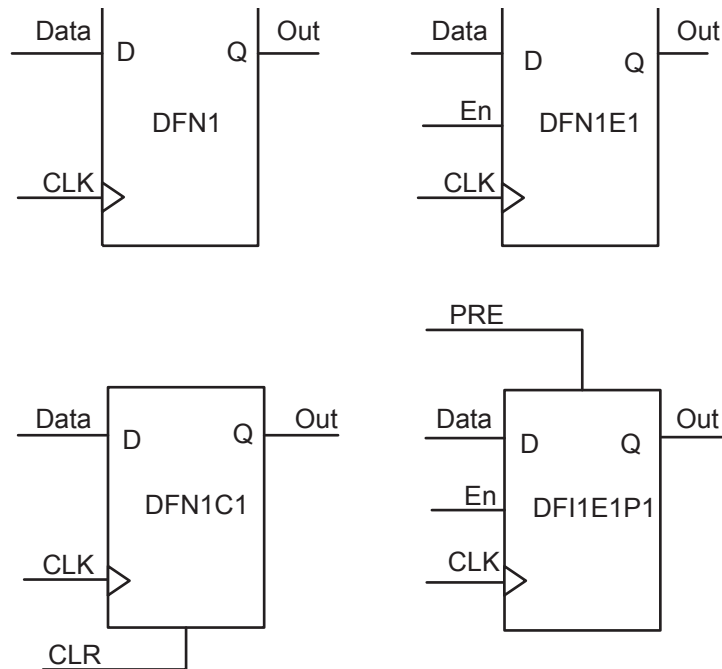


Figure 2-26 • Sample of Sequential Cells

3 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. x is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for a complete board solution for the PLL analog power supply and ground.

There is one VCCPLF pin on ProASIC3 devices.

VCOMPLA/B/C/D/E/F **PLL Ground**

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC3 devices.

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

User's Guides

ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

<http://www.microsemi.com/soc/documents/PckgMechDrwns.pdf>

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are at <http://www.microsemi.com/products/solutions/package/docs.aspx>.

QN132	
Pin Number	A3P125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	A3P125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

QN132	
Pin Number	A3P125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

CS121	
Pin Number	A3P060 Function
A1	GNDQ
A2	IO01RSB0
A3	GAA1/IO03RSB0
A4	GAC1/IO07RSB0
A5	IO15RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	GBB1/IO22RSB0
A9	GBA1/IO24RSB0
A10	GNDQ
A11	VMV0
B1	GAA2/IO95RSB1
B2	IO00RSB0
B3	GAA0/IO02RSB0
B4	GAC0/IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO16RSB0
B8	GBC1/IO20RSB0
B9	GBB0/IO21RSB0
B10	GBB2/IO27RSB0
B11	GBA2/IO25RSB0
C1	IO89RSB1
C2	GAC2/IO91RSB1
C3	GAB1/IO05RSB0
C4	GAB0/IO04RSB0
C5	IO09RSB0
C6	IO14RSB0
C7	GBA0/IO23RSB0
C8	GBC0/IO19RSB0
C9	IO26RSB0
C10	IO28RSB0
C11	GBC2/IO29RSB0
D1	IO88RSB1
D2	IO90RSB1
D3	GAB2/IO93RSB1

CS121	
Pin Number	A3P060 Function
D4	IO10RSB0
D5	IO11RSB0
D6	IO18RSB0
D7	IO32RSB0
D8	IO31RSB0
D9	GCA2/IO41RSB0
D10	IO30RSB0
D11	IO33RSB0
E1	IO87RSB1
E2	GFC0/IO85RSB1
E3	IO92RSB1
E4	IO94RSB1
E5	VCC
E6	VCCIB0
E7	GND
E8	GCC0/IO36RSB0
E9	IO34RSB0
E10	GCB1/IO37RSB0
E11	GCC1/IO35RSB0
F1	VCOMPLF
F2	GFB0/IO83RSB1
F3	GFA0/IO82RSB1
F4	GFC1/IO86RSB1
F5	VCCIB1
F6	VCC
F7	VCCIB0
F8	GCB2/IO42RSB0
F9	GCC2/IO43RSB0
F10	GCB0/IO38RSB0
F11	GCA1/IO39RSB0
G1	VCCPLF
G2	GFB2/IO79RSB1
G3	GFA1/IO81RSB1
G4	GFB1/IO84RSB1
G5	GND
G6	VCCIB1

CS121	
Pin Number	A3P060 Function
G7	VCC
G8	GDC0/IO46RSB0
G9	GDA1/IO49RSB0
G10	GDB0/IO48RSB0
G11	GCA0/IO40RSB0
H1	IO75RSB1
H2	IO76RSB1
H3	GFC2/IO78RSB1
H4	GFA2/IO80RSB1
H5	IO77RSB1
H6	GEC2/IO66RSB1
H7	IO54RSB1
H8	GDC2/IO53RSB1
H9	VJTAG
H10	TRST
H11	IO44RSB0
J1	GEC1/IO74RSB1
J2	GEC0/IO73RSB1
J3	GEB1/IO72RSB1
J4	GEA0/IO69RSB1
J5	GEB2/IO67RSB1
J6	IO62RSB1
J7	GDA2/IO51RSB1
J8	GDB2/IO52RSB1
J9	TDI
J10	TDO
J11	GDC1/IO45RSB0
K1	GEB0/IO71RSB1
K2	GEA1/IO70RSB1
K3	GEA2/IO68RSB1
K4	IO64RSB1
K5	IO60RSB1
K6	IO59RSB1
K7	IO56RSB1
K8	TCK
K9	TMS

PQ208	
Pin Number	A3P600 Function
109	TRST
110	VJTAG
111	GDA0/IO88NDB1
112	GDA1/IO88PDB1
113	GDB0/IO87NDB1
114	GDB1/IO87PDB1
115	GDC0/IO86NDB1
116	GDC1/IO86PDB1
117	IO84NDB1
118	IO84PDB1
119	IO82NDB1
120	IO82PDB1
121	IO81PSB1
122	GND
123	VCCIB1
124	IO77NDB1
125	IO77PDB1
126	NC
127	IO74NDB1
128	GCC2/IO74PDB1
129	GCB2/IO73PSB1
130	GND
131	GCA2/IO72PSB1
132	GCA1/IO71PDB1
133	GCA0/IO71NDB1
134	GCB0/IO70NDB1
135	GCB1/IO70PDB1
136	GCC0/IO69NDB1
137	GCC1/IO69PDB1
138	IO67NDB1
139	IO67PDB1
140	VCCIB1
141	GND
142	VCC
143	IO65PSB1
144	IO64NDB1

PQ208	
Pin Number	A3P600 Function
145	IO64PDB1
146	IO63NDB1
147	IO63PDB1
148	IO62NDB1
149	GBC2/IO62PDB1
150	IO61NDB1
151	GBB2/IO61PDB1
152	IO60NDB1
153	GBA2/IO60PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO59RSB0
159	GBA0/IO58RSB0
160	GBB1/IO57RSB0
161	GBB0/IO56RSB0
162	GND
163	GBC1/IO55RSB0
164	GBC0/IO54RSB0
165	IO52RSB0
166	IO50RSB0
167	IO48RSB0
168	IO46RSB0
169	IO44RSB0
170	VCCIB0
171	VCC
172	IO36RSB0
173	IO35RSB0
174	IO34RSB0
175	IO33RSB0
176	IO32RSB0
177	IO31RSB0
178	GND
179	IO29RSB0
180	IO28RSB0

PQ208	
Pin Number	A3P600 Function
181	IO27RSB0
182	IO26RSB0
183	IO25RSB0
184	IO24RSB0
185	IO23RSB0
186	VCCIB0
187	VCC
188	IO20RSB0
189	IO19RSB0
190	IO18RSB0
191	IO17RSB0
192	IO16RSB0
193	IO14RSB0
194	IO12RSB0
195	GND
196	IO10RSB0
197	IO09RSB0
198	IO08RSB0
199	IO07RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG144	
Pin Number	A3P060 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO04RSB0
A4	GAB1/IO05RSB0
A5	IO08RSB0
A6	GND
A7	IO11RSB0
A8	VCC
A9	IO16RSB0
A10	GBA0/IO23RSB0
A11	GBA1/IO24RSB0
A12	GNDQ
B1	GAB2/IO53RSB1
B2	GND
B3	GAA0/IO02RSB0
B4	GAA1/IO03RSB0
B5	IO00RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO14RSB0
B9	GBB0/IO21RSB0
B10	GBB1/IO22RSB0
B11	GND
B12	VMV0
C1	IO95RSB1
C2	GFA2/IO83RSB1
C3	GAC2/IO94RSB1
C4	VCC
C5	IO01RSB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO17RSB0
C10	GBA2/IO25RSB0
C11	IO26RSB0
C12	GBC2/IO29RSB0

FG144	
Pin Number	A3P060 Function
D1	IO91RSB1
D2	IO92RSB1
D3	IO93RSB1
D4	GAA2/IO51RSB1
D5	GAC0/IO06RSB0
D6	GAC1/IO07RSB0
D7	GBC0/IO19RSB0
D8	GBC1/IO20RSB0
D9	GBB2/IO27RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	GCB1/IO37RSB0
E1	VCC
E2	GFC0/IO88RSB1
E3	GFC1/IO89RSB1
E4	VCCIB1
E5	IO52RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO35RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO40RSB0
E12	IO30RSB0
F1	GFB0/IO86RSB1
F2	VCOMPLF
F3	GFB1/IO87RSB1
F4	IO90RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO36RSB0
F9	GCB0/IO38RSB0
F10	GND
F11	GCA1/IO39RSB0
F12	GCA2/IO41RSB0

FG144	
Pin Number	A3P060 Function
G1	GFA1/IO84RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO85RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO45RSB0
G9	IO32RSB0
G10	GCC2/IO43RSB0
G11	IO31RSB0
G12	GCB2/IO42RSB0
H1	VCC
H2	GFB2/IO82RSB1
H3	GFC2/IO81RSB1
H4	GEC1/IO77RSB1
H5	VCC
H6	IO34RSB0
H7	IO44RSB0
H8	GDB2/IO55RSB1
H9	GDC0/IO46RSB0
H10	VCCIB0
H11	IO33RSB0
H12	VCC
J1	GEB1/IO75RSB1
J2	IO78RSB1
J3	VCCIB1
J4	GEC0/IO76RSB1
J5	IO79RSB1
J6	IO80RSB1
J7	VCC
J8	TCK
J9	GDA2/IO54RSB1
J10	TDO
J11	GDA1/IO49RSB0
J12	GDB1/IO47RSB0

FG144	
Pin Number	A3P125 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO11RSB0
A6	GND
A7	IO18RSB0
A8	VCC
A9	IO25RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO69RSB1
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO08RSB0
B6	IO14RSB0
B7	IO19RSB0
B8	IO22RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV0
C1	IO132RSB1
C2	GFA2/IO120RSB1
C3	GAC2/IO131RSB1
C4	VCC
C5	IO10RSB0
C6	IO12RSB0
C7	IO21RSB0
C8	IO24RSB0
C9	IO27RSB0
C10	GBA2/IO41RSB0
C11	IO42RSB0
C12	GBC2/IO45RSB0

FG144	
Pin Number	A3P125 Function
D1	IO128RSB1
D2	IO129RSB1
D3	IO130RSB1
D4	GAA2/IO67RSB1
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO43RSB0
D10	IO28RSB0
D11	IO44RSB0
D12	GCB1/IO53RSB0
E1	VCC
E2	GFC0/IO125RSB1
E3	GFC1/IO126RSB1
E4	VCCIB1
E5	IO68RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO51RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO56RSB0
E12	IO46RSB0
F1	GFB0/IO123RSB1
F2	VCOMPLF
F3	GFB1/IO124RSB1
F4	IO127RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO52RSB0
F9	GCB0/IO54RSB0
F10	GND
F11	GCA1/IO55RSB0
F12	GCA2/IO57RSB0

FG144	
Pin Number	A3P125 Function
G1	GFA1/IO121RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO122RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO61RSB0
G9	IO48RSB0
G10	GCC2/IO59RSB0
G11	IO47RSB0
G12	GCB2/IO58RSB0
H1	VCC
H2	GFB2/IO119RSB1
H3	GFC2/IO118RSB1
H4	GEC1/IO112RSB1
H5	VCC
H6	IO50RSB0
H7	IO60RSB0
H8	GDB2/IO71RSB1
H9	GDC0/IO62RSB0
H10	VCCIB0
H11	IO49RSB0
H12	VCC
J1	GEB1/IO110RSB1
J2	IO115RSB1
J3	VCCIB1
J4	GEC0/IO111RSB1
J5	IO116RSB1
J6	IO117RSB1
J7	VCC
J8	TCK
J9	GDA2/IO70RSB1
J10	TDO
J11	GDA1/IO65RSB0
J12	GDB1/IO63RSB0

FG256	
Pin Number	A3P1000 Function
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

Revision	Changes	Page
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{\text{ambient}} = 0^{\circ}\text{C}$ to 85°C .	2-2
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).	2-90
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C , with an example of six months instead of three months (SAR 37933).	2-31
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Advance v0.6 (continued)	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	The "Introduction" of the "Advanced I/Os" section was updated.	2-28
	The "I/O Banks" section is new. This section explains the following types of I/Os: Advanced Standard+ Standard Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above.	2-29
	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards	2-29
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-32
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-35
	Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices.	2-64
	The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated.	2-64
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-41
	A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected).	2-30
	Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications	2-45
	Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device)	2-83
	Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated.	2-84
	Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated.	2-84
	The "x" was updated in the "User I/O Naming Convention" section.	2-48
	The "VCC Core Supply Voltage" pin description was updated.	2-50
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-50
	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-50
	The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-50
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51