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Understanding [Embedded - FPGAs (Field Programmable Gate Array)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	71
Number of Gates	125000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p125-vqg100i

ProASIC3 Device Family Overview

ProASIC3 DC and Switching Characteristics

Pin Descriptions

Package Pin Assignments

Datasheet Information

Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3 device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based ProASIC3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2
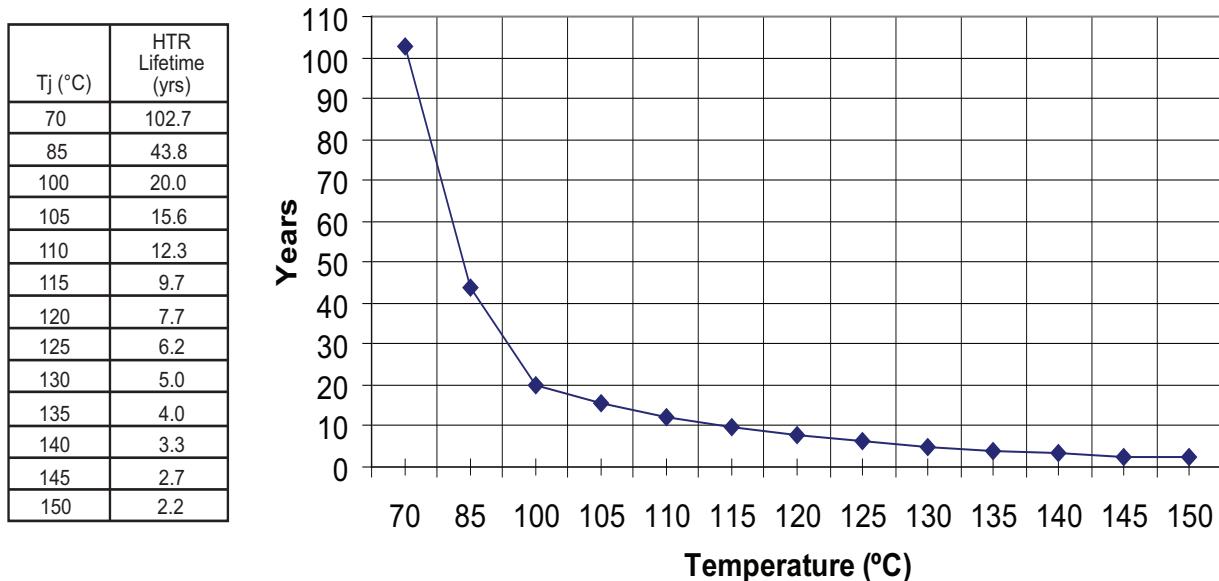
Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

Figure 2-1 • **High-Temperature Data Retention (HTR)**

Table 2-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C)	Maximum Operating Junction Temperature T_J (°C)[2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

Table 2-4 • **Overshoot and Undershoot Limits [1]**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.
2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
3. This table does not provide PCI overshoot/undershoot limits.

Table 2-9 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-10 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range[3]	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

RAM Contribution—P_{MEMORY}

$P_{MEMORY} = P_{AC11} * N_{BLOCKS} * F_{READ-CLOCK} * \beta_2 + P_{AC12} * N_{BLOCK} * F_{WRITE-CLOCK} * \beta_3$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ-CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{WRITE-CLOCK}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in Table 2-17 on page 2-14.

PLL Contribution—P_{PLL}

$P_{PLL} = P_{DC4} + P_{AC13} * F_{CLKOUT}$

F_{CLKOUT} is the output clock frequency.[1]

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1   = 50%
  - Bit 2   = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-16 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-17 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

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1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{AC14} * F_{CLKOUT}$ product) to the total PLL contribution.*

Table 2-44 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
2 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	−1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	−2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
4 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	−1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	−2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
6 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	−1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	−2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
8 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	−1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	−2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
12 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	−1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	−2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns
16 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	−1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	−2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-45 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
2 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	−1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	−2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
4 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	−1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	−2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
6 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	−1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	−2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
8 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	−1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-66 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA[3]	Max mA[3]	μA[4]	μA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-67 • **Minimum and Maximum DC Input and Output Levels**
Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA[3]	Max mA[3]	μA[4]	μA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	44	35	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

## *Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear*
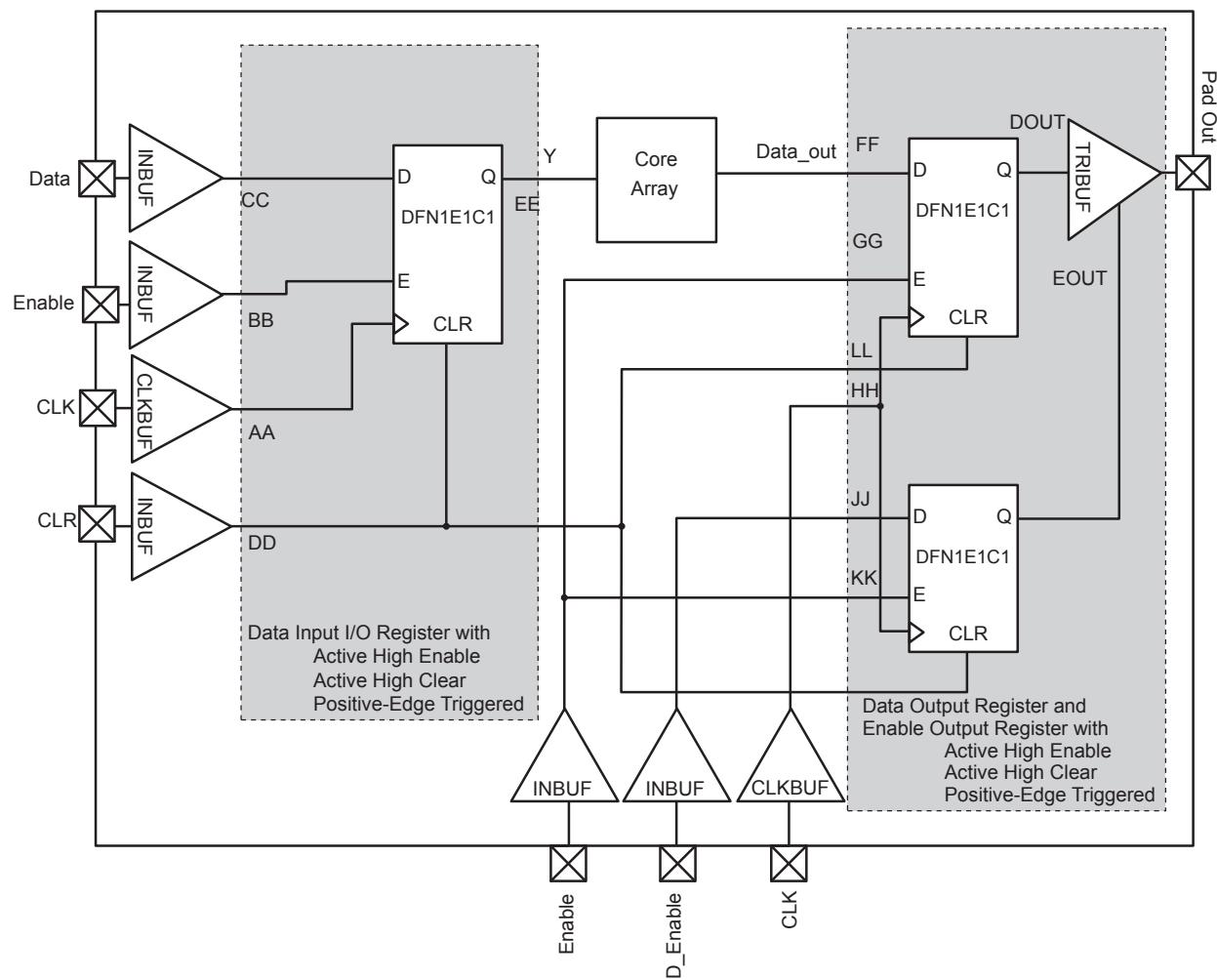
Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Output Enable Register
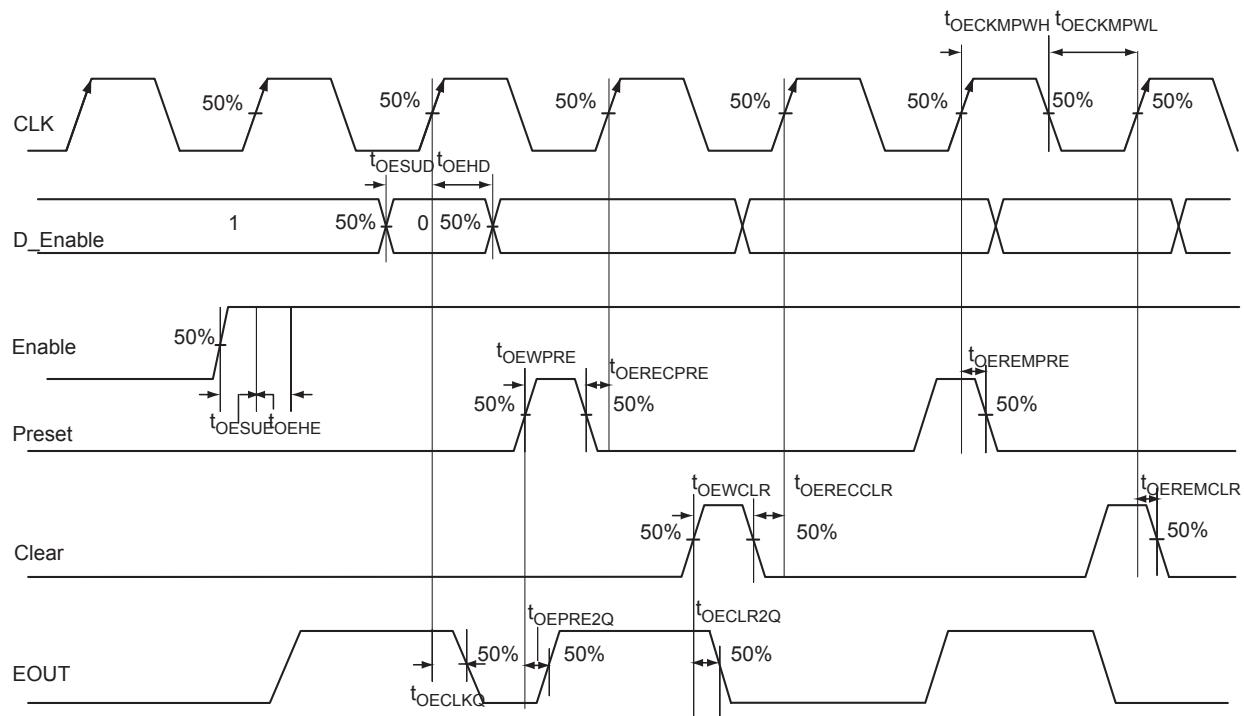
Figure 2-19 • **Output Enable Register Timing Diagram**
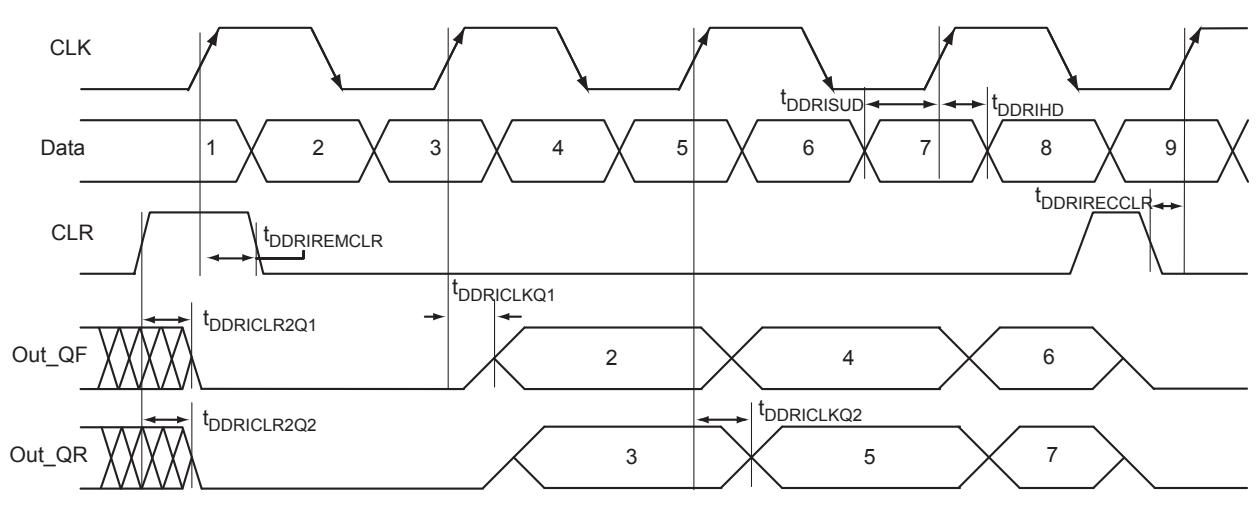
Figure 2-21 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-102 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.27	0.31	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.39	0.44	0.52	ns
$t_{DDRISUD}$	Data Setup for Input DDR (Fall)	0.25	0.28	0.33	ns
	Data Setup for Input DDR (Rise)	0.25	0.28	0.33	ns
t_{DDRIHD}	Data Hold for Input DDR (Fall)	0.00	0.00	0.00	ns
	Data Hold for Input DDR (Rise)	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.46	0.53	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	309	263	MHz

Note: For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.

QN132	
Pin Number	**A3P250 Function**
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

CS121			CS121			CS121	
Pin Number	**A3P060 Function**		**Pin Number**	**A3P060 Function**		**Pin Number**	**A3P060 Function**
A1	GNDQ		D4	IO10RSB0		G7	VCC
A2	IO01RSB0		D5	IO11RSB0		G8	GDC0/IO46RSB0
A3	GAA1/IO03RSB0		D6	IO18RSB0		G9	GDA1/IO49RSB0
A4	GAC1/IO07RSB0		D7	IO32RSB0		G10	GDB0/IO48RSB0
A5	IO15RSB0		D8	IO31RSB0		G11	GCA0/IO40RSB0
A6	IO13RSB0		D9	GCA2/IO41RSB0		H1	IO75RSB1
A7	IO17RSB0		D10	IO30RSB0		H2	IO76RSB1
A8	GBB1/IO22RSB0		D11	IO33RSB0		H3	GFC2/IO78RSB1
A9	GBA1/IO24RSB0		E1	IO87RSB1		H4	GFA2/IO80RSB1
A10	GNDQ		E2	GFC0/IO85RSB1		H5	IO77RSB1
A11	VMV0		E3	IO92RSB1		H6	GEC2/IO66RSB1
B1	GAA2/IO95RSB1		E4	IO94RSB1		H7	IO54RSB1
B2	IO00RSB0		E5	VCC		H8	GDC2/IO53RSB1
B3	GAA0/IO02RSB0		E6	VCCIB0		H9	VJTAG
B4	GAC0/IO06RSB0		E7	GND		H10	TRST
B5	IO08RSB0		E8	GCC0/IO36RSB0		H11	IO44RSB0
B6	IO12RSB0		E9	IO34RSB0		J1	GEC1/IO74RSB1
B7	IO16RSB0		E10	GCB1/IO37RSB0		J2	GEC0/IO73RSB1
B8	GBC1/IO20RSB0		E11	GCC1/IO35RSB0		J3	GEB1/IO72RSB1
B9	GBB0/IO21RSB0		F1	VCOMPLF		J4	GEA0/IO69RSB1
B10	GBB2/IO27RSB0		F2	GFB0/IO83RSB1		J5	GEB2/IO67RSB1
B11	GBA2/IO25RSB0		F3	GFA0/IO82RSB1		J6	IO62RSB1
C1	IO89RSB1		F4	GFC1/IO86RSB1		J7	GDA2/IO51RSB1
C2	GAC2/IO91RSB1		F5	VCCIB1		J8	GDB2/IO52RSB1
C3	GAB1/IO05RSB0		F6	VCC		J9	TDI
C4	GAB0/IO04RSB0		F7	VCCIB0		J10	TDO
C5	IO09RSB0		F8	GCB2/IO42RSB0		J11	GDC1/IO45RSB0
C6	IO14RSB0		F9	GCC2/IO43RSB0		K1	GEB0/IO71RSB1
C7	GBA0/IO23RSB0		F10	GCB0/IO38RSB0		K2	GEA1/IO70RSB1
C8	GBC0/IO19RSB0		F11	GCA1/IO39RSB0		K3	GEA2/IO68RSB1
C9	IO26RSB0		G1	VCCPLF		K4	IO64RSB1
C10	IO28RSB0		G2	GFB2/IO79RSB1		K5	IO60RSB1
C11	GBC2/IO29RSB0		G3	GFA1/IO81RSB1		K6	IO59RSB1
D1	IO88RSB1		G4	GFB1/IO84RSB1		K7	IO56RSB1
D2	IO90RSB1		G5	GND		K8	TCK
D3	GAB2/IO93RSB1		G6	VCCIB1		K9	TMS

VQ100		VQ100		VQ100	
Pin Number	**A3P250 Function**	**Pin Number**	**A3P250 Function**	**Pin Number**	**A3P250 Function**
1	GND	37	VCC	73	GBA2/IO41PDB1
2	GAA2/IO118UDB3	38	GND	74	VMV1
3	IO118VDB3	39	VCCIB2	75	GNDQ
4	GAB2/IO117UDB3	40	IO77RSB2	76	GBA1/IO40RSB0
5	IO117VDB3	41	IO74RSB2	77	GBA0/IO39RSB0
6	GAC2/IO116UDB3	42	IO71RSB2	78	GBB1/IO38RSB0
7	IO116VDB3	43	GDC2/IO63RSB2	79	GBB0/IO37RSB0
8	IO112PSB3	44	GDB2/IO62RSB2	80	GBC1/IO36RSB0
9	GND	45	GDA2/IO61RSB2	81	GBC0/IO35RSB0
10	GFB1/IO109PDB3	46	GNDQ	82	IO29RSB0
11	GFB0/IO109NDB3	47	TCK	83	IO27RSB0
12	VCOMPLF	48	TDI	84	IO25RSB0
13	GFA0/IO108NPB3	49	TMS	85	IO23RSB0
14	VCCPLF	50	VMV2	86	IO21RSB0
15	GFA1/IO108PPB3	51	GND	87	VCCIB0
16	GFA2/IO107PSB3	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB3	54	TDO	90	IO15RSB0
19	GFC2/IO105PSB3	55	TRST	91	IO13RSB0
20	GEC1/IO100PDB3	56	VJTAG	92	IO11RSB0
21	GEC0/IO100NDB3	57	GDA1/IO60USB1	93	GAC1/IO05RSB0
22	GEA1/IO98PDB3	58	GDC0/IO58VDB1	94	GAC0/IO04RSB0
23	GEA0/IO98NDB3	59	GDC1/IO58UDB1	95	GAB1/IO03RSB0
24	VMV3	60	IO52NDB1	96	GAB0/IO02RSB0
25	GNDQ	61	GCB2/IO52PDB1	97	GAA1/IO01RSB0
26	GEA2/IO97RSB2	62	GCA1/IO50PDB1	98	GAA0/IO00RSB0
27	GEB2/IO96RSB2	63	GCA0/IO50NDB1	99	GNDQ
28	GEC2/IO95RSB2	64	GCC0/IO48NDB1	100	VMV0
29	IO93RSB2	65	GCC1/IO48PDB1		
30	IO92RSB2	66	VCCIB1		
31	IO91RSB2	67	GND		
32	IO90RSB2	68	VCC		
33	IO88RSB2	69	IO43NDB1		
34	IO86RSB2	70	GBC2/IO43PDB1		
35	IO85RSB2	71	GBB2/IO42PSB1		
36	IO84RSB2	72	IO41NDB1		

PQ208	
Pin Number	A3P125 Function
109	TRST
110	VJTAG
111	GDA0/IO66RSB0
112	GDA1/IO65RSB0
113	GDB0/IO64RSB0
114	GDB1/IO63RSB0
115	GDC0/IO62RSB0
116	GDC1/IO61RSB0
117	NC
118	NC
119	NC
120	NC
121	NC
122	GND
123	VCCIB0
124	NC
125	NC
126	VCC
127	IO60RSB0
128	GCC2/IO59RSB0
129	GCB2/IO58RSB0
130	GND
131	GCA2/IO57RSB0
132	GCA0/IO56RSB0
133	GCA1/IO55RSB0
134	GCB0/IO54RSB0
135	GCB1/IO53RSB0
136	GCC0/IO52RSB0
137	GCC1/IO51RSB0
138	IO50RSB0
139	IO49RSB0
140	VCCIB0
141	GND
142	VCC
143	IO48RSB0
144	IO47RSB0

PQ208	
Pin Number	A3P125 Function
145	IO46RSB0
146	NC
147	NC
148	NC
149	GBC2/IO45RSB0
150	IO44RSB0
151	GBB2/IO43RSB0
152	IO42RSB0
153	GBA2/IO41RSB0
154	VMV0
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	VCCIB0
171	VCC
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0

PQ208	
Pin Number	A3P125 Function
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	VCCIB0
187	VCC
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG256		FG256		FG256	
Pin Number	**A3P1000 Function**	**Pin Number**	**A3P1000 Function**	**Pin Number**	**A3P1000 Function**
H3	GFB1/IO208PPB3	K9	GND	M15	GDC1/IO111PDB1
H4	VCOMPLF	K10	GND	M16	IO107NDB1
H5	GFC0/IO209NPB3	K11	VCC	N1	IO194PSB3
H6	VCC	K12	VCCIB1	N2	IO192PPB3
H7	GND	K13	IO95NPB1	N3	GEC1/IO190PPB3
H8	GND	K14	IO100NPB1	N4	IO192NPB3
H9	GND	K15	IO102NDB1	N5	GNDQ
H10	GND	K16	IO102PDB1	N6	GEA2/IO187RSB2
H11	VCC	L1	IO202NDB3	N7	IO161RSB2
H12	GCC0/IO91NPB1	L2	IO202PDB3	N8	IO155RSB2
H13	GCB1/IO92PPB1	L3	IO196PPB3	N9	IO141RSB2
H14	GCA0/IO93NPB1	L4	IO193PPB3	N10	IO129RSB2
H15	IO96NPB1	L5	VCCIB3	N11	IO124RSB2
H16	GCB0/IO92NPB1	L6	GND	N12	GNDQ
J1	GFA2/IO206PSB3	L7	VCC	N13	IO110PDB1
J2	GFA1/IO207PDB3	L8	VCC	N14	VJTAG
J3	VCCPLF	L9	VCC	N15	GDC0/IO111NDB1
J4	IO205NDB3	L10	VCC	N16	GDA1/IO113PDB1
J5	GFB2/IO205PDB3	L11	GND	P1	GEB1/IO189PDB3
J6	VCC	L12	VCCIB1	P2	GEB0/IO189NDB3
J7	GND	L13	GDB0/IO112NPB1	P3	VMV2
J8	GND	L14	IO106NDB1	P4	IO179RSB2
J9	GND	L15	IO106PDB1	P5	IO171RSB2
J10	GND	L16	IO107PDB1	P6	IO165RSB2
J11	VCC	M1	IO197NSB3	P7	IO159RSB2
J12	GCB2/IO95PPB1	M2	IO196NPB3	P8	IO151RSB2
J13	GCA1/IO93PPB1	M3	IO193NPB3	P9	IO137RSB2
J14	GCC2/IO96PPB1	M4	GEC0/IO190NPB3	P10	IO134RSB2
J15	IO100PPB1	M5	VMV3	P11	IO128RSB2
J16	GCA2/IO94PSB1	M6	VCCIB2	P12	VMV1
K1	GFC2/IO204PDB3	M7	VCCIB2	P13	TCK
K2	IO204NDB3	M8	IO147RSB2	P14	VPUMP
K3	IO203NDB3	M9	IO136RSB2	P15	TRST
K4	IO203PDB3	M10	VCCIB2	P16	GDA0/IO113NDB1
K5	VCCIB3	M11	VCCIB2	R1	GEA1/IO188PDB3
K6	VCC	M12	VMV2	R2	GEA0/IO188NDB3
K7	GND	M13	IO110NDB1	R3	IO184RSB2
K8	GND	M14	GDB1/IO112PPB1	R4	GEC2/IO185RSB2

FG484			FG484			FG484	
Pin Number	**A3P400 Function**		**Pin Number**	**A3P400 Function**		**Pin Number**	**A3P400 Function**
E21	NC		G13	IO40RSB0		J5	IO149NPB3
E22	NC		G14	IO46RSB0		J6	IO09RSB0
F1	NC		G15	GNDQ		J7	IO152UDB3
F2	NC		G16	IO47RSB0		J8	VCCIB3
F3	NC		G17	GBB2/IO61PPB1		J9	GND
F4	IO154VDB3		G18	IO53RSB0		J10	VCC
F5	IO155VDB3		G19	IO63NDB1		J11	VCC
F6	IO11RSB0		G20	NC		J12	VCC
F7	IO07RSB0		G21	NC		J13	VCC
F8	GAC0/IO04RSB0		G22	NC		J14	GND
F9	GAC1/IO05RSB0		H1	NC		J15	VCCIB1
F10	IO20RSB0		H2	NC		J16	IO62NDB1
F11	IO24RSB0		H3	VCC		J17	IO49RSB0
F12	IO33RSB0		H4	IO150PDB3		J18	IO64PPB1
F13	IO39RSB0		H5	IO08RSB0		J19	IO66NDB1
F14	IO45RSB0		H6	IO153VDB3		J20	NC
F15	GBC0/IO54RSB0		H7	IO152VDB3		J21	NC
F16	IO48RSB0		H8	VMV0		J22	NC
F17	VMV0		H9	VCCIB0		K1	NC
F18	IO61NPB1		H10	VCCIB0		K2	NC
F19	IO63PDB1		H11	IO25RSB0		K3	NC
F20	NC		H12	IO31RSB0		K4	IO148NDB3
F21	NC		H13	VCCIB0		K5	IO148PDB3
F22	NC		H14	VCCIB0		K6	IO149PPB3
G1	NC		H15	VMV1		K7	GFC1/IO147PPB3
G2	NC		H16	GBC2/IO62PDB1		K8	VCCIB3
G3	NC		H17	IO65RSB1		K9	VCC
G4	IO151VDB3		H18	IO52RSB0		K10	GND
G5	IO151UDB3		H19	IO66PDB1		K11	GND
G6	GAC2/IO153UDB3		H20	VCC		K12	GND
G7	IO06RSB0		H21	NC		K13	GND
G8	GNDQ		H22	NC		K14	VCC
G9	IO10RSB0		J1	NC		K15	VCCIB1
G10	IO19RSB0		J2	NC		K16	GCC1/IO67PPB1
G11	IO26RSB0		J3	NC		K17	IO64NPB1
G12	IO30RSB0		J4	IO150NDB3		K18	IO73PDB1

FG484	
Pin Number	**A3P1000 Function**
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2

FG484	
Pin Number	**A3P1000 Function**
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1

FG484	
Pin Number	**A3P1000 Function**
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC

Revision	Changes	Page
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-2
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).	2-90
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933).	2-31
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 11 (March 2012)	Note indicating that A3P015 is not recommended for new designs has been added. The "Devices Not Recommended For New Designs" section is new (SAR 36760).	I to IV
	The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687).	NA
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide* (SAR 34734).	2-12
	Figure 2-4 • Input Buffer Timing Model and Delays (Example) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34883).	2-32
	Added values for minimum pulse width and removed the FRMAX row from Table 2-107 through Table 2-114 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269).	2-85

Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21