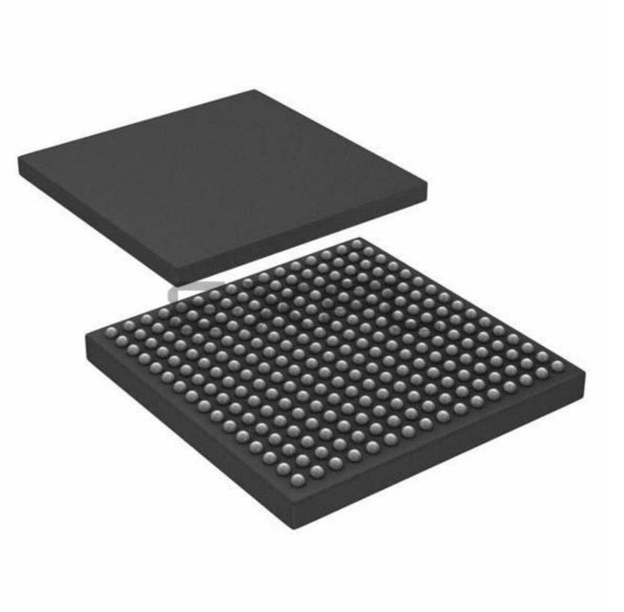
Microchip Technology - A3P250-1FG256 Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

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Applications of Embedded - FPGAs

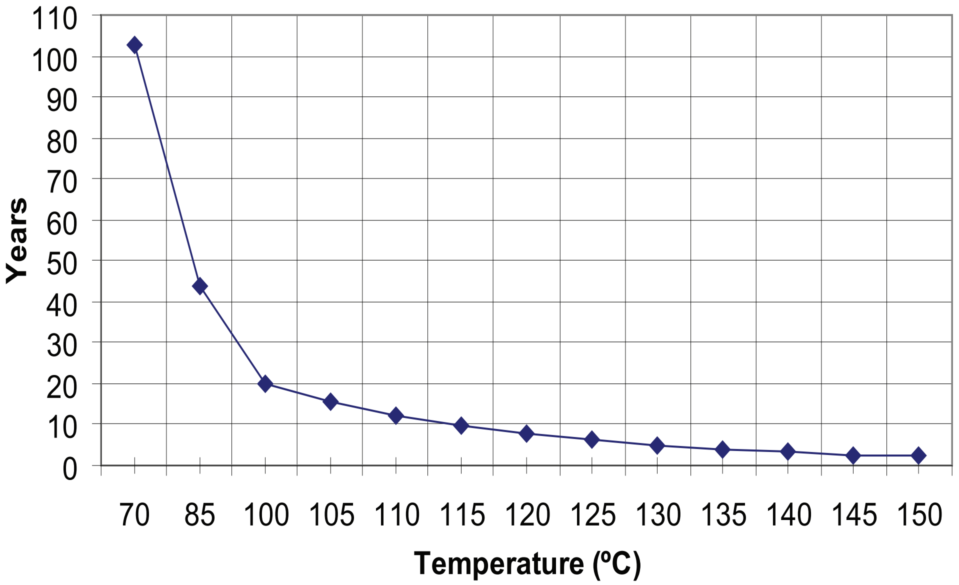
The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	157
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-1fg256

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2



Note: *HTR time is the period during which you would not expect a verify failure due to flash cell leakage.*

Figure 2-1 • **High-Temperature Data Retention (HTR)**

Table 2-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C)	Maximum Operating Junction Temperature T_J (°C)[2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

1. *This is a stress rating only; functional operation at any condition other than those indicated is not implied.*
2. *These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.*

Table 2-4 • **Overshoot and Undershoot Limits [1]**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. *Based on reliability requirements at 85°C.*
2. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
3. *This table does not provide PCI overshoot/undershoot limits.*

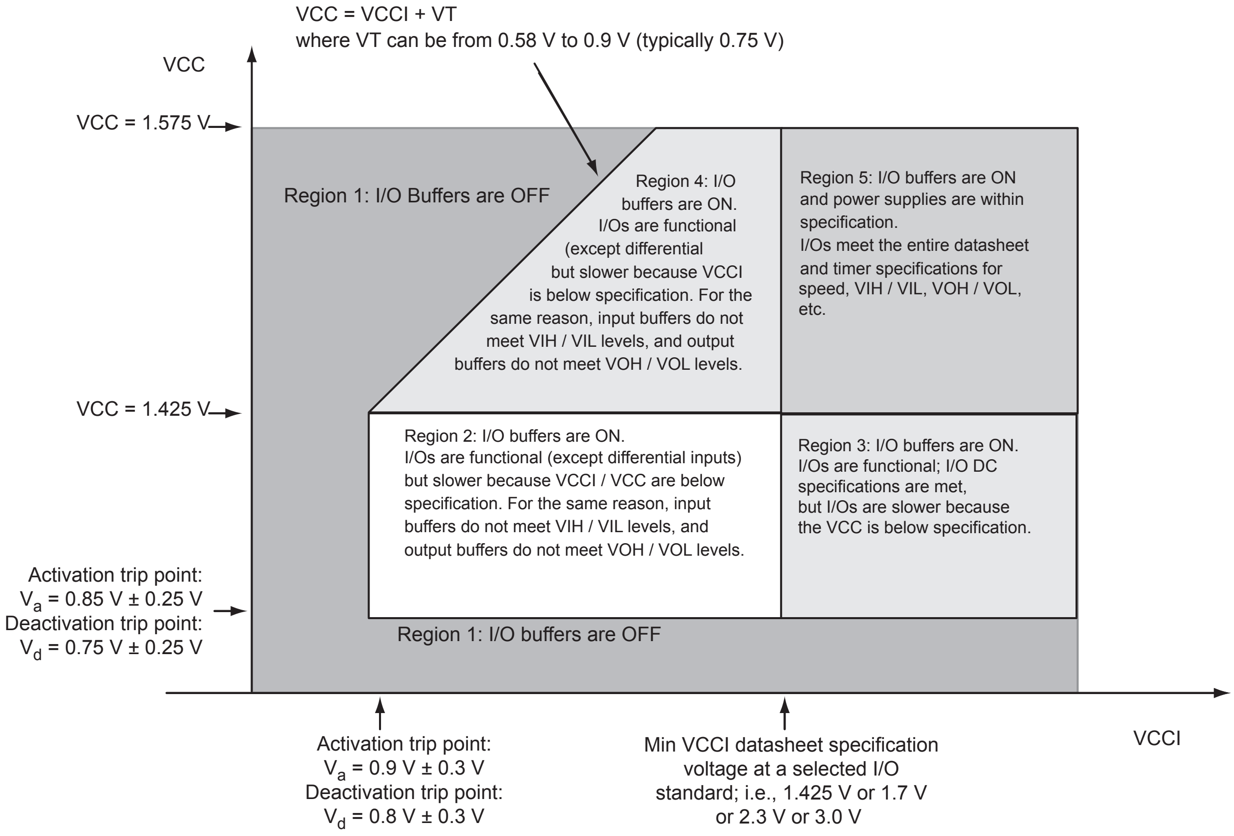


Figure 2-2 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates.

Table 2-9 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-10 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range[3]	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Timing Characteristics

***Table 2-41* • 3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
4 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	–1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	–2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	–1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	–2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-56 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL1	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-57 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-73 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	14.80	0.04	1.20	0.43	13.49	14.80	2.25	1.46	15.73	17.04	ns
	–1	0.56	12.59	0.04	1.02	0.36	11.48	12.59	1.91	1.25	13.38	14.49	ns
	–2	0.49	11.05	0.03	0.90	0.32	10.08	11.05	1.68	1.09	11.75	12.72	ns
4 mA	Std.	0.66	9.90	0.04	1.20	0.43	9.73	9.90	2.65	2.50	11.97	12.13	ns
	–1	0.56	8.42	0.04	1.02	0.36	8.28	8.42	2.26	2.12	10.18	10.32	ns
	–2	0.49	7.39	0.03	0.90	0.32	7.27	7.39	1.98	1.86	8.94	9.06	ns
6 mA	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	–1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	–2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns
8 mA	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	–1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	–2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-74 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	–1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	–2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	–1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	–2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Output Enable Register

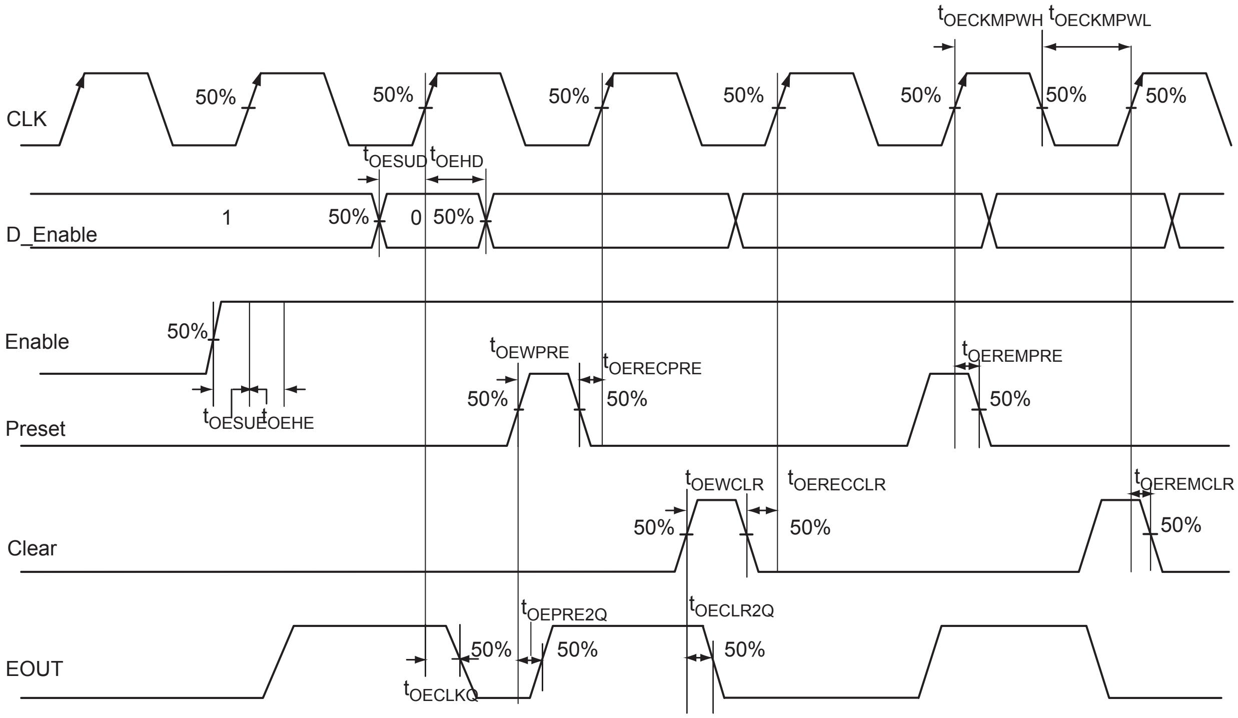


Figure 2-19 • **Output Enable Register Timing Diagram**

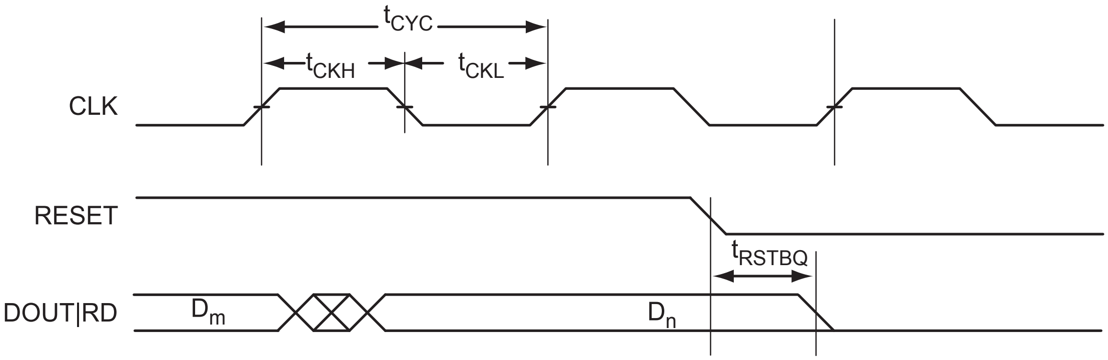


***Figure 2-35* • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

Timing Waveforms

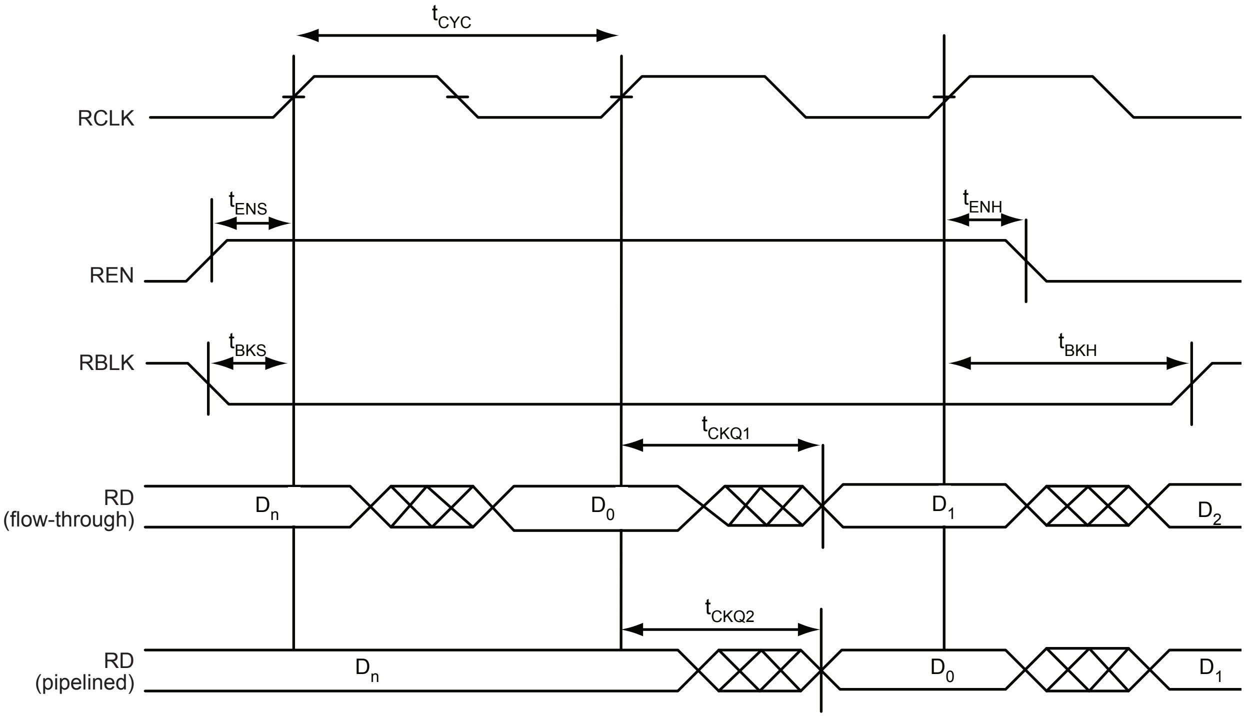


Figure 2-37 **• FIFO Read**

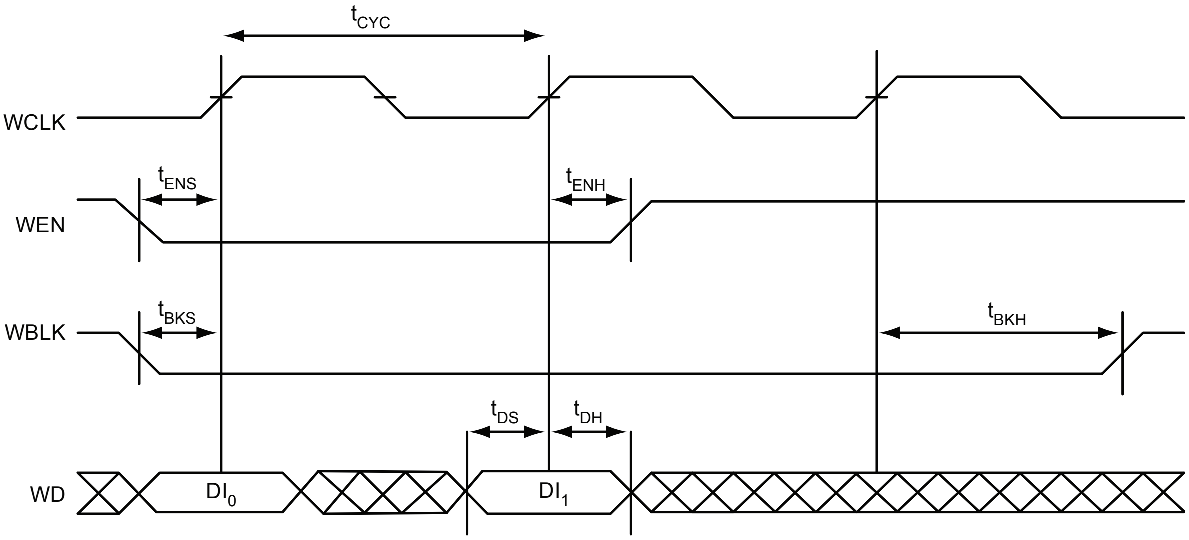


Figure 2-38 **• FIFO Write**

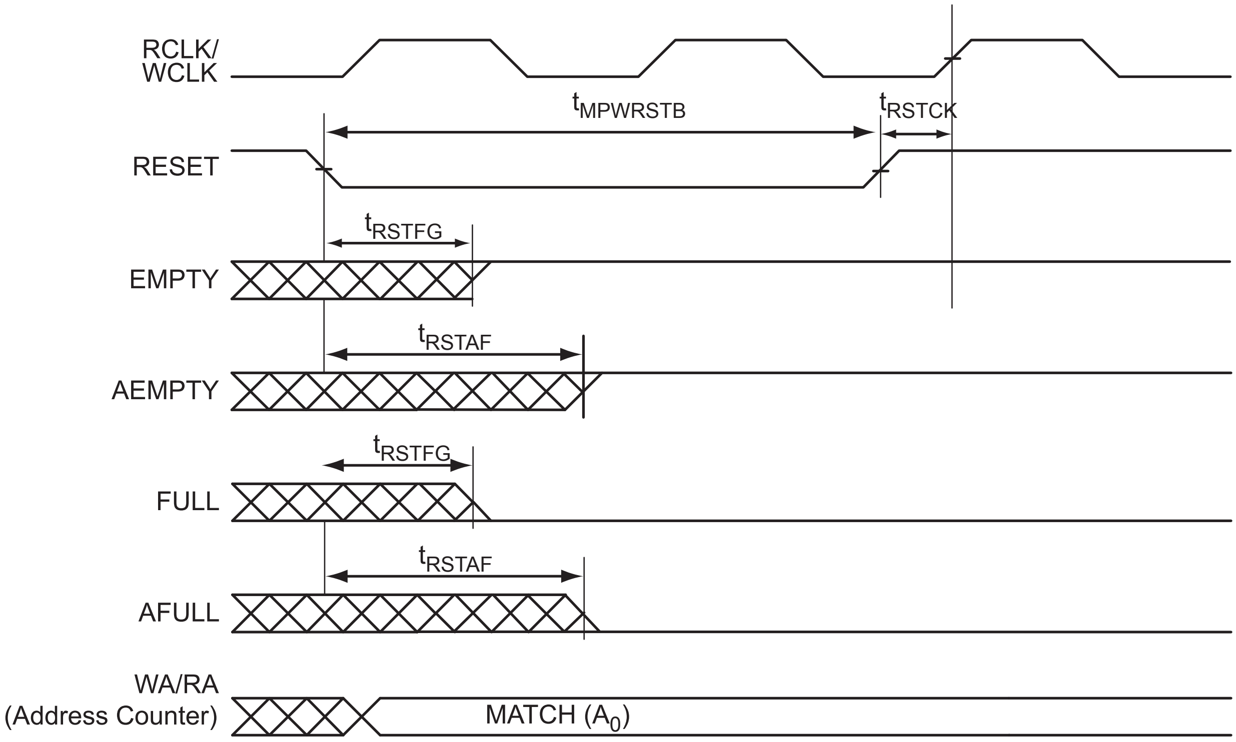


Figure 2-39 • **FIFO Reset**

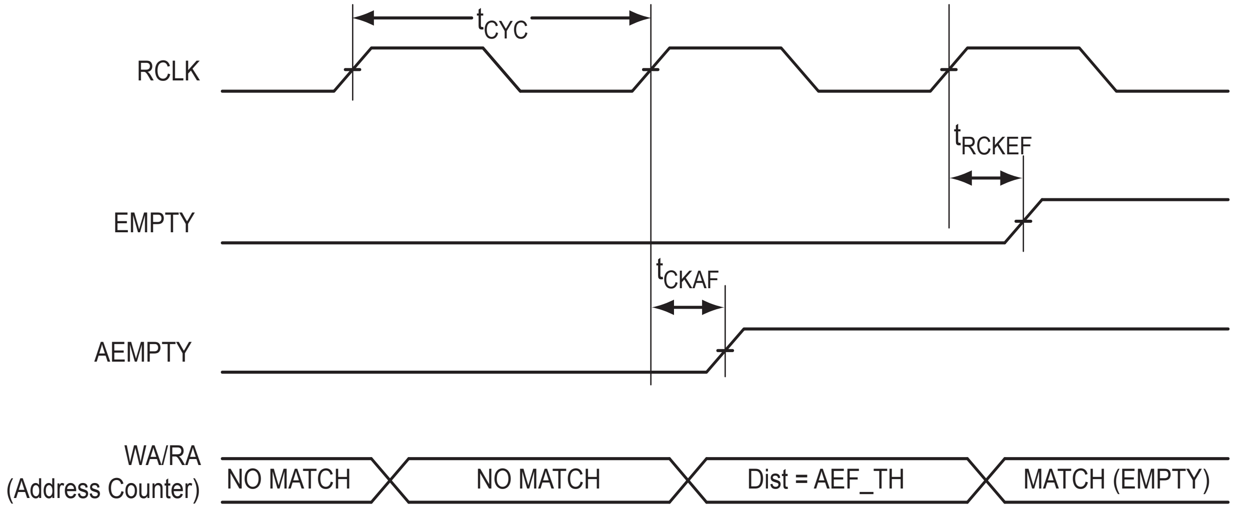
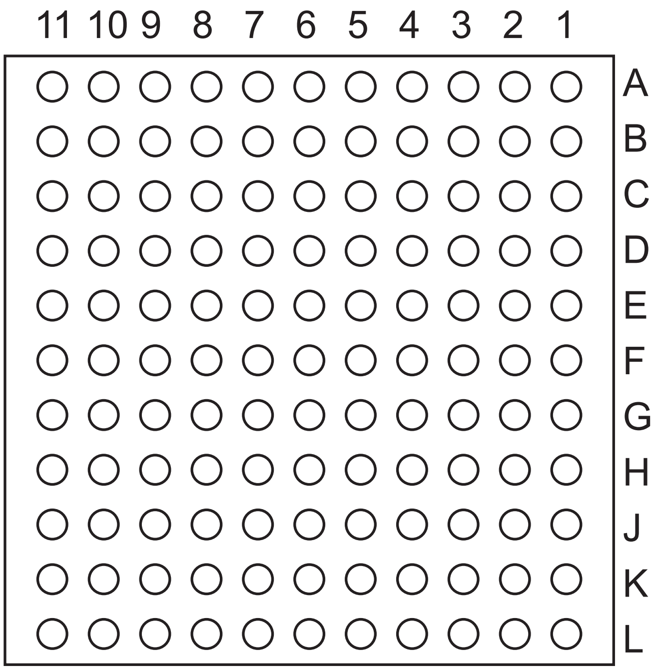


Figure 2-40 • **FIFO EMPTY Flag and AEMPTY Flag Assertion**

CS121 – Bottom View



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG144	
Pin Number	**A3P060 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO04RSB0
A4	GAB1/IO05RSB0
A5	IO08RSB0
A6	GND
A7	IO11RSB0
A8	VCC
A9	IO16RSB0
A10	GBA0/IO23RSB0
A11	GBA1/IO24RSB0
A12	GNDQ
B1	GAB2/IO53RSB1
B2	GND
B3	GAA0/IO02RSB0
B4	GAA1/IO03RSB0
B5	IO00RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO14RSB0
B9	GBB0/IO21RSB0
B10	GBB1/IO22RSB0
B11	GND
B12	VMV0
C1	IO95RSB1
C2	GFA2/IO83RSB1
C3	GAC2/IO94RSB1
C4	VCC
C5	IO01RSB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO17RSB0
C10	GBA2/IO25RSB0
C11	IO26RSB0
C12	GBC2/IO29RSB0
D1	IO91RSB1
D2	IO92RSB1
D3	IO93RSB1
D4	GAA2/IO51RSB1
D5	GAC0/IO06RSB0
D6	GAC1/IO07RSB0
D7	GBC0/IO19RSB0
D8	GBC1/IO20RSB0
D9	GBB2/IO27RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	GCB1/IO37RSB0
E1	VCC
E2	GFC0/IO88RSB1
E3	GFC1/IO89RSB1
E4	VCCIB1
E5	IO52RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO35RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO40RSB0
E12	IO30RSB0
F1	GFB0/IO86RSB1
F2	VCOMPLF
F3	GFB1/IO87RSB1
F4	IO90RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO36RSB0
F9	GCB0/IO38RSB0
F10	GND
F11	GCA1/IO39RSB0
F12	GCA2/IO41RSB0
G1	GFA1/IO84RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO85RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO45RSB0
G9	IO32RSB0
G10	GCC2/IO43RSB0
G11	IO31RSB0
G12	GCB2/IO42RSB0
H1	VCC
H2	GFB2/IO82RSB1
H3	GFC2/IO81RSB1
H4	GEC1/IO77RSB1
H5	VCC
H6	IO34RSB0
H7	IO44RSB0
H8	GDB2/IO55RSB1
H9	GDC0/IO46RSB0
H10	VCCIB0
H11	IO33RSB0
H12	VCC
J1	GEB1/IO75RSB1
J2	IO78RSB1
J3	VCCIB1
J4	GEC0/IO76RSB1
J5	IO79RSB1
J6	IO80RSB1
J7	VCC
J8	TCK
J9	GDA2/IO54RSB1
J10	TDO
J11	GDA1/IO49RSB0
J12	GDB1/IO47RSB0

FG256	
Pin Number	**A3P400 Function**
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1

FG256	
Pin Number	**A3P400 Function**
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3

FG256	
Pin Number	**A3P400 Function**
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2

FG256	
Pin Number	**A3P1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG484	
Pin Number	**A3P400 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO15RSB0
A7	IO18RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO35RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO50RSB0
A17	IO51RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC

FG484	
Pin Number	**A3P400 Function**
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

FG484	
Pin Number	**A3P400 Function**
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND

FG484	
Pin Number	**A3P600 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND

FG484	
Pin Number	A3P1000 Function
R17	GDB1/IO112PPB1
R18	GDC1/IO111PDB1
R19	IO107NDB1
R20	VCC
R21	IO104NDB1
R22	IO105PDB1
T1	IO198PDB3
T2	IO198NDB3
T3	NC
T4	IO194PPB3
T5	IO192PPB3
T6	GEC1/IO190PPB3
T7	IO192NPB3
T8	GNDQ
T9	GEA2/IO187RSB2
T10	IO161RSB2
T11	IO155RSB2
T12	IO141RSB2
T13	IO129RSB2
T14	IO124RSB2
T15	GNDQ
T16	IO110PDB1
T17	VJTAG
T18	GDC0/IO111NDB1
T19	GDA1/IO113PDB1
T20	NC
T21	IO108PDB1
T22	IO105NDB1
U1	IO195PDB3
U2	IO195NDB3
U3	IO194NPB3
U4	GEB1/IO189PDB3
U5	GEB0/IO189NDB3
U6	VMV2
U7	IO179RSB2
U8	IO171RSB2
U9	IO165RSB2
U10	IO159RSB2
U11	IO151RSB2
U12	IO137RSB2
U13	IO134RSB2
U14	IO128RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO113NDB1
U20	NC
U21	IO108NDB1
U22	IO109PDB1
V1	NC
V2	NC
V3	GND
V4	GEA1/IO188PDB3
V5	GEA0/IO188NDB3
V6	IO184RSB2
V7	GEC2/IO185RSB2
V8	IO168RSB2
V9	IO163RSB2
V10	IO157RSB2
V11	IO149RSB2
V12	IO143RSB2
V13	IO138RSB2
V14	IO131RSB2
V15	IO125RSB2
V16	GDB2/IO115RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	IO109NDB1
W1	NC
W2	IO191PDB3
W3	NC
W4	GND
W5	IO183RSB2
W6	GEB2/IO186RSB2
W7	IO172RSB2
W8	IO170RSB2
W9	IO164RSB2
W10	IO158RSB2
W11	IO153RSB2
W12	IO142RSB2
W13	IO135RSB2
W14	IO130RSB2
W15	GDC2/IO116RSB2
W16	IO120RSB2
W17	GDA2/IO114RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO191NDB3
Y3	NC
Y4	IO182RSB2
Y5	GND
Y6	IO177RSB2
Y7	IO174RSB2
Y8	VCC
Y9	VCC
Y10	IO154RSB2
Y11	IO148RSB2
Y12	IO140RSB2
Y13	NC
Y14	VCC

Revision	Changes	Page
Revision 5 (Aug 2008) DC and Switching Characteristics v1.3	TJ, Maximum Junction Temperature, was changed to 100° from 110º in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.	2-6
	Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics.	2-7
	Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new.	2-11, 2-12
	The "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	Both fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 • Input DDR Propagation Delays.	2-78
	Table 2-107 • A3P015 Global Resource is new.	2-86
	The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
Revision 4 (Jun 2008) DC and Switching Characteristics v1.2	Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed.	2-2
	The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power.	2-7
	Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X.	2-27
	Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-66
Revision 3 (Jun 2008) Packaging v1.3	Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram.	4-3
	The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
Revision 2 (Feb 2008) Product Brief v1.0	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Flash Family FPGAs" "A3P015 and A3P030" note Introduction and Overview (NA)	N/A

Revision	**Changes**	**Page**
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3 Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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