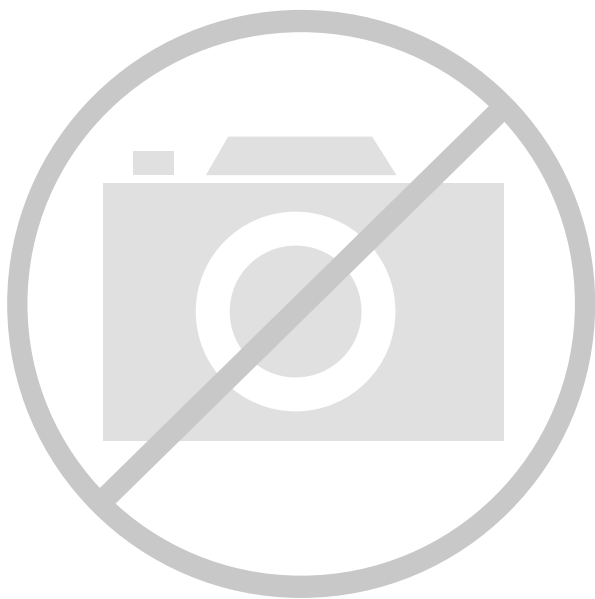




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Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	97
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-2fg144i

I/Os Per Package ¹

ProASIC3 Devices	A3P015 ²	A3P030	A3P060	A3P125	A3P250 ³		A3P400 ³		A3P600		A3P1000	
Cortex-M1 Devices					M1A3P250 ^{3,5}		M1A3P400 ³		M1A3P600		M1A3P1000	
Package	I/O Type											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs
QN48	–	34	–	–	–	–		–	–	–	–	–
QN68	49	49	–	–	–	–	–	–		–	–	–
QN132 ⁷	–	81	80	84	87	19	–	–		–	–	–
CS121	–	–	96	–	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–		–	–	–
TQ144	–	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	–	133	151	34	151	34	154	35	154	35
FG144	–	–	96	97	97	24	97	25	97	25	97	25
FG256 ^{5,6}	–	–	–	–	157	38	178	38	177	43	177	44
FG484 ⁶	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3 FPGA Fabric User Guide](#) to ensure complying with design and board migration requirements.
2. A3P015 is not recommended for new designs.
3. For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the [ProASIC3 FPGA Fabric Users Guide](#) for position assignments of the 15 LVPECL pairs.
4. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
5. The M1A3P250 device does not support FG256 package.
6. FG256 and FG484 are footprint-compatible packages.
7. Package not available.

Table 1 • ProASIC3 FPGAs Package Sizes Dimensions

Package	CS121	QN48	QN68	QN132 *	VQ100	TQ144	PQ208	FG144	FG256	FG484
Length × Width (mm × mm)	6 × 6	6 × 6	8 × 8	8 × 8	14 × 14	20 × 20	28 × 28	13 × 13	17 × 17	23 × 23
Nominal Area (mm ²)	36	36	64	64	196	400	784	169	289	529
Pitch (mm)	0.5	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	1.0
Height (mm)	0.99	0.90	0.90	0.75	1.00	1.40	3.40	1.45	1.60	2.23

Note: * Package not available

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 300 μs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4 on page 2-3](#).
2. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on [page 3-1](#) for further information.
3. For flash programming and retention maximum limits, refer to [Table 2-3 on page 2-3](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).

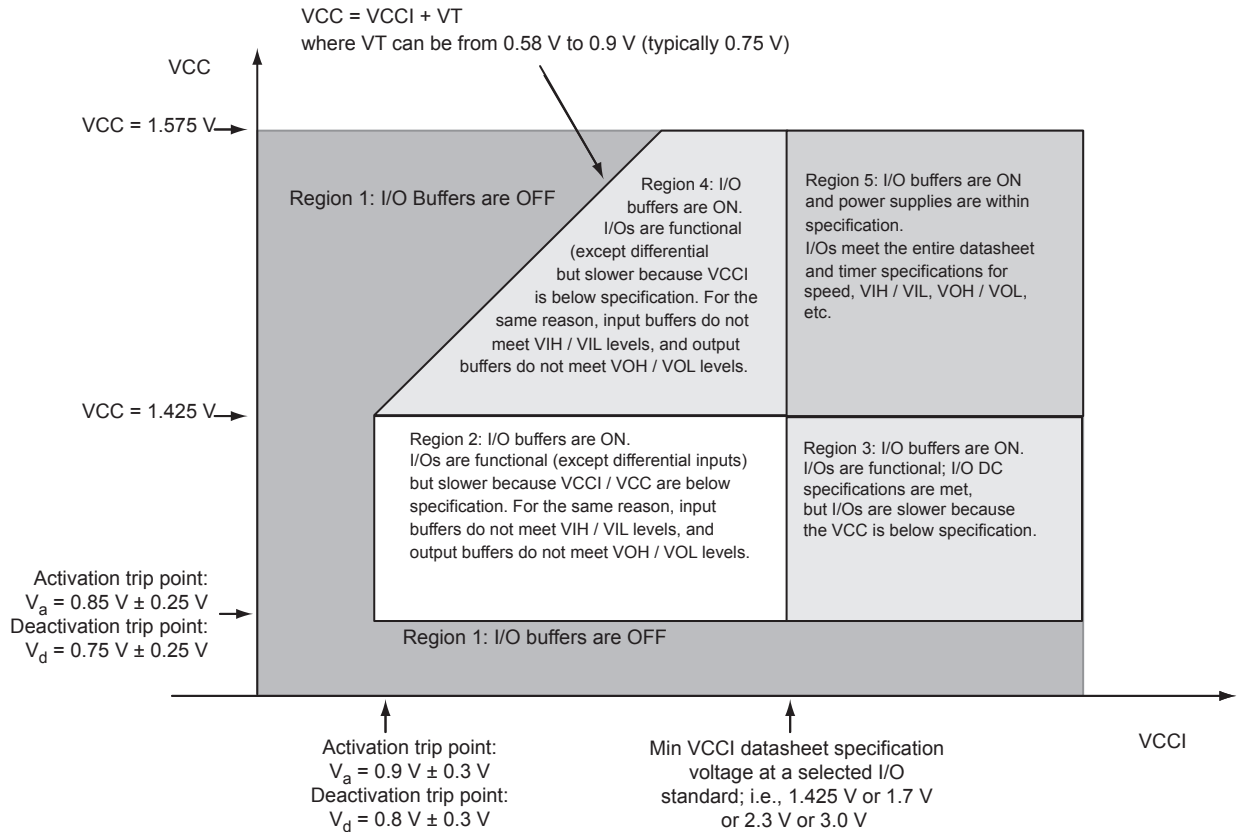


Figure 2-2 • I/O State as a Function of VCCI and VCC Voltage Levels

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates.

User I/O Characteristics

Timing Model

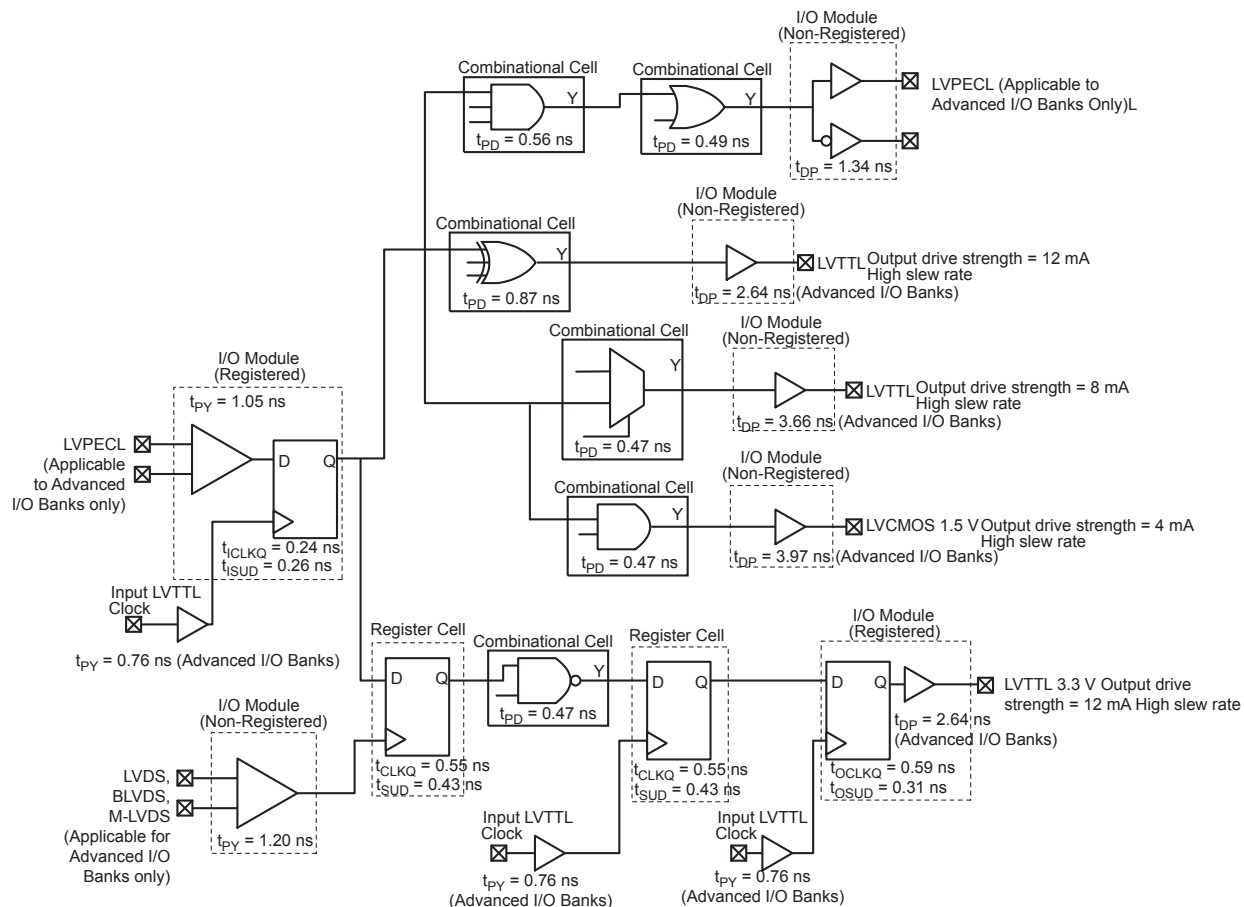


Figure 2-3 • Timing Model

Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J = 70^\circ\text{C}$), Worst Case $V_{CC} = 1.425$ V

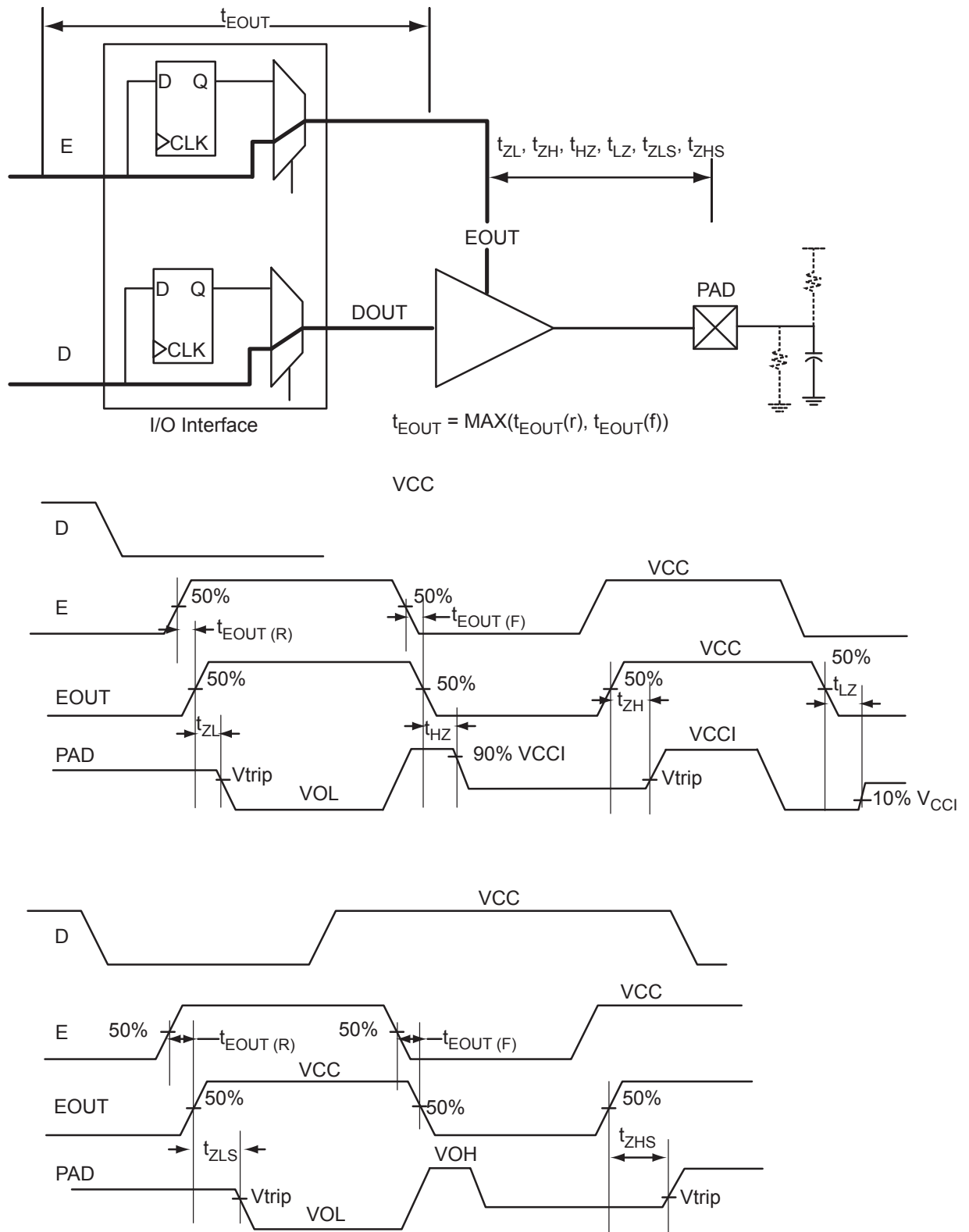


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (Example)

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case V_{CCI} (per standard)
 Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	35	–	0.45	4.08	0.03	0.76	0.32	4.08	3.20	3.71	4.14	6.61	5.74	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ⁴	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁴	0.45	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	–	High	–	–	0.45	1.37	0.03	1.20	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.45	1.34	0.03	1.05	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-64](#) for connectivity. This resistor is not required during normal operation.

Table 2-44 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$** **Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
4 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
6 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
8 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
12 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns
16 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.**Table 2-45 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew****Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$** **Applicable to Standard I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
4 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
6 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	–2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
8 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns

Table 2-72 • 1.8 V LVC MOS High Slew**Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.7\text{ V}$** **Applicable to Standard Plus I/O Banks**

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.33	0.04	1.20	0.43	8.72	11.33	2.24	1.52	10.96	13.57	ns
	–1	0.56	9.64	0.04	1.02	0.36	7.42	9.64	1.91	1.29	9.32	11.54	ns
	–2	0.49	8.46	0.03	0.90	0.32	6.51	8.46	1.68	1.14	8.18	10.13	ns
4 mA	Std.	0.66	6.48	0.04	1.20	0.43	5.48	6.48	2.65	2.60	7.72	8.72	ns
	–1	0.56	5.51	0.04	1.02	0.36	4.66	5.51	2.25	2.21	6.56	7.42	ns
	–2	0.49	4.84	0.03	0.90	0.32	4.09	4.84	1.98	1.94	5.76	6.51	ns
6 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns
8 mA	Std.	0.66	4.06	0.04	1.20	0.43	3.84	4.06	2.93	3.10	6.07	6.30	ns
	–1	0.56	3.45	0.04	1.02	0.36	3.27	3.45	2.49	2.64	5.17	5.36	ns
	–2	0.49	3.03	0.03	0.90	0.32	2.87	3.03	2.19	2.32	4.54	4.70	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-86 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max., V	Min. V	mA	mA	Max. mA ¹	Max. mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 85°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in [Figure 2-11](#).

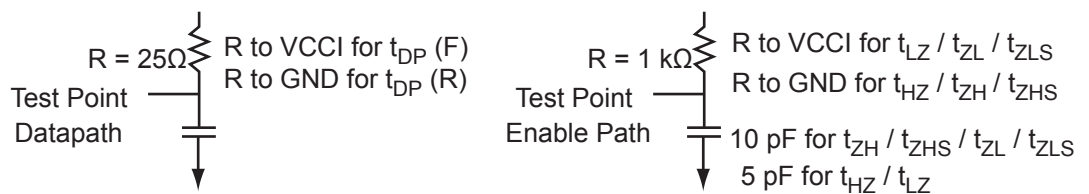


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in [Table 2-87](#).

Table 2-87 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	0.285 * V _{CCI} for $t_{DP(R)}$ 0.615 * V _{CCI} for $t_{DP(F)}$	10

Note: *Measuring point = V_{trip} . See [Table 2-22 on page 2-22](#) for a complete table of trip points.

Timing Characteristics

Table 2-88 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.68	0.04	0.86	0.43	2.73	1.95	3.21	3.58	4.97	4.19	ns
–1	0.56	2.28	0.04	0.73	0.36	2.32	1.66	2.73	3.05	4.22	3.56	ns
–2	0.49	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-89 • 3.3 V PCI/PCI-X

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
 Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.66	2.31	0.04	0.85	0.43	2.35	1.70	2.79	3.22	4.59	3.94	ns
–1	0.56	1.96	0.04	0.72	0.36	2.00	1.45	2.37	2.74	3.90	3.35	ns
–2	0.49	1.72	0.03	0.64	0.32	1.76	1.27	2.08	2.41	3.42	2.94	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in [Figure 2-12](#). The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

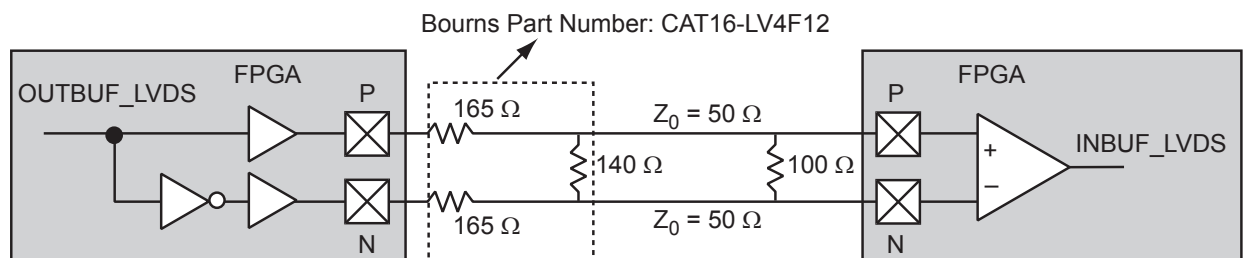


Figure 2-12 • LVDS Circuit Diagram and Board-Level Implementation

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

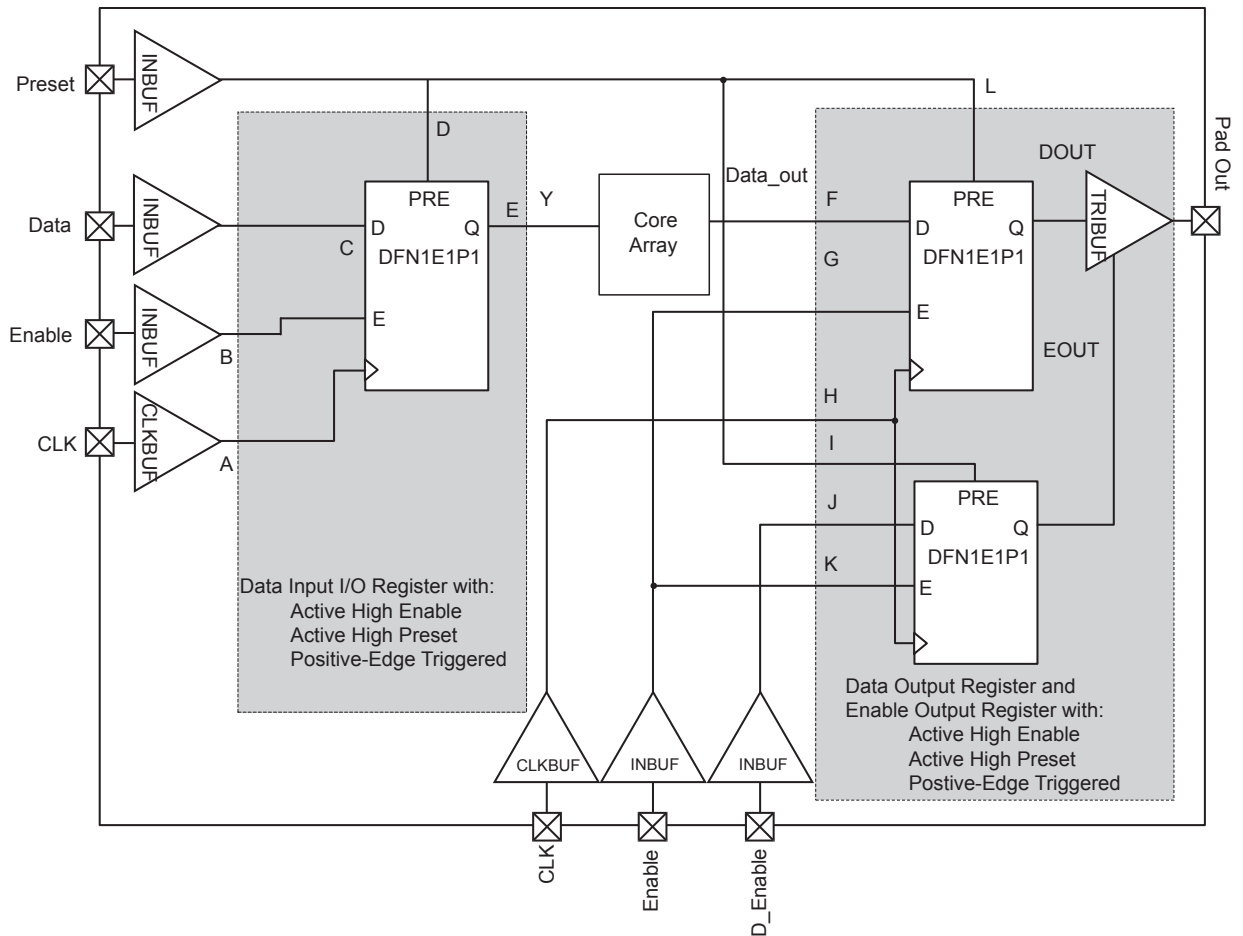


Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-111 • A3P250 Global Resource
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.80	1.01	0.91	1.15	1.07	1.36	ns
t_{RCKH}	Input High Delay for Global Clock	0.78	1.04	0.89	1.18	1.04	1.39	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-112 • A3P400 Global Resource
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t_{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Waveforms

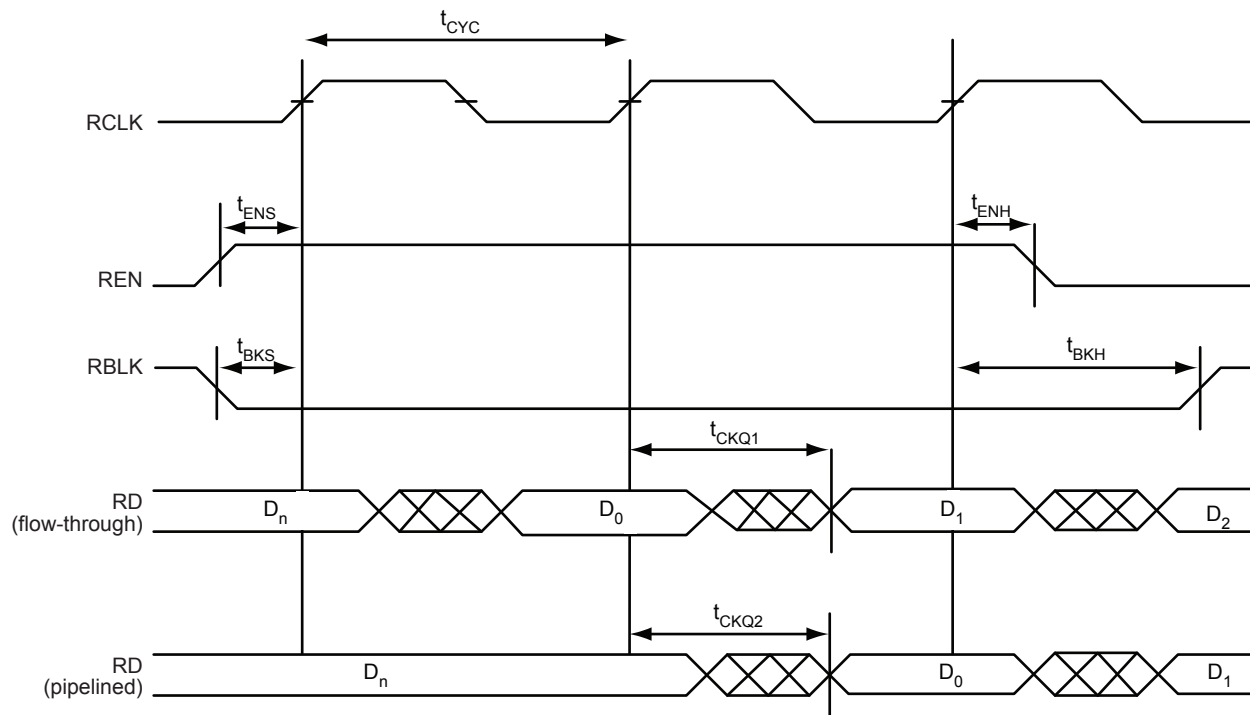


Figure 2-37 • FIFO Read

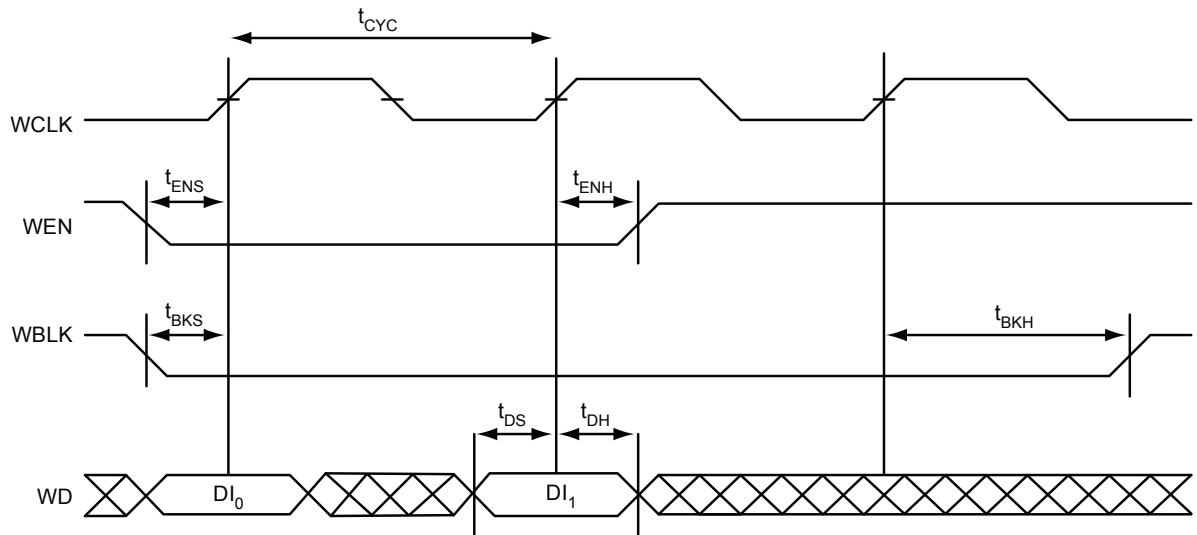


Figure 2-38 • FIFO Write

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-15 for more details.

Timing Characteristics

Table 2-125 • JTAG 1532

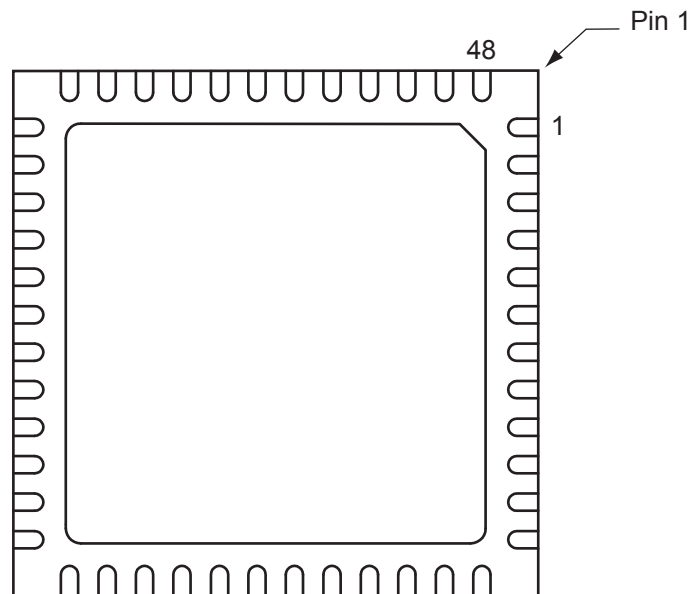
Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.50	0.57	0.67	ns
t_{DIHD}	Test Data Input Hold Time	1.00	1.13	1.33	ns
t_{TMSSU}	Test Mode Select Setup Time	0.50	0.57	0.67	ns
t_{TMDHD}	Test Mode Select Hold Time	1.00	1.13	1.33	ns
t_{TCK2Q}	Clock to Q (data out)	6.00	6.80	8.00	ns
t_{RSTB2Q}	Reset to Q (data out)	20.00	22.67	26.67	ns
F_{TCKMAX}	TCK Maximum Frequency	25.00	22.00	19.00	MHz
t_{TRSTREM}	ResetB Removal Time	0.00	0.00	0.00	ns
t_{TRSTREC}	ResetB Recovery Time	0.20	0.23	0.27	ns
t_{TRSTMPW}	ResetB Minimum Pulse	TBD	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

4 – Package Pin Assignments

QN48 – Bottom View



Note: The die attach paddle center of the package is tied to ground (GND).

Note

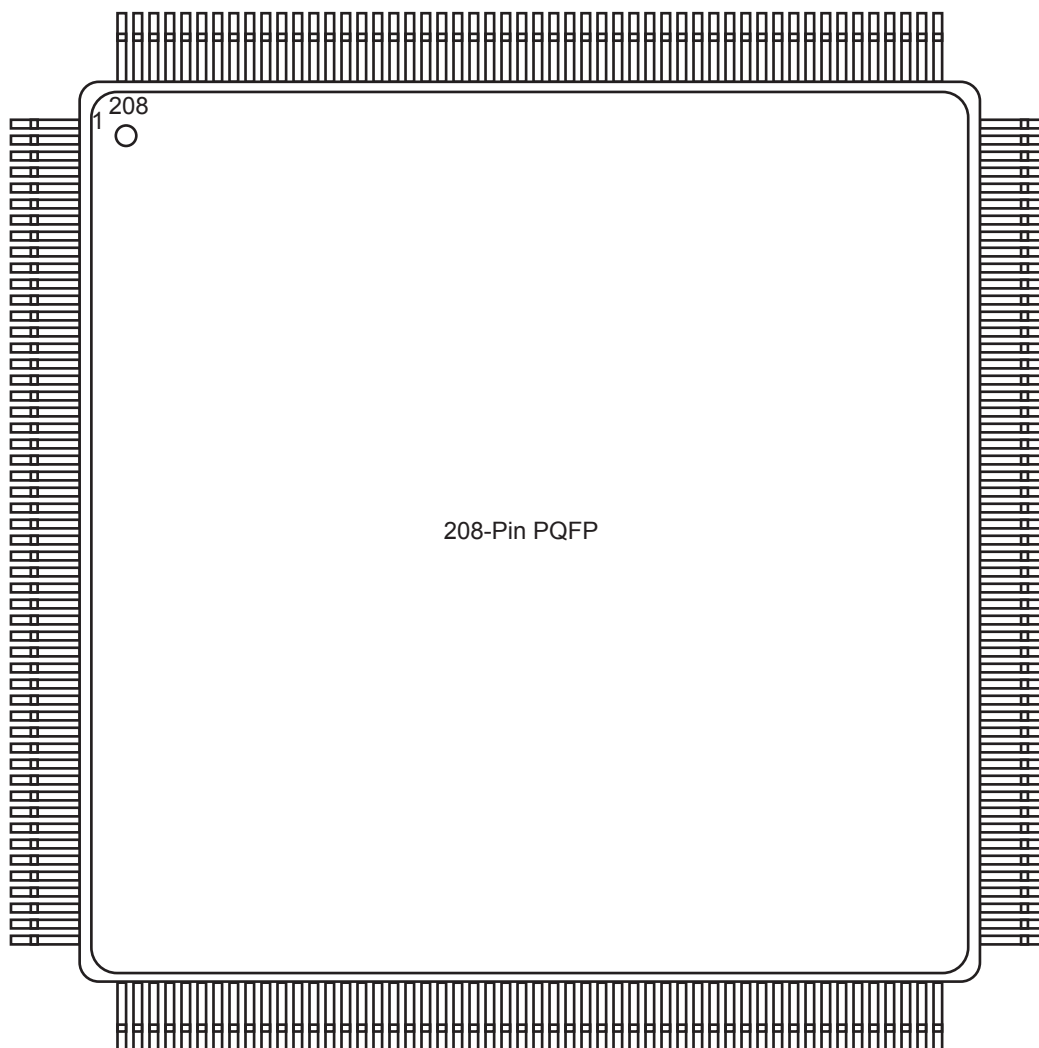
For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

QN132	
Pin Number	A3P030 Function
A1	IO01RSB1
A2	IO81RSB1
A3	NC
A4	IO80RSB1
A5	GEC0/IO77RSB1
A6	NC
A7	GEB0/IO75RSB1
A8	IO73RSB1
A9	NC
A10	VCC
A11	IO71RSB1
A12	IO68RSB1
A13	IO63RSB1
A14	IO60RSB1
A15	NC
A16	IO59RSB1
A17	IO57RSB1
A18	VCC
A19	IO54RSB1
A20	IO52RSB1
A21	IO49RSB1
A22	IO48RSB1
A23	IO47RSB1
A24	TDI
A25	TRST
A26	IO44RSB0
A27	NC
A28	IO43RSB0
A29	IO42RSB0
A30	IO40RSB0
A31	IO39RSB0
A32	GDC0/IO36RSB0
A33	NC
A34	VCC
A35	IO34RSB0
A36	IO31RSB0

QN132	
Pin Number	A3P030 Function
A37	IO26RSB0
A38	IO23RSB0
A39	NC
A40	IO22RSB0
A41	IO20RSB0
A42	IO18RSB0
A43	VCC
A44	IO15RSB0
A45	IO12RSB0
A46	IO10RSB0
A47	IO09RSB0
A48	IO06RSB0
B1	IO02RSB1
B2	IO82RSB1
B3	GND
B4	IO79RSB1
B5	NC
B6	GND
B7	IO74RSB1
B8	NC
B9	GND
B10	IO70RSB1
B11	IO67RSB1
B12	IO64RSB1
B13	IO61RSB1
B14	GND
B15	IO58RSB1
B16	IO56RSB1
B17	GND
B18	IO53RSB1
B19	IO50RSB1
B20	GND
B21	IO46RSB1
B22	TMS
B23	TDO
B24	IO45RSB0

QN132	
Pin Number	A3P030 Function
B25	GND
B26	NC
B27	IO41RSB0
B28	GND
B29	GDA0/IO37RSB0
B30	NC
B31	GND
B32	IO33RSB0
B33	IO30RSB0
B34	IO27RSB0
B35	IO24RSB0
B36	GND
B37	IO21RSB0
B38	IO19RSB0
B39	GND
B40	IO16RSB0
B41	IO13RSB0
B42	GND
B43	IO08RSB0
B44	IO05RSB0
C1	IO03RSB1
C2	IO00RSB1
C3	NC
C4	IO78RSB1
C5	GEA0/IO76RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO69RSB1
C10	IO66RSB1
C11	IO65RSB1
C12	IO62RSB1
C13	NC
C14	NC
C15	IO55RSB1
C16	VCCIB1

PQ208 – Top View



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

FG256	
Pin Number	A3P250 Function
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

FG256	
Pin Number	A3P250 Function
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

FG256	
Pin Number	A3P400 Function
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2

FG256	
Pin Number	A3P400 Function
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND