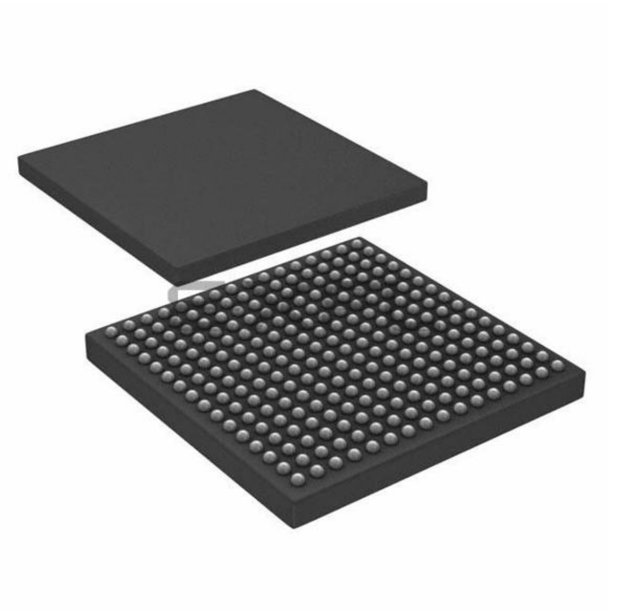

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 36864 |
| Number of I/O | 157 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p250-2fg256 |

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings**
**–2 Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst Case VCC = 1.425 V,**
**Worst-Case VCCI (per standard)**
**Standard I/O Banks**

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 8 mA | 8 mA | High | 35 | – | 0.45 | 3.29 | 0.03 | 0.75 | 0.32 | 3.36 | 2.80 | 1.79 | 2.01 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 8 mA | High | 35 | – | 0.45 | 5.09 | 0.03 | 1.13 | 0.32 | 5.09 | 4.25 | 2.77 | 3.11 | ns |
| 2.5 V LVCMOS | 8 mA | 8 mA | High | 35 | – | 0.45 | 3.56 | 0.03 | 0.96 | 0.32 | 3.40 | 3.56 | 1.78 | 1.91 | ns |
| 1.8 V LVCMOS | 4 mA | 4 mA | High | 35 | – | 0.45 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |
| 1.5 V LVCMOS | 2 mA | 2 mA | High | 35 | – | 0.45 | 5.71 | 0.03 | 1.06 | 0.32 | 4.71 | 5.71 | 1.83 | 1.83 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-30 • I/O Output Buffer Maximum Resistances[1]
Applicable to Standard I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ (Ω)[2] | $R_{PULL\text{-}UP}$ (Ω)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 3.3 V LVCMOS Wide Range[4] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

**Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | $R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω) | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 3.3 V (wide range I/Os) | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCI_{MAX} - VOH_{spec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOL_{spec}) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

**Table 2-34 • I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks**

| | Drive Strength | IOSL (mA)[1] | IOSH (mA)[1] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |

*Notes:*

1. *$T_J$ = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. $I_{OSL}/I_{OSH}$ dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

**Table 2-35 • Duration of Short Circuit Event Before Failure**

| Temperature | Time before Failure |
|---|---|
| –40°C | > 20 years |
| 0°C | > 20 years |
| 25°C | > 20 years |
| 70°C | 5 years |
| 85°C | 2 years |
| 100°C | 0.5 years |

**Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability**

| Input Buffer | Input Rise/Fall Time (min) | Input Rise/Fall Time (max) | Reliability |
|---|---|---|---|
| LVTTL/LVCMOS | No requirement | 10 ns * | 20 years (110°C) |
| LVDS/B-LVDS/ M-LVDS/LVPECL | No requirement | 10 ns * | 10 years (100°C) |

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

*Table 2-42 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-51 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 15.86 | 0.04 | 1.54 | 0.43 | 15.86 | 13.51 | 4.09 | 3.80 | 19.25 | 16.90 | ns |
| | | –1 | 0.51 | 13.49 | 0.04 | 1.31 | 0.36 | 13.49 | 11.49 | 3.48 | 3.23 | 16.38 | 14.38 | ns |
| | | –2 | 0.45 | 11.84 | 0.03 | 1.15 | 0.32 | 11.84 | 10.09 | 3.05 | 2.84 | 14.38 | 12.62 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 11.25 | 0.04 | 1.54 | 0.43 | 11.25 | 9.54 | 4.61 | 4.70 | 14.64 | 12.93 | ns |
| | | –1 | 0.51 | 9.57 | 0.04 | 1.31 | 0.36 | 9.57 | 8.11 | 3.92 | 4.00 | 12.46 | 11.00 | ns |
| | | –2 | 0.45 | 8.40 | 0.03 | 1.15 | 0.32 | 8.40 | 7.12 | 3.44 | 3.51 | 10.93 | 9.66 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 11.25 | 0.04 | 1.54 | 0.43 | 11.25 | 9.54 | 4.61 | 4.70 | 14.64 | 12.93 | ns |
| | | –1 | 0.51 | 9.57 | 0.04 | 1.31 | 0.36 | 9.57 | 8.11 | 3.92 | 4.00 | 12.46 | 11.00 | ns |
| | | –2 | 0.45 | 8.40 | 0.03 | 1.15 | 0.32 | 8.40 | 7.12 | 3.44 | 3.51 | 10.93 | 9.66 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 8.63 | 0.04 | 1.54 | 0.43 | 8.63 | 7.39 | 4.96 | 5.28 | 12.02 | 10.79 | ns |
| | | –1 | 0.51 | 7.34 | 0.04 | 1.31 | 0.36 | 7.34 | 6.29 | 4.22 | 4.49 | 10.23 | 9.18 | ns |
| | | –2 | 0.45 | 6.44 | 0.03 | 1.15 | 0.32 | 6.44 | 5.52 | 3.70 | 3.94 | 8.98 | 8.06 | ns |
| 100 µA | 16 mA | Std. | 0.60 | 8.05 | 0.04 | 1.54 | 0.43 | 8.05 | 6.93 | 5.03 | 5.43 | 11.44 | 10.32 | ns |
| | | –1 | 0.51 | 6.85 | 0.04 | 1.31 | 0.36 | 6.85 | 5.90 | 4.28 | 4.62 | 9.74 | 8.78 | ns |
| | | –2 | 0.45 | 6.01 | 0.03 | 1.15 | 0.32 | 6.01 | 5.18 | 3.76 | 4.06 | 8.55 | 7.71 | ns |
| 100 µA | 24 mA | Std. | 0.60 | 7.50 | 0.04 | 1.54 | 0.43 | 7.50 | 6.90 | 5.13 | 6.00 | 10.89 | 10.29 | ns |
| | | –1 | 0.51 | 6.38 | 0.04 | 1.31 | 0.36 | 6.38 | 5.87 | 4.36 | 5.11 | 9.27 | 8.76 | ns |
| | | –2 | 0.45 | 5.60 | 0.03 | 1.15 | 0.32 | 5.60 | 5.15 | 3.83 | 4.48 | 8.13 | 7.69 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## 1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

***Table 2-66 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA[3] | Max mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 8 | 8 | 51 | 45 | 10 | 10 |
| 12 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 | 74 | 91 | 10 | 10 |
| 16 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 16 | 16 | 74 | 91 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

***Table 2-67 •*** **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

| 1.8 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[1] | IIH[2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA[3] | Max mA[3] | µA[4] | µA[4] |
| 2 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 2 | 2 | 11 | 9 | 10 | 10 |
| 4 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 4 | 4 | 22 | 17 | 10 | 10 |
| 6 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 6 | 6 | 44 | 35 | 10 | 10 |
| 8 mA | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 3.6 | 0.45 | VCCI – 0.45 | 8 | 8 | 44 | 35 | 10 | 10 |

*Notes:*

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

### Timing Characteristics

**Table 2-70 • 1.8 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 11.86 | 0.04 | 1.22 | 0.43 | 9.14 | 11.86 | 2.77 | 1.66 | 11.37 | 14.10 | ns |
| | –1 | 0.56 | 10.09 | 0.04 | 1.04 | 0.36 | 7.77 | 10.09 | 2.36 | 1.41 | 9.67 | 11.99 | ns |
| | –2 | 0.49 | 8.86 | 0.03 | 0.91 | 0.32 | 6.82 | 8.86 | 2.07 | 1.24 | 8.49 | 10.53 | ns |
| 4 mA | Std. | 0.66 | 6.91 | 0.04 | 1.22 | 0.43 | 5.86 | 6.91 | 3.22 | 2.84 | 8.10 | 9.15 | ns |
| | –1 | 0.56 | 5.88 | 0.04 | 1.04 | 0.36 | 4.99 | 5.88 | 2.74 | 2.41 | 6.89 | 7.78 | ns |
| | –2 | 0.49 | 5.16 | 0.03 | 0.91 | 0.32 | 4.38 | 5.16 | 2.41 | 2.12 | 6.05 | 6.83 | ns |
| 6 mA | Std. | 0.66 | 4.45 | 0.04 | 1.22 | 0.43 | 4.18 | 4.45 | 3.53 | 3.38 | 6.42 | 6.68 | ns |
| | –1 | 0.56 | 3.78 | 0.04 | 1.04 | 0.36 | 3.56 | 3.78 | 3.00 | 2.88 | 5.46 | 5.69 | ns |
| | –2 | 0.49 | 3.32 | 0.03 | 0.91 | 0.32 | 3.12 | 3.32 | 2.64 | 2.53 | 4.79 | 4.99 | ns |
| 8 mA | Std. | 0.66 | 3.92 | 0.04 | 1.22 | 0.43 | 3.93 | 3.92 | 3.60 | 3.52 | 6.16 | 6.16 | ns |
| | –1 | 0.56 | 3.34 | 0.04 | 1.04 | 0.36 | 3.34 | 3.34 | 3.06 | 3.00 | 5.24 | 5.24 | ns |
| | –2 | 0.49 | 2.93 | 0.03 | 0.91 | 0.32 | 2.93 | 2.93 | 2.69 | 2.63 | 4.60 | 4.60 | ns |
| 12 mA | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | –1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | –2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 16 mA | Std. | 0.66 | 3.53 | 0.04 | 1.22 | 0.43 | 3.60 | 3.04 | 3.70 | 4.08 | 5.84 | 5.28 | ns |
| | –1 | 0.56 | 3.01 | 0.04 | 1.04 | 0.36 | 3.06 | 2.59 | 3.15 | 3.47 | 4.96 | 4.49 | ns |
| | –2 | 0.49 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

### Timing Characteristics

*Table 2-88* • **3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | ns |
| –1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | ns |
| –2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-89* • **3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.31 | 0.04 | 0.85 | 0.43 | 2.35 | 1.70 | 2.79 | 3.22 | 4.59 | 3.94 | ns |
| –1 | 0.56 | 1.96 | 0.04 | 0.72 | 0.36 | 2.00 | 1.45 | 2.37 | 2.74 | 3.90 | 3.35 | ns |
| –2 | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Differential I/O Characteristics

### *Physical Implementation*

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### *LVDS*

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

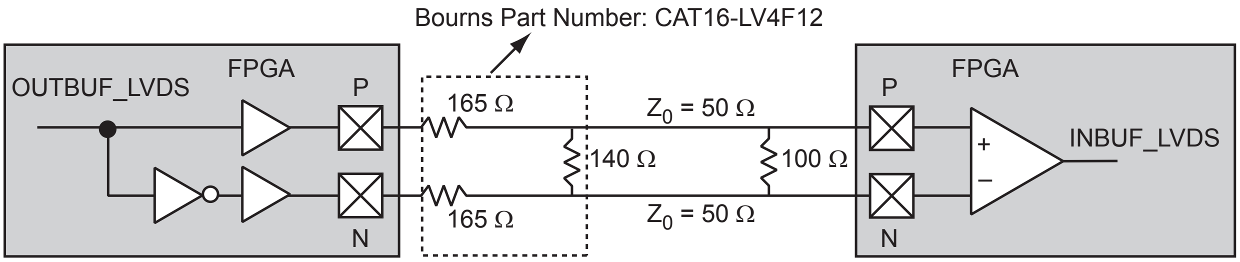

*Figure 2-12* • **LVDS Circuit Diagram and Board-Level Implementation**

# I/O Register Specifications

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

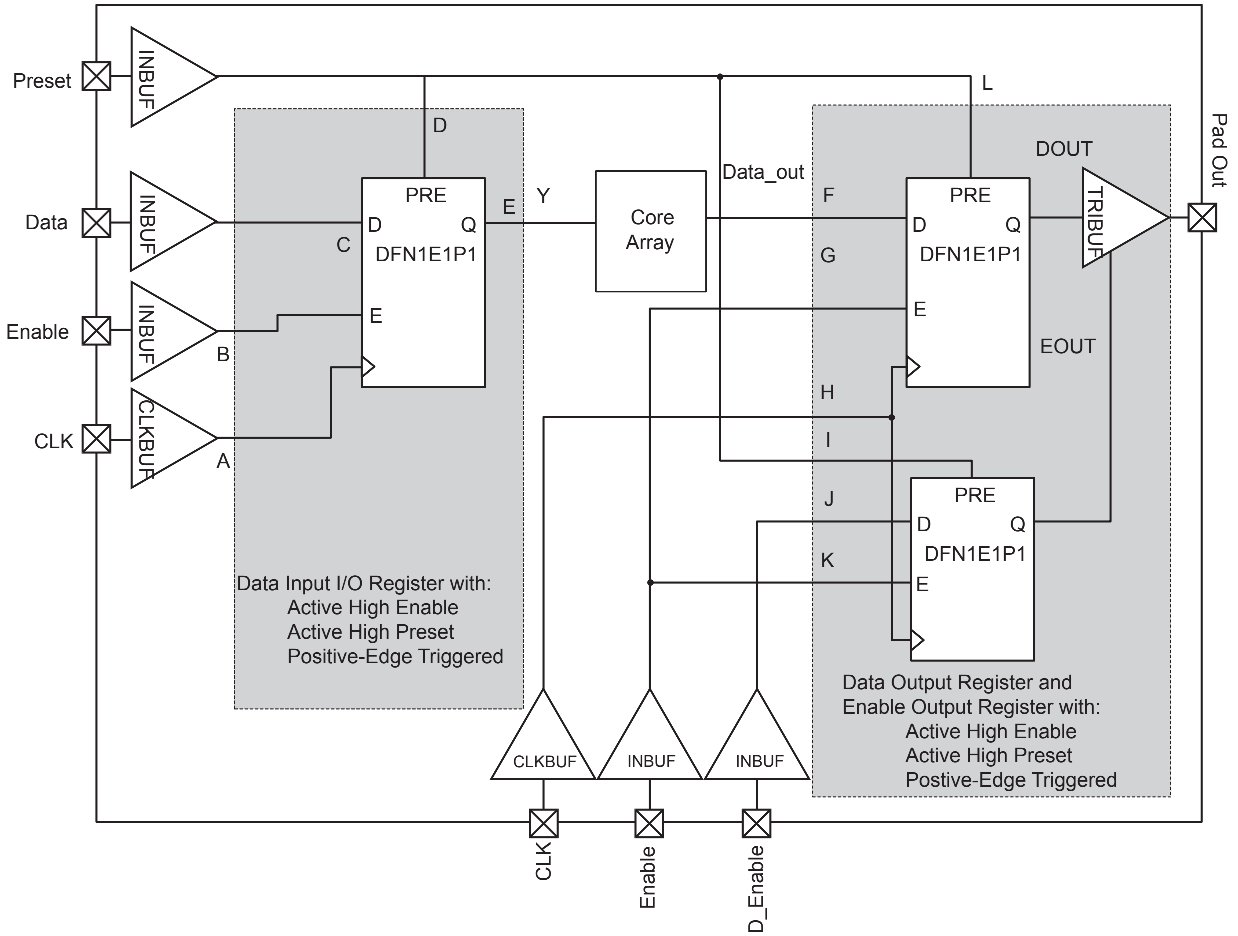

*Figure 2-15* • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

# VersaTile Characteristics

## VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.

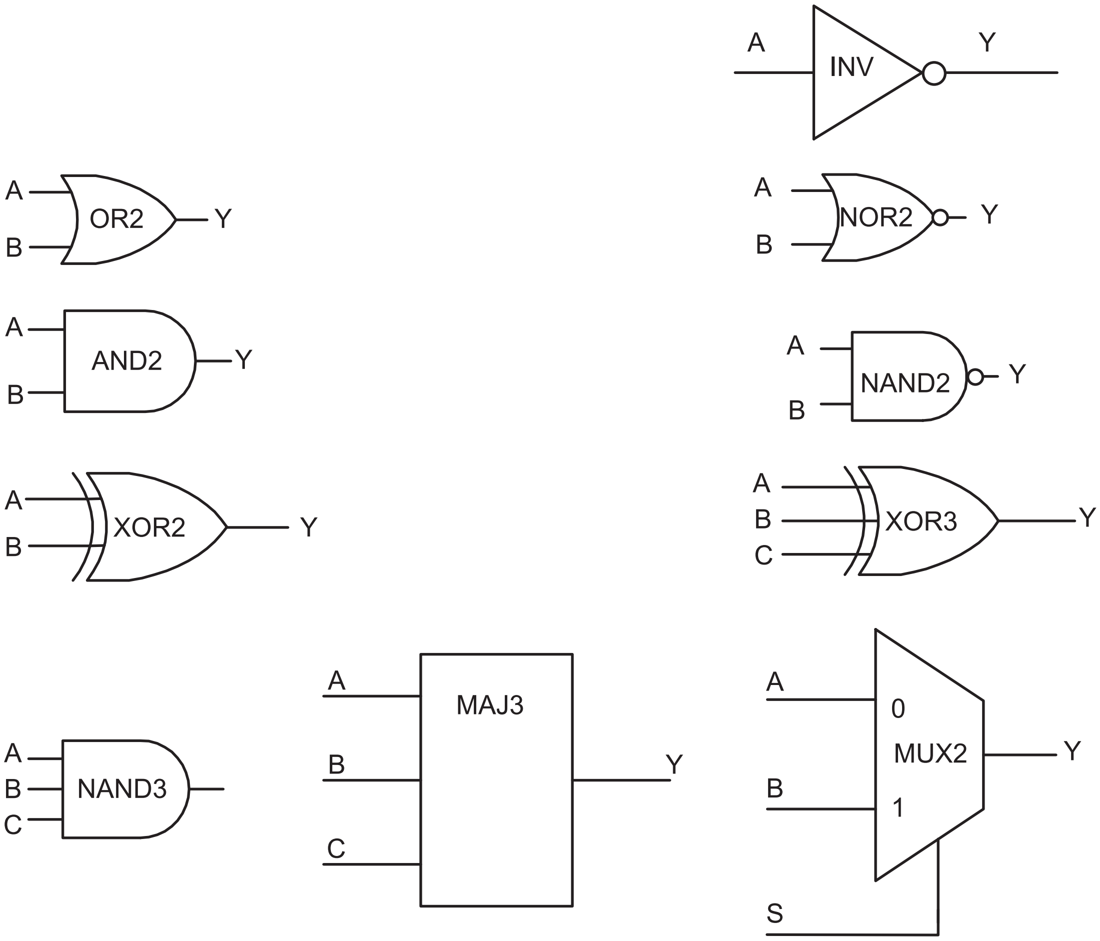

***Figure 2-24 •*** **Sample of Combinatorial Cells**

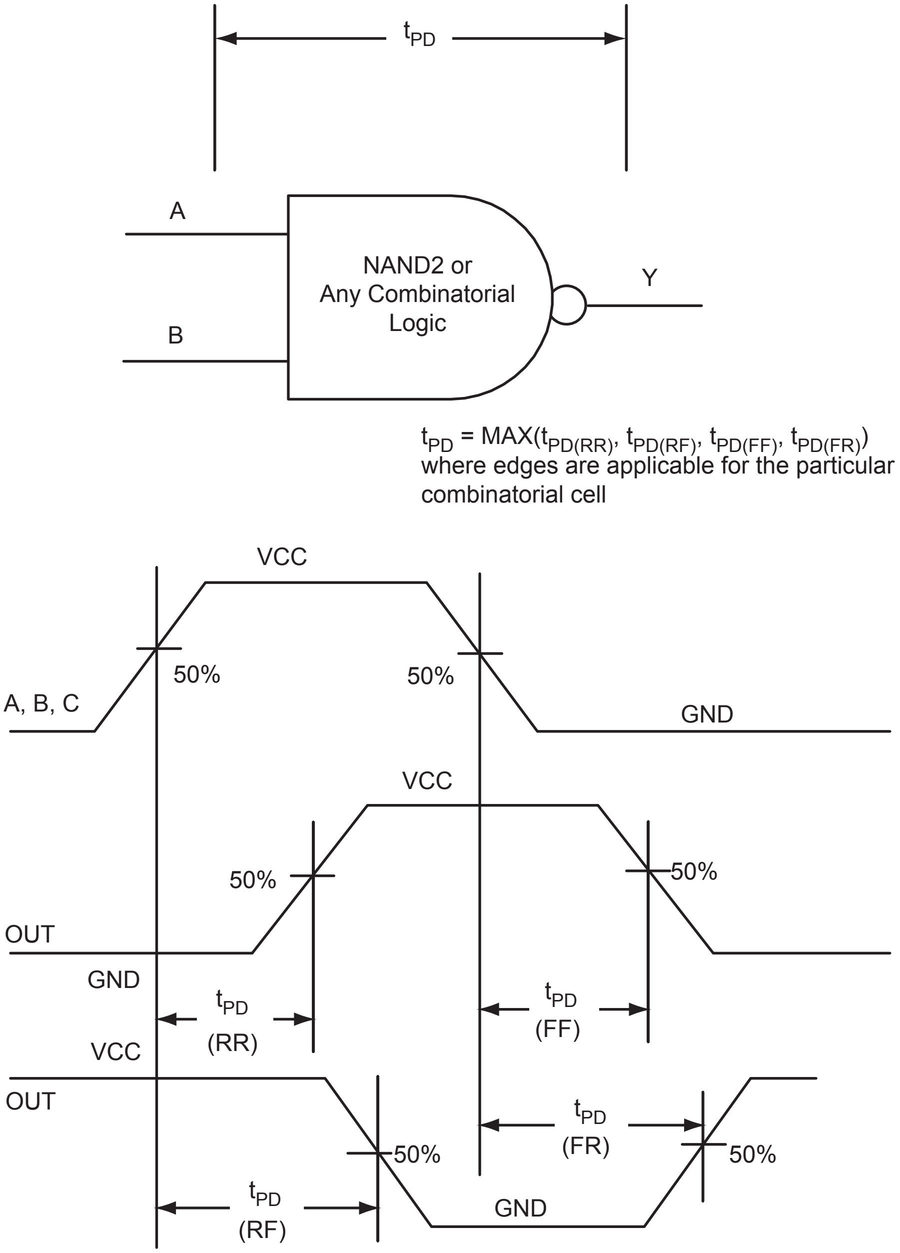

*Figure 2-25* • **Timing Model and Waveforms**

## Timing Waveforms

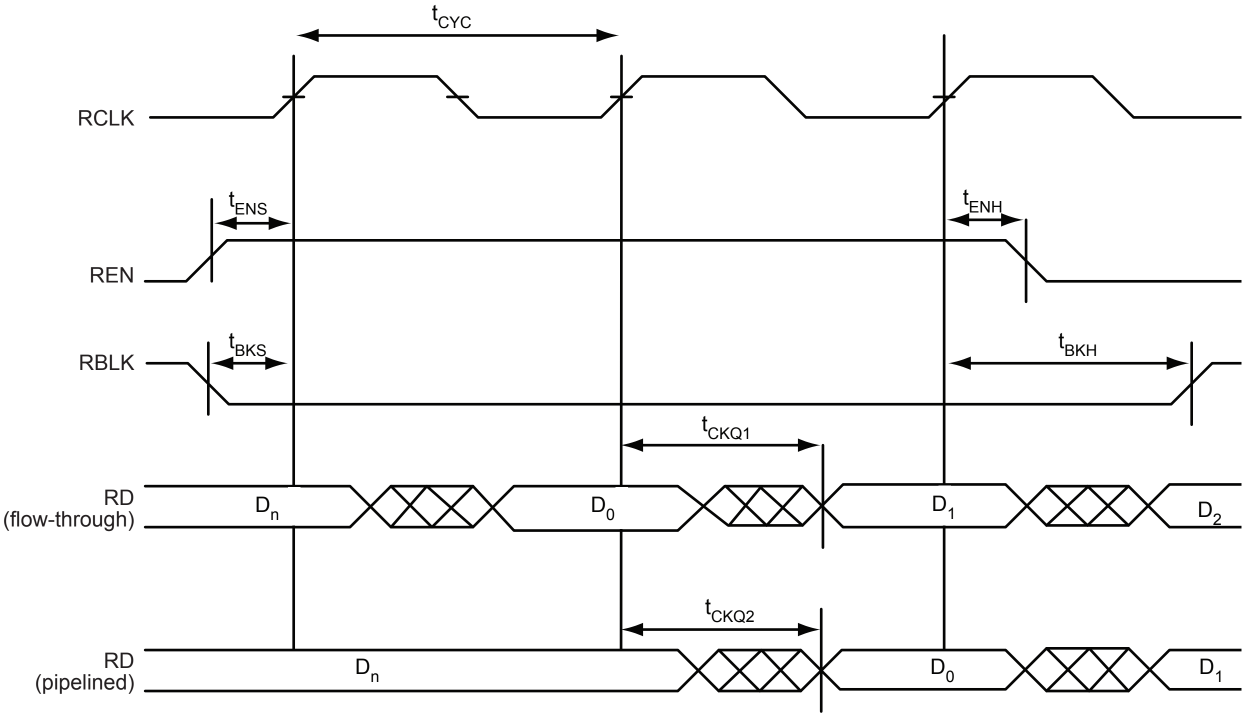

***Figure 2-37 •*** **FIFO Read**

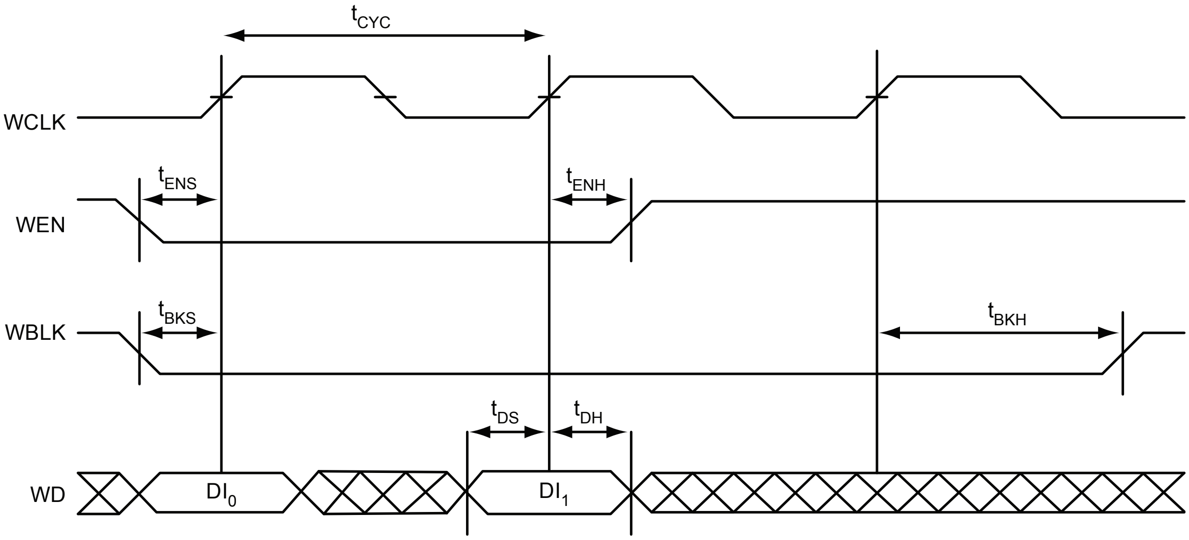

***Figure 2-38 •*** **FIFO Write**

| QN68 | |
|---|---|
| **Pin Number** | **A3P030 Function** |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |
| 36 | TDO |

| QN68 | |
|---|---|
| **Pin Number** | **A3P030 Function** |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | VCCIB0 |
| 60 | GND |
| 61 | VCC |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

| VQ100 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| 1 | GND |
| 2 | GAA2/IO118UDB3 |
| 3 | IO118VDB3 |
| 4 | GAB2/IO117UDB3 |
| 5 | IO117VDB3 |
| 6 | GAC2/IO116UDB3 |
| 7 | IO116VDB3 |
| 8 | IO112PSB3 |
| 9 | GND |
| 10 | GFB1/IO109PDB3 |
| 11 | GFB0/IO109NDB3 |
| 12 | VCOMPLF |
| 13 | GFA0/IO108NPB3 |
| 14 | VCCPLF |
| 15 | GFA1/IO108PPB3 |
| 16 | GFA2/IO107PSB3 |
| 17 | VCC |
| 18 | VCCIB3 |
| 19 | GFC2/IO105PSB3 |
| 20 | GEC1/IO100PDB3 |
| 21 | GEC0/IO100NDB3 |
| 22 | GEA1/IO98PDB3 |
| 23 | GEA0/IO98NDB3 |
| 24 | VMV3 |
| 25 | GNDQ |
| 26 | GEA2/IO97RSB2 |
| 27 | GEB2/IO96RSB2 |
| 28 | GEC2/IO95RSB2 |
| 29 | IO93RSB2 |
| 30 | IO92RSB2 |
| 31 | IO91RSB2 |
| 32 | IO90RSB2 |
| 33 | IO88RSB2 |
| 34 | IO86RSB2 |
| 35 | IO85RSB2 |
| 36 | IO84RSB2 |
| 37 | VCC |
| 38 | GND |
| 39 | VCCIB2 |
| 40 | IO77RSB2 |
| 41 | IO74RSB2 |
| 42 | IO71RSB2 |
| 43 | GDC2/IO63RSB2 |
| 44 | GDB2/IO62RSB2 |
| 45 | GDA2/IO61RSB2 |
| 46 | GNDQ |
| 47 | TCK |
| 48 | TDI |
| 49 | TMS |
| 50 | VMV2 |
| 51 | GND |
| 52 | VPUMP |
| 53 | NC |
| 54 | TDO |
| 55 | TRST |
| 56 | VJTAG |
| 57 | GDA1/IO60USB1 |
| 58 | GDC0/IO58VDB1 |
| 59 | GDC1/IO58UDB1 |
| 60 | IO52NDB1 |
| 61 | GCB2/IO52PDB1 |
| 62 | GCA1/IO50PDB1 |
| 63 | GCA0/IO50NDB1 |
| 64 | GCC0/IO48NDB1 |
| 65 | GCC1/IO48PDB1 |
| 66 | VCCIB1 |
| 67 | GND |
| 68 | VCC |
| 69 | IO43NDB1 |
| 70 | GBC2/IO43PDB1 |
| 71 | GBB2/IO42PSB1 |
| 72 | IO41NDB1 |
| 73 | GBA2/IO41PDB1 |
| 74 | VMV1 |
| 75 | GNDQ |
| 76 | GBA1/IO40RSB0 |
| 77 | GBA0/IO39RSB0 |
| 78 | GBB1/IO38RSB0 |
| 79 | GBB0/IO37RSB0 |
| 80 | GBC1/IO36RSB0 |
| 81 | GBC0/IO35RSB0 |
| 82 | IO29RSB0 |
| 83 | IO27RSB0 |
| 84 | IO25RSB0 |
| 85 | IO23RSB0 |
| 86 | IO21RSB0 |
| 87 | VCCIB0 |
| 88 | GND |
| 89 | VCC |
| 90 | IO15RSB0 |
| 91 | IO13RSB0 |
| 92 | IO11RSB0 |
| 93 | GAC1/IO05RSB0 |
| 94 | GAC0/IO04RSB0 |
| 95 | GAB1/IO03RSB0 |
| 96 | GAB0/IO02RSB0 |
| 97 | GAA1/IO01RSB0 |
| 98 | GAA0/IO00RSB0 |
| 99 | GNDQ |
| 100 | VMV0 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO88NDB1 |
| 112 | GDA1/IO88PDB1 |
| 113 | GDB0/IO87NDB1 |
| 114 | GDB1/IO87PDB1 |
| 115 | GDC0/IO86NDB1 |
| 116 | GDC1/IO86PDB1 |
| 117 | IO84NDB1 |
| 118 | IO84PDB1 |
| 119 | IO82NDB1 |
| 120 | IO82PDB1 |
| 121 | IO81PSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | IO77NDB1 |
| 125 | IO77PDB1 |
| 126 | NC |
| 127 | IO74NDB1 |
| 128 | GCC2/IO74PDB1 |
| 129 | GCB2/IO73PSB1 |
| 130 | GND |
| 131 | GCA2/IO72PSB1 |
| 132 | GCA1/IO71PDB1 |
| 133 | GCA0/IO71NDB1 |
| 134 | GCB0/IO70NDB1 |
| 135 | GCB1/IO70PDB1 |
| 136 | GCC0/IO69NDB1 |
| 137 | GCC1/IO69PDB1 |
| 138 | IO67NDB1 |
| 139 | IO67PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO65PSB1 |
| 144 | IO64NDB1 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| 145 | IO64PDB1 |
| 146 | IO63NDB1 |
| 147 | IO63PDB1 |
| 148 | IO62NDB1 |
| 149 | GBC2/IO62PDB1 |
| 150 | IO61NDB1 |
| 151 | GBB2/IO61PDB1 |
| 152 | IO60NDB1 |
| 153 | GBA2/IO60PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO59RSB0 |
| 159 | GBA0/IO58RSB0 |
| 160 | GBB1/IO57RSB0 |
| 161 | GBB0/IO56RSB0 |
| 162 | GND |
| 163 | GBC1/IO55RSB0 |
| 164 | GBC0/IO54RSB0 |
| 165 | IO52RSB0 |
| 166 | IO50RSB0 |
| 167 | IO48RSB0 |
| 168 | IO46RSB0 |
| 169 | IO44RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO36RSB0 |
| 173 | IO35RSB0 |
| 174 | IO34RSB0 |
| 175 | IO33RSB0 |
| 176 | IO32RSB0 |
| 177 | IO31RSB0 |
| 178 | GND |
| 179 | IO29RSB0 |
| 180 | IO28RSB0 |

| PQ208 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| 181 | IO27RSB0 |
| 182 | IO26RSB0 |
| 183 | IO25RSB0 |
| 184 | IO24RSB0 |
| 185 | IO23RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO20RSB0 |
| 189 | IO19RSB0 |
| 190 | IO18RSB0 |
| 191 | IO17RSB0 |
| 192 | IO16RSB0 |
| 193 | IO14RSB0 |
| 194 | IO12RSB0 |
| 195 | GND |
| 196 | IO10RSB0 |
| 197 | IO09RSB0 |
| 198 | IO08RSB0 |
| 199 | IO07RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO04RSB0 |
| A4 | GAB1/IO05RSB0 |
| A5 | IO08RSB0 |
| A6 | GND |
| A7 | IO11RSB0 |
| A8 | VCC |
| A9 | IO16RSB0 |
| A10 | GBA0/IO23RSB0 |
| A11 | GBA1/IO24RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO53RSB1 |
| B2 | GND |
| B3 | GAA0/IO02RSB0 |
| B4 | GAA1/IO03RSB0 |
| B5 | IO00RSB0 |
| B6 | IO10RSB0 |
| B7 | IO12RSB0 |
| B8 | IO14RSB0 |
| B9 | GBB0/IO21RSB0 |
| B10 | GBB1/IO22RSB0 |
| B11 | GND |
| B12 | VMV0 |
| C1 | IO95RSB1 |
| C2 | GFA2/IO83RSB1 |
| C3 | GAC2/IO94RSB1 |
| C4 | VCC |
| C5 | IO01RSB0 |
| C6 | IO09RSB0 |
| C7 | IO13RSB0 |
| C8 | IO15RSB0 |
| C9 | IO17RSB0 |
| C10 | GBA2/IO25RSB0 |
| C11 | IO26RSB0 |
| C12 | GBC2/IO29RSB0 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| D1 | IO91RSB1 |
| D2 | IO92RSB1 |
| D3 | IO93RSB1 |
| D4 | GAA2/IO51RSB1 |
| D5 | GAC0/IO06RSB0 |
| D6 | GAC1/IO07RSB0 |
| D7 | GBC0/IO19RSB0 |
| D8 | GBC1/IO20RSB0 |
| D9 | GBB2/IO27RSB0 |
| D10 | IO18RSB0 |
| D11 | IO28RSB0 |
| D12 | GCB1/IO37RSB0 |
| E1 | VCC |
| E2 | GFC0/IO88RSB1 |
| E3 | GFC1/IO89RSB1 |
| E4 | VCCIB1 |
| E5 | IO52RSB1 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO35RSB0 |
| E9 | VCCIB0 |
| E10 | VCC |
| E11 | GCA0/IO40RSB0 |
| E12 | IO30RSB0 |
| F1 | GFB0/IO86RSB1 |
| F2 | VCOMPLF |
| F3 | GFB1/IO87RSB1 |
| F4 | IO90RSB1 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO36RSB0 |
| F9 | GCB0/IO38RSB0 |
| F10 | GND |
| F11 | GCA1/IO39RSB0 |
| F12 | GCA2/IO41RSB0 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| G1 | GFA1/IO84RSB1 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO85RSB1 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO45RSB0 |
| G9 | IO32RSB0 |
| G10 | GCC2/IO43RSB0 |
| G11 | IO31RSB0 |
| G12 | GCB2/IO42RSB0 |
| H1 | VCC |
| H2 | GFB2/IO82RSB1 |
| H3 | GFC2/IO81RSB1 |
| H4 | GEC1/IO77RSB1 |
| H5 | VCC |
| H6 | IO34RSB0 |
| H7 | IO44RSB0 |
| H8 | GDB2/IO55RSB1 |
| H9 | GDC0/IO46RSB0 |
| H10 | VCCIB0 |
| H11 | IO33RSB0 |
| H12 | VCC |
| J1 | GEB1/IO75RSB1 |
| J2 | IO78RSB1 |
| J3 | VCCIB1 |
| J4 | GEC0/IO76RSB1 |
| J5 | IO79RSB1 |
| J6 | IO80RSB1 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO54RSB1 |
| J10 | TDO |
| J11 | GDA1/IO49RSB0 |
| J12 | GDB1/IO47RSB0 |

| FG144 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| K1 | GEB0/IO74RSB1 |
| K2 | GEA1/IO73RSB1 |
| K3 | GEA0/IO72RSB1 |
| K4 | GEA2/IO71RSB1 |
| K5 | IO65RSB1 |
| K6 | IO64RSB1 |
| K7 | GND |
| K8 | IO57RSB1 |
| K9 | GDC2/IO56RSB1 |
| K10 | GND |
| K11 | GDA0/IO50RSB0 |
| K12 | GDB0/IO48RSB0 |
| L1 | GND |
| L2 | VMV1 |
| L3 | GEB2/IO70RSB1 |
| L4 | IO67RSB1 |
| L5 | VCCIB1 |
| L6 | IO62RSB1 |
| L7 | IO59RSB1 |
| L8 | IO58RSB1 |
| L9 | TMS |
| L10 | VJTAG |
| L11 | VMV1 |
| L12 | TRST |
| M1 | GNDQ |
| M2 | GEC2/IO69RSB1 |
| M3 | IO68RSB1 |
| M4 | IO66RSB1 |
| M5 | IO63RSB1 |
| M6 | IO61RSB1 |
| M7 | IO60RSB1 |
| M8 | NC |
| M9 | TDI |
| M10 | VCCIB1 |
| M11 | VPUMP |
| M12 | GNDQ |

# 5 – Datasheet Information

## List of Changes

The following table lists critical changes that were made in each version of the ProASIC3 datasheet.

| Revision | Changes | Page |
|---|---|---|
| Revision 18<br>(March 2016) | Updated 3.3 V DC supply voltage's maximum Commercial and Industrial values from 3.3 V to 3.6 V in Table 2-2 (SAR 72693). | 2-2 |
| | Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833). | NA |
| Revision 17<br>(June 2015) | Removed PQFP embedded heat spreader info. from Table 2-5 (SAR 52320). | 2-6 |
| | Updated "VCCIBx I/O Supply Voltage" (SAR 43323). | 3-1 |
| Revision 16<br>(December 2014) | Updated "ProASIC3 Ordering Information". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079).<br>Added Note "Only devices with package size greater than or equal to 5x5 are supported". | 1-IV |
| | Updated Table Note (2) in Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature so that the Table Note is not applicable for Maximum Storage Temperature $T_{STG}$ (SAR 54297). | 2-3 |
| | Added values for Drive strength 2 mA in Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Table 2-43 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, and Table 2-44 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew (SAR 57184). | 2-34, 2-35, 2-36, 2-37 |
| | Added Figure 2-1 • High-Temperature Data Retention (HTR) (SAR 45466). | 2-3 |
| | Updates made to maintain the style and consistency of the document. | NA |
| Revision 15<br>(July 2014) | Added corner pad table note (3) to "QN132 – Bottom View" (SAR 47442). | 4-6 |
| | Ambient temperature removed in Table 2-2, table notes and "ProASIC3 Ordering Information" figure were modified (SAR 48343). | 2-2<br>1-IV |
| | Other updates were made to maintain the style and consistency of the datasheet. | NA |
| Revision 14<br>(April 2014) | Note added for the discontinuance of QN132 package to the following tables and section: "ProASIC3 Devices", "I/Os Per Package 1", "ProASIC3 FPGAs Package Sizes Dimensions" and "QN132 – Bottom View" section (SAR 55118). | I, III, 4-6 |

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (September 2011) | The "In-System Programming (ISP) and Security" section and Security section were revised to clarify that although no existing security measures can give an absolute guarantee, Microsemi FPGAs implement the best security available in the industry (SAR 32865). | I |
| | The value of 34 I/Os for the QN48 package in A3P030 was added to the "I/Os Per Package 1" section (SAR 33907). | III |
| | The Y security option and Licensed DPA Logo were added to the "ProASIC3 Ordering Information" section. The trademarked Licensed DPA Logo identifies that a product is covered by a DPA counter-measures license from Cryptography Research (SAR 32151). | IV |
| | The "Specifying I/O States During Programming" section is new (SAR 21281). | 1-7 |
| | In Table 2-2 • Recommended Operating Conditions 1, VPUMP programming voltage in programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45" (SAR 30666). It was corrected in v2.0 of this datasheet in April 2007 but inadvertently changed back to “3.0 to 3.6 V” in v1.4 in August 2009. The following changes were made to Table 2-2 • Recommended Operating Conditions 1:<br>VCCPLL analog power supply (PLL) was changed from "1.4 to 1.6" to "1.425 to 1.575" (SAR 33850).<br>For VCCI and VMV, values for 3.3 V DC and 3.3 V DC Wide Range were corrected. The correct value for 3.3 V DC is "3.0 to 3.6 V" and the correct value for 3.3 V Wide Range is "2.7 to 3.6" (SAR 33848). | 2-2 |
| | Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings was update to restore values to the correct columns. Previously the Slew Rate column was missing and data were aligned incorrectly (SAR 34034). | 2-24 |
| | The notes regarding drive strength in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section and "3.3 V LVCMOS Wide Range" section tables were revised for clarification. They now state that the minimum drive strength for the default software configuration when run in wide range is ±100 µA. The drive strength displayed in software is supported in normal range only. For a detailed I/V curve, refer to the IBIS models (SAR 25700). | 2-22, 2-39 |

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