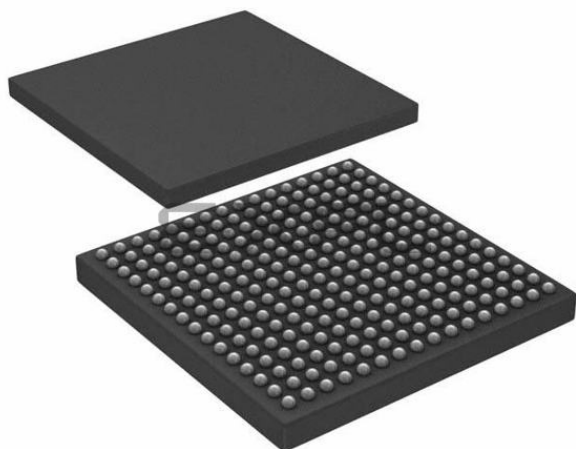




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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	157
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p250-fg256i

I/Os Per Package ¹

ProASIC3 Devices	A3P015 ²	A3P030	A3P060	A3P125	A3P250 ³		A3P400 ³		A3P600		A3P1000	
Cortex-M1 Devices					M1A3P250 ^{3,5}		M1A3P400 ³		M1A3P600		M1A3P1000	
Package	I/O Type											
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs	Single-Ended I/O ⁴	Differential I/O Pairs
QN48	–	34	–	–	–	–		–	–	–	–	–
QN68	49	49	–	–	–	–	–	–		–	–	–
QN132 ⁷	–	81	80	84	87	19	–	–		–	–	–
CS121	–	–	96	–	–	–	–	–	–	–	–	–
VQ100	–	77	71	71	68	13	–	–		–	–	–
TQ144	–	–	91	100	–	–	–	–	–	–	–	–
PQ208	–	–	–	133	151	34	151	34	154	35	154	35
FG144	–	–	96	97	97	24	97	25	97	25	97	25
FG256 ^{5,6}	–	–	–	–	157	38	178	38	177	43	177	44
FG484 ⁶	–	–	–	–	–	–	194	38	235	60	300	74

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3 FPGA Fabric User Guide](#) to ensure complying with design and board migration requirements.
2. A3P015 is not recommended for new designs.
3. For A3P250 and A3P400 devices, the maximum number of LVPECL pairs in east and west banks cannot exceed 15. Refer to the [ProASIC3 FPGA Fabric Users Guide](#) for position assignments of the 15 LVPECL pairs.
4. Each used differential I/O pair reduces the number of single-ended I/Os available by two.
5. The M1A3P250 device does not support FG256 package.
6. FG256 and FG484 are footprint-compatible packages.
7. Package not available.

Table 1 • ProASIC3 FPGAs Package Sizes Dimensions

Package	CS121	QN48	QN68	QN132 *	VQ100	TQ144	PQ208	FG144	FG256	FG484
Length × Width (mm × mm)	6 × 6	6 × 6	8 × 8	8 × 8	14 × 14	20 × 20	28 × 28	13 × 13	17 × 17	23 × 23
Nominal Area (mm ²)	36	36	64	64	196	400	784	169	289	529
Pitch (mm)	0.5	0.4	0.4	0.5	0.5	0.5	0.5	1.0	1.0	1.0
Height (mm)	0.99	0.90	0.90	0.75	1.00	1.40	3.40	1.45	1.60	2.23

Note: * Package not available

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges.

In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-2 on page 2-5](#).

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points ([Figure 2-2 on page 2-5](#)).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.2\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1.1\text{ V}$

VCC Trip Point:

Ramping up: $0.6\text{ V} < \text{trip_point_up} < 1.1\text{ V}$

Ramping down: $0.5\text{ V} < \text{trip_point_down} < 1\text{ V}$

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see [Figure 2-2 on page 2-5](#) for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels ($0.75\text{ V} \pm 0.25\text{ V}$), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the [ProASIC3 FPGA Fabric User's Guide](#) for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in [Table 2-5 on page 2-6](#).

P = Power dissipation

Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case V_{CCI} (per standard)
 Standard I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
3.3 V LVCMOS Wide Range ²	100 μA	8 mA	High	35	–	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns
2.5 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
1.8 V LVCMOS	4 mA	4 mA	High	35	–	0.45	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns
1.5 V LVCMOS	2 mA	2 mA	High	35	–	0.45	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-52 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	11.14	0.04	1.52	0.43	11.14	9.54	3.51	3.61	14.53	12.94	ns
		–1	0.51	9.48	0.04	1.29	0.36	9.48	8.12	2.99	3.07	12.36	11.00	ns
		–2	0.45	8.32	0.03	1.14	0.32	8.32	7.13	2.62	2.70	10.85	9.66	ns
100 μA	4 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 μA	6 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 μA	8 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
100 μA	16 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-53 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	14.97	0.04	1.52	0.43	14.97	12.79	3.52	3.41	18.36	16.18	ns
		–1	0.51	12.73	0.04	1.29	0.36	12.73	10.88	2.99	2.90	15.62	13.77	ns
		–2	0.45	11.18	0.03	1.14	0.32	11.18	9.55	2.63	2.55	13.71	12.08	ns
100 μA	4 mA	Std.	0.60	10.36	0.04	1.52	0.43	10.36	8.93	3.99	4.24	13.75	12.33	ns
		–1	0.51	8.81	0.04	1.29	0.36	8.81	7.60	3.39	3.60	11.70	10.49	ns
		–2	0.45	7.74	0.03	1.14	0.32	7.74	6.67	2.98	3.16	10.27	9.21	ns
100 μA	6 mA	Std.	0.60	10.36	0.04	1.52	0.43	10.36	8.93	3.99	4.24	13.75	12.33	ns
		–1	0.51	8.81	0.04	1.29	0.36	8.81	7.60	3.39	3.60	11.70	10.49	ns
		–2	0.45	7.74	0.03	1.14	0.32	7.74	6.67	2.98	3.16	10.27	9.21	ns
100 μA	8 mA	Std.	0.60	7.81	0.04	1.52	0.43	7.81	6.85	4.32	4.76	11.20	10.24	ns
		–1	0.51	6.64	0.04	1.29	0.36	6.64	5.82	3.67	4.05	9.53	8.71	ns
		–2	0.45	5.83	0.03	1.14	0.32	5.83	5.11	3.22	3.56	8.36	7.65	ns
100 μA	16 mA	Std.	0.60	7.81	0.04	1.52	0.43	7.81	6.85	4.32	4.76	11.20	10.24	ns
		–1	0.51	6.64	0.04	1.29	0.36	6.64	5.82	3.67	4.05	9.53	8.71	ns
		–2	0.45	5.83	0.03	1.14	0.32	5.83	5.11	3.22	3.56	8.36	7.65	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-58 • Minimum and Maximum DC Input and Output Levels
 Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	-0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	-0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

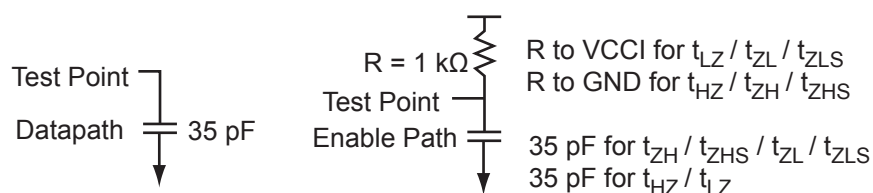


Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.

Table 2-73 • 1.8 V LVC MOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	14.80	0.04	1.20	0.43	13.49	14.80	2.25	1.46	15.73	17.04	ns
	–1	0.56	12.59	0.04	1.02	0.36	11.48	12.59	1.91	1.25	13.38	14.49	ns
	–2	0.49	11.05	0.03	0.90	0.32	10.08	11.05	1.68	1.09	11.75	12.72	ns
4 mA	Std.	0.66	9.90	0.04	1.20	0.43	9.73	9.90	2.65	2.50	11.97	12.13	ns
	–1	0.56	8.42	0.04	1.02	0.36	8.28	8.42	2.26	2.12	10.18	10.32	ns
	–2	0.49	7.39	0.03	0.90	0.32	7.27	7.39	1.98	1.86	8.94	9.06	ns
6 mA	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	–1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	–2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns
8 mA	Std.	0.66	7.44	0.04	1.20	0.43	7.58	7.32	2.94	2.99	9.81	9.56	ns
	–1	0.56	6.33	0.04	1.02	0.36	6.44	6.23	2.50	2.54	8.35	8.13	ns
	–2	0.49	5.55	0.03	0.90	0.32	5.66	5.47	2.19	2.23	7.33	7.14	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-74 • 1.8 V LVC MOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	11.21	0.04	1.20	0.43	8.53	11.21	1.99	1.21	ns
	–1	0.56	9.54	0.04	1.02	0.36	7.26	9.54	1.69	1.03	ns
	–2	0.49	8.37	0.03	0.90	0.32	6.37	8.37	1.49	0.90	ns
4 mA	Std.	0.66	6.34	0.04	1.20	0.43	5.38	6.34	2.41	2.48	ns
	–1	0.56	5.40	0.04	1.02	0.36	4.58	5.40	2.05	2.11	ns
	–2	0.49	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-77 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-78 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

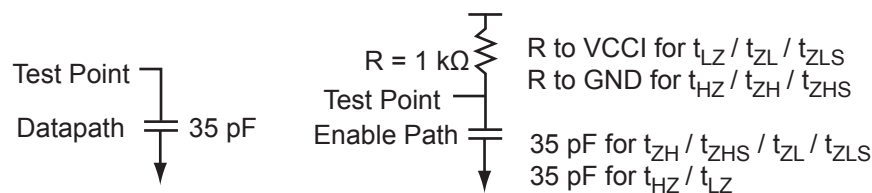


Figure 2-10 • AC Loading

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-22 for a complete table of trip points.

Table 2-81 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-82 • 1.5 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 1.4\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [Fusion](#), [IGLOO®/e](#), and [ProASIC3/E Macro Library Guide](#).

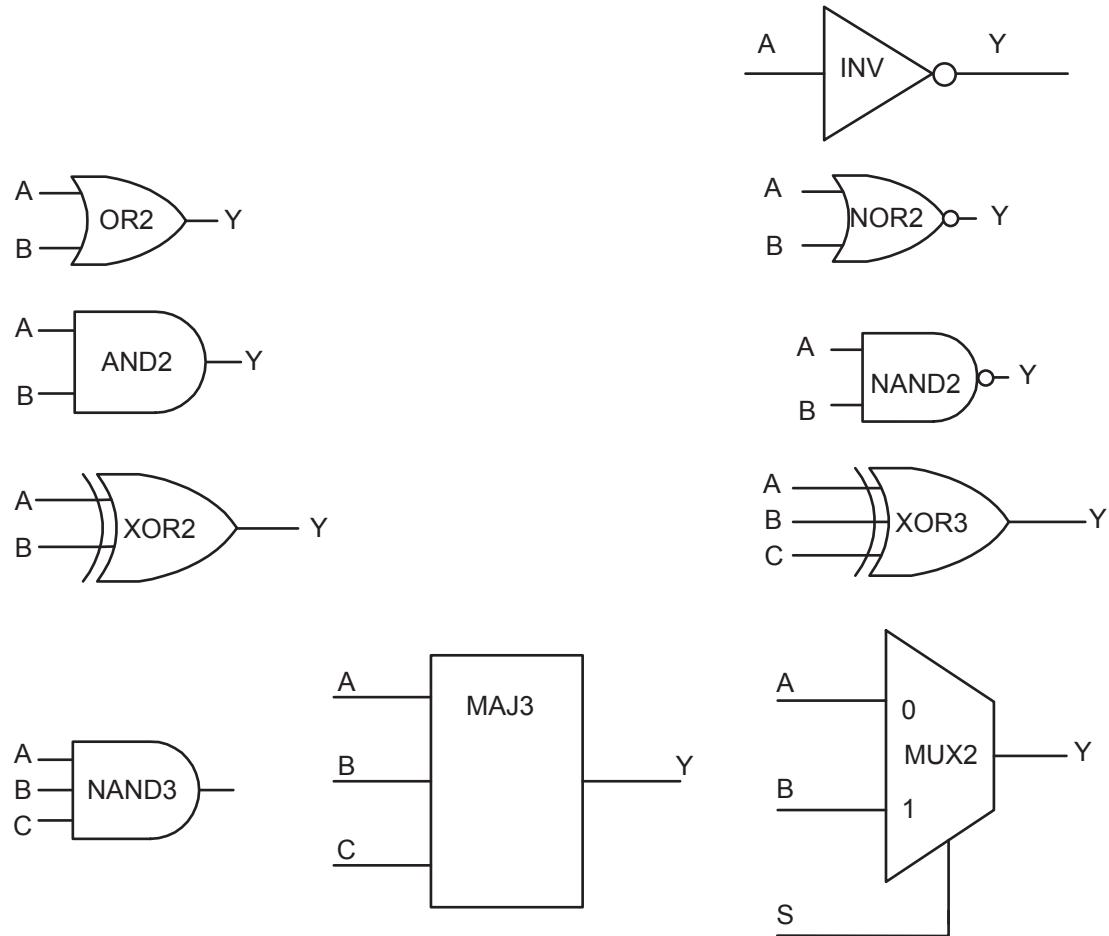


Figure 2-24 • Sample of Combinatorial Cells

Embedded SRAM and FIFO Characteristics

SRAM

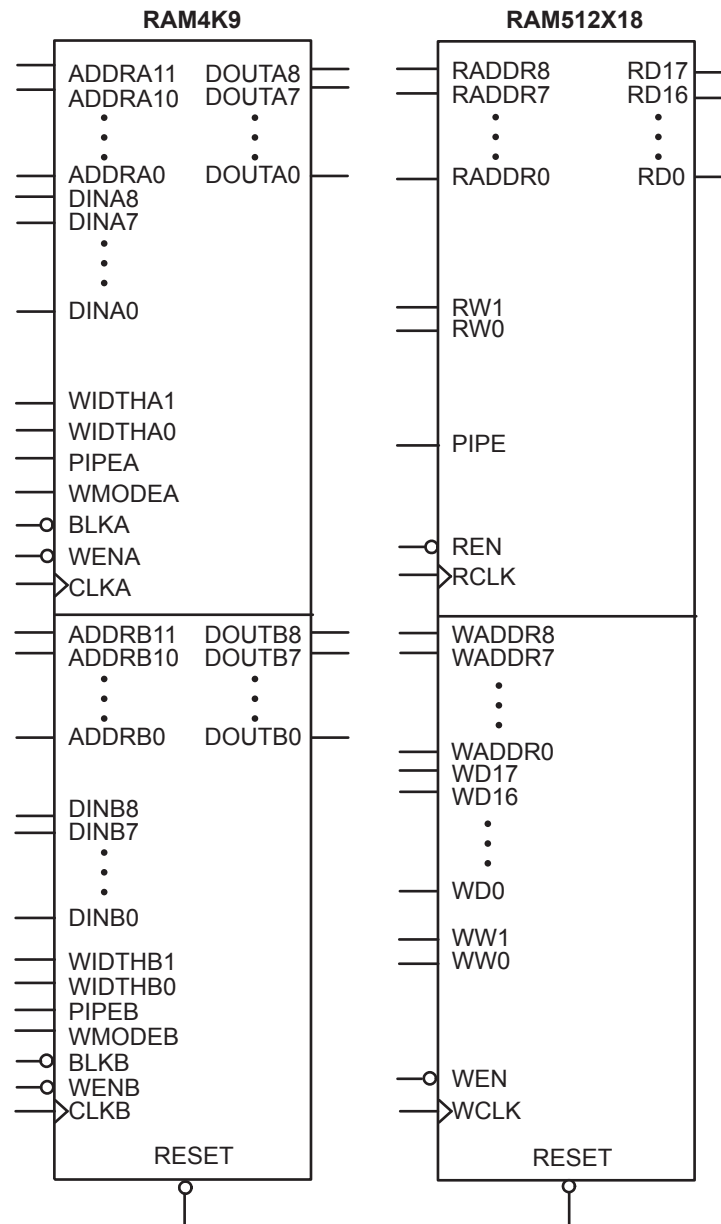


Figure 2-30 • RAM Models

FIFO

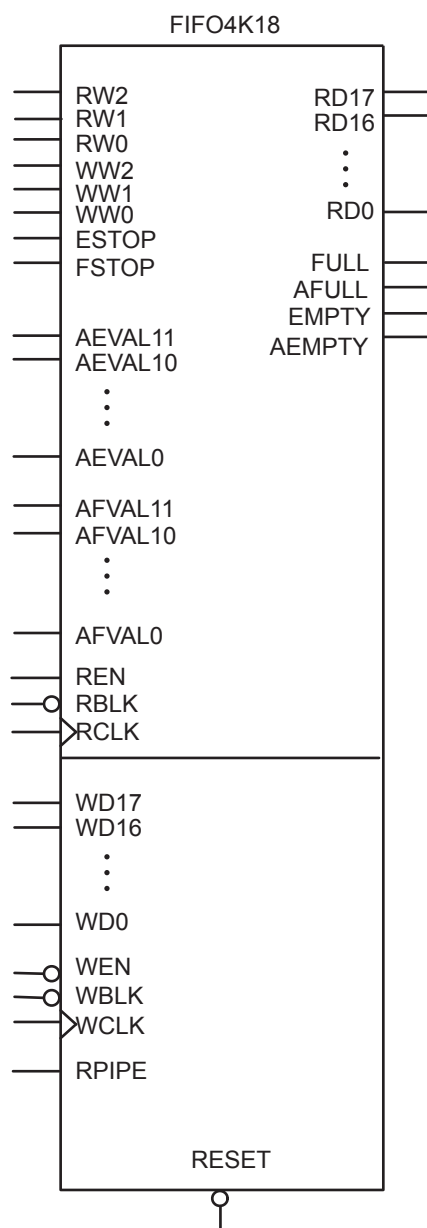


Figure 2-36 • FIFO Model

Table 2-121 • A3P250 FIFO 1k×4**Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.05	4.61	5.42	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Table 2-122 • A3P250 FIFO 2k×2

 Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.39	5.00	5.88	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Table 2-123 • A3P250 FIFO 4k×1

 Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.86	5.53	6.50	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns

QN132	
Pin Number	A3P030 Function
A1	IO01RSB1
A2	IO81RSB1
A3	NC
A4	IO80RSB1
A5	GEC0/IO77RSB1
A6	NC
A7	GEB0/IO75RSB1
A8	IO73RSB1
A9	NC
A10	VCC
A11	IO71RSB1
A12	IO68RSB1
A13	IO63RSB1
A14	IO60RSB1
A15	NC
A16	IO59RSB1
A17	IO57RSB1
A18	VCC
A19	IO54RSB1
A20	IO52RSB1
A21	IO49RSB1
A22	IO48RSB1
A23	IO47RSB1
A24	TDI
A25	TRST
A26	IO44RSB0
A27	NC
A28	IO43RSB0
A29	IO42RSB0
A30	IO40RSB0
A31	IO39RSB0
A32	GDC0/IO36RSB0
A33	NC
A34	VCC
A35	IO34RSB0
A36	IO31RSB0

QN132	
Pin Number	A3P030 Function
A37	IO26RSB0
A38	IO23RSB0
A39	NC
A40	IO22RSB0
A41	IO20RSB0
A42	IO18RSB0
A43	VCC
A44	IO15RSB0
A45	IO12RSB0
A46	IO10RSB0
A47	IO09RSB0
A48	IO06RSB0
B1	IO02RSB1
B2	IO82RSB1
B3	GND
B4	IO79RSB1
B5	NC
B6	GND
B7	IO74RSB1
B8	NC
B9	GND
B10	IO70RSB1
B11	IO67RSB1
B12	IO64RSB1
B13	IO61RSB1
B14	GND
B15	IO58RSB1
B16	IO56RSB1
B17	GND
B18	IO53RSB1
B19	IO50RSB1
B20	GND
B21	IO46RSB1
B22	TMS
B23	TDO
B24	IO45RSB0

QN132	
Pin Number	A3P030 Function
B25	GND
B26	NC
B27	IO41RSB0
B28	GND
B29	GDA0/IO37RSB0
B30	NC
B31	GND
B32	IO33RSB0
B33	IO30RSB0
B34	IO27RSB0
B35	IO24RSB0
B36	GND
B37	IO21RSB0
B38	IO19RSB0
B39	GND
B40	IO16RSB0
B41	IO13RSB0
B42	GND
B43	IO08RSB0
B44	IO05RSB0
C1	IO03RSB1
C2	IO00RSB1
C3	NC
C4	IO78RSB1
C5	GEA0/IO76RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO69RSB1
C10	IO66RSB1
C11	IO65RSB1
C12	IO62RSB1
C13	NC
C14	NC
C15	IO55RSB1
C16	VCCIB1

VQ100		VQ100		VQ100	
Pin Number	A3P030 Function	Pin Number	A3P030 Function	Pin Number	A3P030 Function
1	GND	37	VCC	73	IO27RSB0
2	IO82RSB1	38	GND	74	IO26RSB0
3	IO81RSB1	39	VCCIB1	75	IO25RSB0
4	IO80RSB1	40	IO49RSB1	76	IO24RSB0
5	IO79RSB1	41	IO47RSB1	77	IO23RSB0
6	IO78RSB1	42	IO46RSB1	78	IO22RSB0
7	IO77RSB1	43	IO45RSB1	79	IO21RSB0
8	IO76RSB1	44	IO44RSB1	80	IO20RSB0
9	GND	45	IO43RSB1	81	IO19RSB0
10	IO75RSB1	46	IO42RSB1	82	IO18RSB0
11	IO74RSB1	47	TCK	83	IO17RSB0
12	GEC0/IO73RSB1	48	TDI	84	IO16RSB0
13	GEA0/IO72RSB1	49	TMS	85	IO15RSB0
14	GEB0/IO71RSB1	50	NC	86	IO14RSB0
15	IO70RSB1	51	GND	87	VCCIB0
16	IO69RSB1	52	VPUMP	88	GND
17	VCC	53	NC	89	VCC
18	VCCIB1	54	TDO	90	IO12RSB0
19	IO68RSB1	55	TRST	91	IO10RSB0
20	IO67RSB1	56	VJTAG	92	IO08RSB0
21	IO66RSB1	57	IO41RSB0	93	IO07RSB0
22	IO65RSB1	58	IO40RSB0	94	IO06RSB0
23	IO64RSB1	59	IO39RSB0	95	IO05RSB0
24	IO63RSB1	60	IO38RSB0	96	IO04RSB0
25	IO62RSB1	61	IO37RSB0	97	IO03RSB0
26	IO61RSB1	62	IO36RSB0	98	IO02RSB0
27	IO60RSB1	63	GDB0/IO34RSB0	99	IO01RSB0
28	IO59RSB1	64	GDA0/IO33RSB0	100	IO00RSB0
29	IO58RSB1	65	GDC0/IO32RSB0		
30	IO57RSB1	66	VCCIB0		
31	IO56RSB1	67	GND		
32	IO55RSB1	68	VCC		
33	IO54RSB1	69	IO31RSB0		
34	IO53RSB1	70	IO30RSB0		
35	IO52RSB1	71	IO29RSB0		
36	IO51RSB1	72	IO28RSB0		

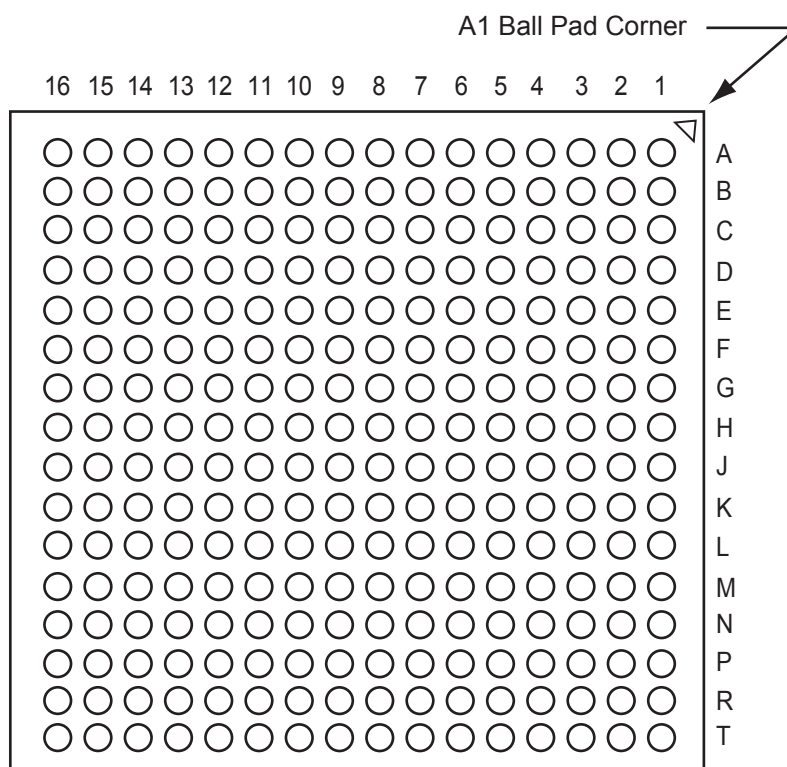
PQ208	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	NC
8	NC
9	IO130RSB1
10	IO129RSB1
11	NC
12	IO128RSB1
13	NC
14	NC
15	NC
16	VCC
17	GND
18	VCCIB1
19	IO127RSB1
20	NC
21	GFC1/IO126RSB1
22	GFC0/IO125RSB1
23	GFB1/IO124RSB1
24	GFB0/IO123RSB1
25	VCOMPLF
26	GFA0/IO122RSB1
27	VCCPLF
28	GFA1/IO121RSB1
29	GND
30	GFA2/IO120RSB1
31	NC
32	GFB2/IO119RSB1
33	NC
34	GFC2/IO118RSB1
35	IO117RSB1
36	NC

PQ208	
Pin Number	A3P125 Function
37	IO116RSB1
38	IO115RSB1
39	NC
40	VCCIB1
41	GND
42	IO114RSB1
43	IO113RSB1
44	GEC1/IO112RSB1
45	GEC0/IO111RSB1
46	GEB1/IO110RSB1
47	GEB0/IO109RSB1
48	GEA1/IO108RSB1
49	GEA0/IO107RSB1
50	VMV1
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO106RSB1
56	GEB2/IO105RSB1
57	GEC2/IO104RSB1
58	IO103RSB1
59	IO102RSB1
60	IO101RSB1
61	IO100RSB1
62	VCCIB1
63	IO99RSB1
64	IO98RSB1
65	GND
66	IO97RSB1
67	IO96RSB1
68	IO95RSB1
69	IO94RSB1
70	IO93RSB1
71	VCC
72	VCCIB1

PQ208	
Pin Number	A3P125 Function
73	IO92RSB1
74	IO91RSB1
75	IO90RSB1
76	IO89RSB1
77	IO88RSB1
78	IO87RSB1
79	IO86RSB1
80	IO85RSB1
81	GND
82	IO84RSB1
83	IO83RSB1
84	IO82RSB1
85	IO81RSB1
86	IO80RSB1
87	IO79RSB1
88	VCC
89	VCCIB1
90	IO78RSB1
91	IO77RSB1
92	IO76RSB1
93	IO75RSB1
94	IO74RSB1
95	IO73RSB1
96	GDC2/IO72RSB1
97	GND
98	GDB2/IO71RSB1
99	GDA2/IO70RSB1
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV1
105	GND
106	VPUMP
107	NC
108	TDO

FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG256 – Bottom View



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1