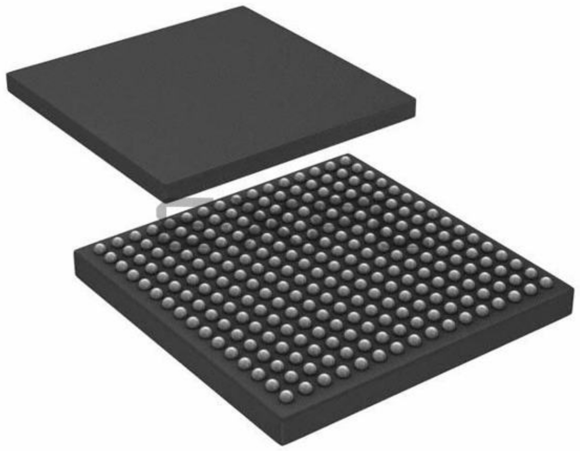
# Microchip Technology - A3P400-1FG256 Datasheet



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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 55296 |
| Number of I/O | 178 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 256-LBGA |
| Supplier Device Package | 256-FPBGA (17x17) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p400-1fg256 |

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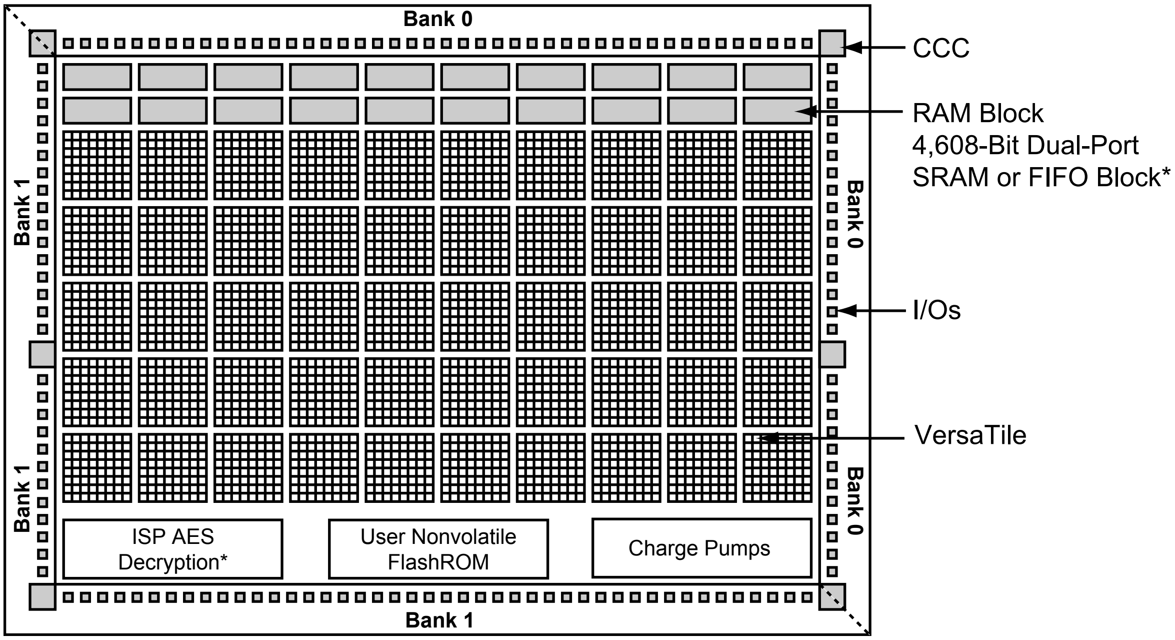
## Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

## Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory†
- Extensive CCCs and PLLs†
- Advanced I/O structure



*Note:* **Not supported by A3P015 and A3P030 devices*

***Figure 1-1 •*** **ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)**

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† *The A3P015 and A3P030 do not support PLL or SRAM.*

# 2 – ProASIC3 DC and Switching Characteristics

## General Specifications

### Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

***Table 2-1 •*** **Absolute Maximum Ratings**

| Symbol | Parameter | Limits | Units |
|---|---|---|---|
| VCC | DC core supply voltage | –0.3 to 1.65 | V |
| VJTAG | JTAG DC voltage | –0.3 to 3.75 | V |
| VPUMP | Programming voltage | –0.3 to 3.75 | V |
| VCCPLL | Analog power supply (PLL) | –0.3 to 1.65 | V |
| VCCI | DC I/O output buffer supply voltage | –0.3 to 3.75 | V |
| VMV | DC I/O input buffer supply voltage | –0.3 to 3.75 | V |
| VI | I/O input voltage | –0.3 V to 3.6 V<br>(when I/O hot insertion mode is enabled)<br>–0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled) | V |
| $T_{STG}$ [2] | Storage temperature | –65 to +150 | °C |
| $T_J$ [2] | Junction temperature | +125 | °C |

*Notes:*

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

*Table 2-42 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 4 mA | Std. | 0.66 | 10.26 | 0.04 | 1.02 | 0.43 | 10.45 | 8.90 | 2.64 | 2.46 | 12.68 | 11.13 | ns |
| | –1 | 0.56 | 8.72 | 0.04 | 0.86 | 0.36 | 8.89 | 7.57 | 2.25 | 2.09 | 10.79 | 9.47 | ns |
| | –2 | 0.49 | 7.66 | 0.03 | 0.76 | 0.32 | 7.80 | 6.64 | 1.98 | 1.83 | 9.47 | 8.31 | ns |
| 6 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 8 mA | Std. | 0.66 | 7.27 | 0.04 | 1.02 | 0.43 | 7.41 | 6.28 | 2.98 | 3.04 | 9.65 | 8.52 | ns |
| | –1 | 0.56 | 6.19 | 0.04 | 0.86 | 0.36 | 6.30 | 5.35 | 2.54 | 2.59 | 8.20 | 7.25 | ns |
| | –2 | 0.49 | 5.43 | 0.03 | 0.76 | 0.32 | 5.53 | 4.69 | 2.23 | 2.27 | 7.20 | 6.36 | ns |
| 12 mA | Std. | 0.66 | 5.58 | 0.04 | 1.02 | 0.43 | 5.68 | 4.87 | 3.21 | 3.42 | 7.92 | 7.11 | ns |
| | –1 | 0.56 | 4.75 | 0.04 | 0.86 | 0.36 | 4.84 | 4.14 | 2.73 | 2.91 | 6.74 | 6.05 | ns |
| | –2 | 0.49 | 4.17 | 0.03 | 0.76 | 0.32 | 4.24 | 3.64 | 2.39 | 2.55 | 5.91 | 5.31 | ns |
| 16 mA | Std. | 0.66 | 5.21 | 0.04 | 1.02 | 0.43 | 5.30 | 4.56 | 3.26 | 3.51 | 7.54 | 6.80 | ns |
| | –1 | 0.56 | 4.43 | 0.04 | 0.86 | 0.36 | 4.51 | 3.88 | 2.77 | 2.99 | 6.41 | 5.79 | ns |
| | –2 | 0.49 | 3.89 | 0.03 | 0.76 | 0.32 | 3.96 | 3.41 | 2.43 | 2.62 | 5.63 | 5.08 | ns |
| 24 mA | Std. | 0.66 | 4.85 | 0.04 | 1.02 | 0.43 | 4.94 | 4.54 | 3.32 | 3.88 | 7.18 | 6.78 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 0.86 | 0.36 | 4.20 | 3.87 | 2.82 | 3.30 | 6.10 | 5.77 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.76 | 0.32 | 3.69 | 3.39 | 2.48 | 2.90 | 5.36 | 5.06 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-53* • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 14.97 | 0.04 | 1.52 | 0.43 | 14.97 | 12.79 | 3.52 | 3.41 | 18.36 | 16.18 | ns |
| | | –1 | 0.51 | 12.73 | 0.04 | 1.29 | 0.36 | 12.73 | 10.88 | 2.99 | 2.90 | 15.62 | 13.77 | ns |
| | | –2 | 0.45 | 11.18 | 0.03 | 1.14 | 0.32 | 11.18 | 9.55 | 2.63 | 2.55 | 13.71 | 12.08 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 10.36 | 0.04 | 1.52 | 0.43 | 10.36 | 8.93 | 3.99 | 4.24 | 13.75 | 12.33 | ns |
| | | –1 | 0.51 | 8.81 | 0.04 | 1.29 | 0.36 | 8.81 | 7.60 | 3.39 | 3.60 | 11.70 | 10.49 | ns |
| | | –2 | 0.45 | 7.74 | 0.03 | 1.14 | 0.32 | 7.74 | 6.67 | 2.98 | 3.16 | 10.27 | 9.21 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 10.36 | 0.04 | 1.52 | 0.43 | 10.36 | 8.93 | 3.99 | 4.24 | 13.75 | 12.33 | ns |
| | | –1 | 0.51 | 8.81 | 0.04 | 1.29 | 0.36 | 8.81 | 7.60 | 3.39 | 3.60 | 11.70 | 10.49 | ns |
| | | –2 | 0.45 | 7.74 | 0.03 | 1.14 | 0.32 | 7.74 | 6.67 | 2.98 | 3.16 | 10.27 | 9.21 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 7.81 | 0.04 | 1.52 | 0.43 | 7.81 | 6.85 | 4.32 | 4.76 | 11.20 | 10.24 | ns |
| | | –1 | 0.51 | 6.64 | 0.04 | 1.29 | 0.36 | 6.64 | 5.82 | 3.67 | 4.05 | 9.53 | 8.71 | ns |
| | | –2 | 0.45 | 5.83 | 0.03 | 1.14 | 0.32 | 5.83 | 5.11 | 3.22 | 3.56 | 8.36 | 7.65 | ns |
| 100 µA | 16 mA | Std. | 0.60 | 7.81 | 0.04 | 1.52 | 0.43 | 7.81 | 6.85 | 4.32 | 4.76 | 11.20 | 10.24 | ns |
| | | –1 | 0.51 | 6.64 | 0.04 | 1.29 | 0.36 | 6.64 | 5.82 | 3.67 | 4.05 | 9.53 | 8.71 | ns |
| | | –2 | 0.45 | 5.83 | 0.03 | 1.14 | 0.32 | 5.83 | 5.11 | 3.22 | 3.56 | 8.36 | 7.65 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-55 •* **3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks**

| Drive Strength | Equiv. Software Default Drive Strength Option[1] | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 100 µA | 2 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 4 mA | Std. | 0.60 | 14.64 | 0.04 | 1.52 | 0.43 | 14.64 | 12.97 | 3.21 | 3.15 | ns |
| | | –1 | 0.51 | 12.45 | 0.04 | 1.29 | 0.36 | 12.45 | 11.04 | 2.73 | 2.68 | ns |
| | | –2 | 0.45 | 10.93 | 0.03 | 1.13 | 0.32 | 10.93 | 9.69 | 2.39 | 2.35 | ns |
| 100 µA | 6 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |
| 100 µA | 8 mA | Std. | 0.60 | 10.16 | 0.04 | 1.52 | 0.43 | 10.16 | 9.08 | 3.71 | 3.98 | ns |
| | | –1 | 0.51 | 8.64 | 0.04 | 1.29 | 0.36 | 8.64 | 7.73 | 3.15 | 3.39 | ns |
| | | –2 | 0.45 | 7.58 | 0.03 | 1.13 | 0.32 | 7.58 | 6.78 | 2.77 | 2.97 | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-62 •* **2.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 8.28 | 0.04 | 1.30 | 0.43 | 7.41 | 8.28 | 2.25 | 2.07 | 9.64 | 10.51 | ns |
| | –1 | 0.56 | 7.04 | 0.04 | 1.10 | 0.36 | 6.30 | 7.04 | 1.92 | 1.76 | 8.20 | 8.94 | ns |
| | –2 | 0.49 | 6.18 | 0.03 | 0.97 | 0.32 | 5.53 | 6.18 | 1.68 | 1.55 | 7.20 | 7.85 | ns |
| 6 mA | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 8 mA | Std. | 0.66 | 4.85 | 0.04 | 1.30 | 0.43 | 4.65 | 4.85 | 2.59 | 2.71 | 6.88 | 7.09 | ns |
| | –1 | 0.56 | 4.13 | 0.04 | 1.10 | 0.36 | 3.95 | 4.13 | 2.20 | 2.31 | 5.85 | 6.03 | ns |
| | –2 | 0.49 | 3.62 | 0.03 | 0.97 | 0.32 | 3.47 | 3.62 | 1.93 | 2.02 | 5.14 | 5.29 | ns |
| 12 mA | Std. | 0.66 | 3.21 | 0.04 | 1.30 | 0.43 | 3.27 | 3.14 | 2.82 | 3.11 | 5.50 | 5.38 | ns |
| | –1 | 0.56 | 2.73 | 0.04 | 1.10 | 0.36 | 2.78 | 2.67 | 2.40 | 2.65 | 4.68 | 4.57 | ns |
| | –2 | 0.49 | 2.39 | 0.03 | 0.97 | 0.32 | 2.44 | 2.35 | 2.11 | 2.32 | 4.11 | 4.02 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-63 •* **2.5 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.66 | 10.84 | 0.04 | 1.30 | 0.43 | 10.64 | 10.84 | 2.26 | 1.99 | 12.87 | 13.08 | ns |
| | –1 | 0.56 | 9.22 | 0.04 | 1.10 | 0.36 | 9.05 | 9.22 | 1.92 | 1.69 | 10.95 | 11.12 | ns |
| | –2 | 0.49 | 8.10 | 0.03 | 0.97 | 0.32 | 7.94 | 8.10 | 1.68 | 1.49 | 9.61 | 9.77 | ns |
| 6 mA | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | –1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | –2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 8 mA | Std. | 0.66 | 7.37 | 0.04 | 1.30 | 0.43 | 7.50 | 7.36 | 2.59 | 2.61 | 9.74 | 9.60 | ns |
| | –1 | 0.56 | 6.27 | 0.04 | 1.10 | 0.36 | 6.38 | 6.26 | 2.20 | 2.22 | 8.29 | 8.16 | ns |
| | –2 | 0.49 | 5.50 | 0.03 | 0.97 | 0.32 | 5.60 | 5.50 | 1.93 | 1.95 | 7.27 | 7.17 | ns |
| 12 mA | Std. | 0.66 | 5.63 | 0.04 | 1.30 | 0.43 | 5.73 | 5.51 | 2.83 | 3.01 | 7.97 | 7.74 | ns |
| | –1 | 0.56 | 4.79 | 0.04 | 1.10 | 0.36 | 4.88 | 4.68 | 2.41 | 2.56 | 6.78 | 6.59 | ns |
| | –2 | 0.49 | 4.20 | 0.03 | 0.97 | 0.32 | 4.28 | 4.11 | 2.11 | 2.25 | 5.95 | 5.78 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-73 •*** **1.8 V LVCMOS Low Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard Plus I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 14.80 | 0.04 | 1.20 | 0.43 | 13.49 | 14.80 | 2.25 | 1.46 | 15.73 | 17.04 | ns |
| | –1 | 0.56 | 12.59 | 0.04 | 1.02 | 0.36 | 11.48 | 12.59 | 1.91 | 1.25 | 13.38 | 14.49 | ns |
| | –2 | 0.49 | 11.05 | 0.03 | 0.90 | 0.32 | 10.08 | 11.05 | 1.68 | 1.09 | 11.75 | 12.72 | ns |
| 4 mA | Std. | 0.66 | 9.90 | 0.04 | 1.20 | 0.43 | 9.73 | 9.90 | 2.65 | 2.50 | 11.97 | 12.13 | ns |
| | –1 | 0.56 | 8.42 | 0.04 | 1.02 | 0.36 | 8.28 | 8.42 | 2.26 | 2.12 | 10.18 | 10.32 | ns |
| | –2 | 0.49 | 7.39 | 0.03 | 0.90 | 0.32 | 7.27 | 7.39 | 1.98 | 1.86 | 8.94 | 9.06 | ns |
| 6 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | –1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | –2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |
| 8 mA | Std. | 0.66 | 7.44 | 0.04 | 1.20 | 0.43 | 7.58 | 7.32 | 2.94 | 2.99 | 9.81 | 9.56 | ns |
| | –1 | 0.56 | 6.33 | 0.04 | 1.02 | 0.36 | 6.44 | 6.23 | 2.50 | 2.54 | 8.35 | 8.13 | ns |
| | –2 | 0.49 | 5.55 | 0.03 | 0.90 | 0.32 | 5.66 | 5.47 | 2.19 | 2.23 | 7.33 | 7.14 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-74 •*** **1.8 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V**
**Applicable to Standard I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 11.21 | 0.04 | 1.20 | 0.43 | 8.53 | 11.21 | 1.99 | 1.21 | ns |
| | –1 | 0.56 | 9.54 | 0.04 | 1.02 | 0.36 | 7.26 | 9.54 | 1.69 | 1.03 | ns |
| | –2 | 0.49 | 8.37 | 0.03 | 0.90 | 0.32 | 6.37 | 8.37 | 1.49 | 0.90 | ns |
| 4 mA | Std. | 0.66 | 6.34 | 0.04 | 1.20 | 0.43 | 5.38 | 6.34 | 2.41 | 2.48 | ns |
| | –1 | 0.56 | 5.40 | 0.04 | 1.02 | 0.36 | 4.58 | 5.40 | 2.05 | 2.11 | ns |
| | –2 | 0.49 | 4.74 | 0.03 | 0.90 | 0.32 | 4.02 | 4.74 | 1.80 | 1.85 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Characteristics

***Table 2-80 •*** **1.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 2 mA | Std. | 0.66 | 8.36 | 0.04 | 1.44 | 0.43 | 6.82 | 8.36 | 3.39 | 2.77 | 9.06 | 10.60 | ns |
| | –1 | 0.56 | 7.11 | 0.04 | 1.22 | 0.36 | 5.80 | 7.11 | 2.88 | 2.35 | 7.71 | 9.02 | ns |
| | –2 | 0.49 | 6.24 | 0.03 | 1.07 | 0.32 | 5.10 | 6.24 | 2.53 | 2.06 | 6.76 | 7.91 | ns |
| 4 mA | Std. | 0.66 | 5.31 | 0.04 | 1.44 | 0.43 | 4.85 | 5.31 | 3.74 | 3.40 | 7.09 | 7.55 | ns |
| | –1 | 0.56 | 4.52 | 0.04 | 1.22 | 0.36 | 4.13 | 4.52 | 3.18 | 2.89 | 6.03 | 6.42 | ns |
| | –2 | 0.49 | 3.97 | 0.03 | 1.07 | 0.32 | 3.62 | 3.97 | 2.79 | 2.54 | 5.29 | 5.64 | ns |
| 6 mA | Std. | 0.66 | 4.67 | 0.04 | 1.44 | 0.43 | 4.55 | 4.67 | 3.82 | 3.56 | 6.78 | 6.90 | ns |
| | –1 | 0.56 | 3.97 | 0.04 | 1.22 | 0.36 | 3.87 | 3.97 | 3.25 | 3.03 | 5.77 | 5.87 | ns |
| | –2 | 0.49 | 3.49 | 0.03 | 1.07 | 0.32 | 3.40 | 3.49 | 2.85 | 2.66 | 5.07 | 5.16 | ns |
| 8 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 12 mA | Std. | 0.66 | 4.08 | 0.04 | 1.44 | 0.43 | 4.15 | 3.58 | 3.94 | 4.20 | 6.39 | 5.81 | ns |
| | –1 | 0.56 | 3.47 | 0.04 | 1.22 | 0.36 | 3.53 | 3.04 | 3.36 | 3.58 | 5.44 | 4.95 | ns |
| | –2 | 0.49 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

*Table 2-97 •* **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

*Note: *See Figure 2-16 on page 2-71 for more information.*

# Embedded SRAM and FIFO Characteristics

## SRAM

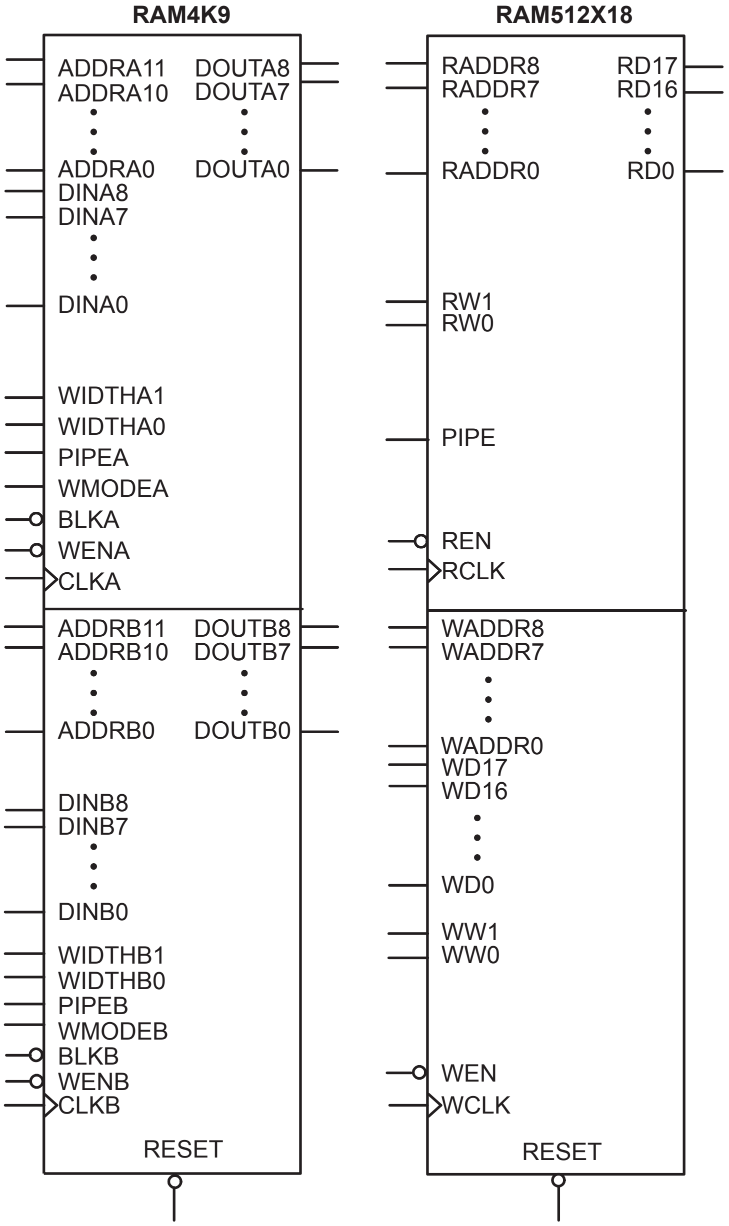


*Figure 2-30* • **RAM Models**

## Timing Characteristics

***Table 2-116* • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BLK hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.36 | 2.68 | 3.15 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 1.79 | 2.03 | 2.39 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge | 0.33 | 0.28 | 0.25 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-122* • A3P250 FIFO 2k×2**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

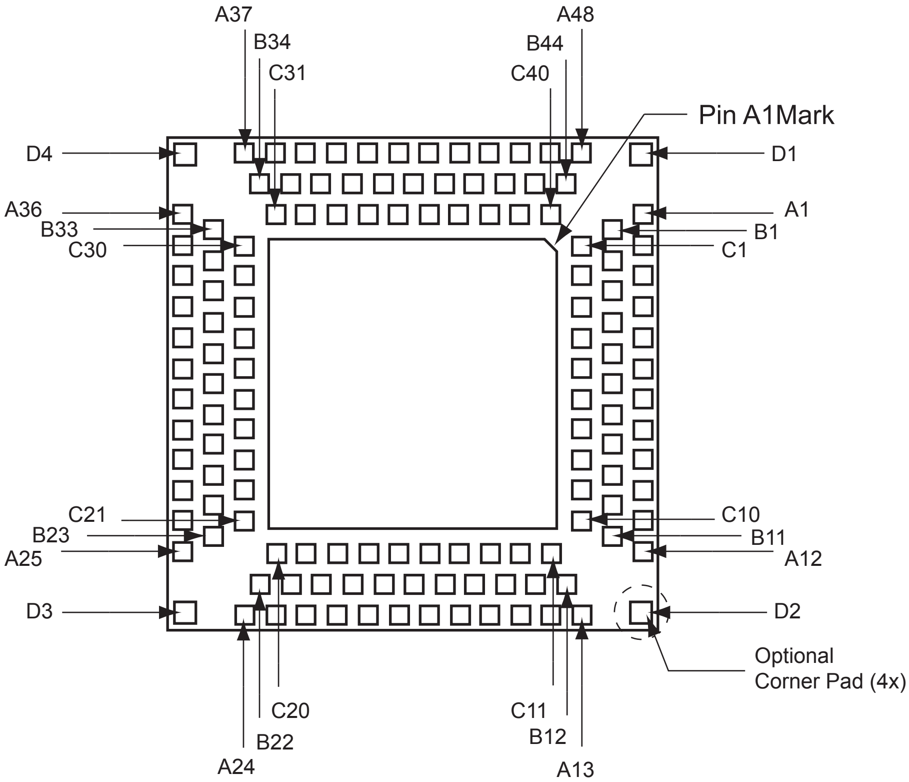
| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 4.39 | 5.00 | 5.88 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
|  | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

***Table 2-123* • A3P250 FIFO 4k×1**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 4.86 | 5.53 | 6.50 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.36 | 2.68 | 3.15 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |

| QN68 | |
|---|---|
| **Pin Number** | **A3P030 Function** |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |
| 36 | TDO |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | VCCIB0 |
| 60 | GND |
| 61 | VCC |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

## QN132 – Bottom View



*Notes:*

1. *The die attach paddle center of the package is tied to ground (GND).*
2. *Option corner pads come with this device and package combination. It is optional to tie them to ground or leave them floating.*
3. *The QN132 package is discontinued and is not available for ProASIC3 devices.*
4. For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| TQ144 | |
|---|---|
| Pin Number | A3P125 Function |
| 1 | GAA2/IO67RSB1 |
| 2 | IO68RSB1 |
| 3 | GAB2/IO69RSB1 |
| 4 | IO132RSB1 |
| 5 | GAC2/IO131RSB1 |
| 6 | IO130RSB1 |
| 7 | IO129RSB1 |
| 8 | IO128RSB1 |
| 9 | VCC |
| 10 | GND |
| 11 | VCCIB1 |
| 12 | IO127RSB1 |
| 13 | GFC1/IO126RSB1 |
| 14 | GFC0/IO125RSB1 |
| 15 | GFB1/IO124RSB1 |
| 16 | GFB0/IO123RSB1 |
| 17 | VCOMPLF |
| 18 | GFA0/IO122RSB1 |
| 19 | VCCPLF |
| 20 | GFA1/IO121RSB1 |
| 21 | GFA2/IO120RSB1 |
| 22 | GFB2/IO119RSB1 |
| 23 | GFC2/IO118RSB1 |
| 24 | IO117RSB1 |
| 25 | IO116RSB1 |
| 26 | IO115RSB1 |
| 27 | GND |
| 28 | VCCIB1 |
| 29 | GEC1/IO112RSB1 |
| 30 | GEC0/IO111RSB1 |
| 31 | GEB1/IO110RSB1 |
| 32 | GEB0/IO109RSB1 |
| 33 | GEA1/IO108RSB1 |
| 34 | GEA0/IO107RSB1 |
| 35 | VMV1 |
| 36 | GNDQ |
| 37 | NC |
| 38 | GEA2/IO106RSB1 |
| 39 | GEB2/IO105RSB1 |
| 40 | GEC2/IO104RSB1 |
| 41 | IO103RSB1 |
| 42 | IO102RSB1 |
| 43 | IO101RSB1 |
| 44 | IO100RSB1 |
| 45 | VCC |
| 46 | GND |
| 47 | VCCIB1 |
| 48 | IO99RSB1 |
| 49 | IO97RSB1 |
| 50 | IO95RSB1 |
| 51 | IO93RSB1 |
| 52 | IO92RSB1 |
| 53 | IO90RSB1 |
| 54 | IO88RSB1 |
| 55 | IO86RSB1 |
| 56 | IO84RSB1 |
| 57 | IO83RSB1 |
| 58 | IO82RSB1 |
| 59 | IO81RSB1 |
| 60 | IO80RSB1 |
| 61 | IO79RSB1 |
| 62 | VCC |
| 63 | GND |
| 64 | VCCIB1 |
| 65 | GDC2/IO72RSB1 |
| 66 | GDB2/IO71RSB1 |
| 67 | GDA2/IO70RSB1 |
| 68 | GNDQ |
| 69 | TCK |
| 70 | TDI |
| 71 | TMS |
| 72 | VMV1 |
| 73 | VPUMP |
| 74 | NC |
| 75 | TDO |
| 76 | TRST |
| 77 | VJTAG |
| 78 | GDA0/IO66RSB0 |
| 79 | GDB0/IO64RSB0 |
| 80 | GDB1/IO63RSB0 |
| 81 | VCCIB0 |
| 82 | GND |
| 83 | IO60RSB0 |
| 84 | GCC2/IO59RSB0 |
| 85 | GCB2/IO58RSB0 |
| 86 | GCA2/IO57RSB0 |
| 87 | GCA0/IO56RSB0 |
| 88 | GCA1/IO55RSB0 |
| 89 | GCB0/IO54RSB0 |
| 90 | GCB1/IO53RSB0 |
| 91 | GCC0/IO52RSB0 |
| 92 | GCC1/IO51RSB0 |
| 93 | IO50RSB0 |
| 94 | IO49RSB0 |
| 95 | NC |
| 96 | NC |
| 97 | NC |
| 98 | VCCIB0 |
| 99 | GND |
| 100 | VCC |
| 101 | IO47RSB0 |
| 102 | GBC2/IO45RSB0 |
| 103 | IO44RSB0 |
| 104 | GBB2/IO43RSB0 |
| 105 | IO42RSB0 |
| 106 | GBA2/IO41RSB0 |
| 107 | VMV0 |
| 108 | GNDQ |

| FG256 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| G13 | GCC1/IO48PPB1 |
| G14 | IO47NPB1 |
| G15 | IO54PDB1 |
| G16 | IO54NDB1 |
| H1 | GFB0/IO109NPB3 |
| H2 | GFA0/IO108NDB3 |
| H3 | GFB1/IO109PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO110NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO48NPB1 |
| H13 | GCB1/IO49PPB1 |
| H14 | GCA0/IO50NPB1 |
| H15 | NC |
| H16 | GCB0/IO49NPB1 |
| J1 | GFA2/IO107PPB3 |
| J2 | GFA1/IO108PDB3 |
| J3 | VCCPLF |
| J4 | IO106NDB3 |
| J5 | GFB2/IO106PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO52PPB1 |
| J13 | GCA1/IO50PPB1 |
| J14 | GCC2/IO53PPB1 |
| J15 | NC |
| J16 | GCA2/IO51PDB1 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| K1 | GFC2/IO105PDB3 |
| K2 | IO107NPB3 |
| K3 | IO104PPB3 |
| K4 | NC |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO52NPB1 |
| K14 | IO55RSB1 |
| K15 | IO53NPB1 |
| K16 | IO51NDB1 |
| L1 | IO105NDB3 |
| L2 | IO104NPB3 |
| L3 | NC |
| L4 | IO102RSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO59VPB1 |
| L14 | IO57VDB1 |
| L15 | IO57UDB1 |
| L16 | IO56PDB1 |
| M1 | IO103PDB3 |
| M2 | NC |
| M3 | IO101NPB3 |
| M4 | GEC0/IO100NPB3 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | NC |
| M9 | IO74RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | NC |
| M14 | GDB1/IO59UPB1 |
| M15 | GDC1/IO58UDB1 |
| M16 | IO56NDB1 |
| N1 | IO103NDB3 |
| N2 | IO101PPB3 |
| N3 | GEC1/IO100PPB3 |
| N4 | NC |
| N5 | GNDQ |
| N6 | GEA2/IO97RSB2 |
| N7 | IO86RSB2 |
| N8 | IO82RSB2 |
| N9 | IO75RSB2 |
| N10 | IO69RSB2 |
| N11 | IO64RSB2 |
| N12 | GNDQ |
| N13 | NC |
| N14 | VJTAG |
| N15 | GDC0/IO58VDB1 |
| N16 | GDA1/IO60UDB1 |
| P1 | GEB1/IO99PDB3 |
| P2 | GEB0/IO99NDB3 |
| P3 | NC |
| P4 | NC |
| P5 | IO92RSB2 |
| P6 | IO89RSB2 |
| P7 | IO85RSB2 |
| P8 | IO81RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| P9 | IO76RSB2 |
| P10 | IO71RSB2 |
| P11 | IO66RSB2 |
| P12 | NC |
| P13 | TCK |
| P14 | VPUMP |
| P15 | TRST |
| P16 | GDA0/IO60VDB1 |
| R1 | GEA1/IO98PDB3 |
| R2 | GEA0/IO98NDB3 |
| R3 | NC |
| R4 | GEC2/IO95RSB2 |
| R5 | IO91RSB2 |
| R6 | IO88RSB2 |
| R7 | IO84RSB2 |
| R8 | IO80RSB2 |
| R9 | IO77RSB2 |
| R10 | IO72RSB2 |
| R11 | IO68RSB2 |
| R12 | IO65RSB2 |
| R13 | GDB2/IO62RSB2 |
| R14 | TDI |
| R15 | NC |
| R16 | TDO |
| T1 | GND |
| T2 | IO94RSB2 |
| T3 | GEB2/IO96RSB2 |
| T4 | IO93RSB2 |
| T5 | IO90RSB2 |
| T6 | IO87RSB2 |
| T7 | IO83RSB2 |
| T8 | IO79RSB2 |
| T9 | IO78RSB2 |
| T10 | IO73RSB2 |
| T11 | IO70RSB2 |
| T12 | GDC2/IO63RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P250 Function** |
| T13 | IO67RSB2 |
| T14 | GDA2/IO61RSB2 |
| T15 | TMS |
| T16 | GND |

| FG484 | |
|---|---|
| Pin Number | A3P400 Function |
| E21 | NC |
| E22 | NC |
| F1 | NC |
| F2 | NC |
| F3 | NC |
| F4 | IO154VDB3 |
| F5 | IO155VDB3 |
| F6 | IO11RSB0 |
| F7 | IO07RSB0 |
| F8 | GAC0/IO04RSB0 |
| F9 | GAC1/IO05RSB0 |
| F10 | IO20RSB0 |
| F11 | IO24RSB0 |
| F12 | IO33RSB0 |
| F13 | IO39RSB0 |
| F14 | IO45RSB0 |
| F15 | GBC0/IO54RSB0 |
| F16 | IO48RSB0 |
| F17 | VMV0 |
| F18 | IO61NPB1 |
| F19 | IO63PDB1 |
| F20 | NC |
| F21 | NC |
| F22 | NC |
| G1 | NC |
| G2 | NC |
| G3 | NC |
| G4 | IO151VDB3 |
| G5 | IO151UDB3 |
| G6 | GAC2/IO153UDB3 |
| G7 | IO06RSB0 |
| G8 | GNDQ |
| G9 | IO10RSB0 |
| G10 | IO19RSB0 |
| G11 | IO26RSB0 |
| G12 | IO30RSB0 |
| G13 | IO40RSB0 |
| G14 | IO46RSB0 |
| G15 | GNDQ |
| G16 | IO47RSB0 |
| G17 | GBB2/IO61PPB1 |
| G18 | IO53RSB0 |
| G19 | IO63NDB1 |
| G20 | NC |
| G21 | NC |
| G22 | NC |
| H1 | NC |
| H2 | NC |
| H3 | VCC |
| H4 | IO150PDB3 |
| H5 | IO08RSB0 |
| H6 | IO153VDB3 |
| H7 | IO152VDB3 |
| H8 | VMV0 |
| H9 | VCCIB0 |
| H10 | VCCIB0 |
| H11 | IO25RSB0 |
| H12 | IO31RSB0 |
| H13 | VCCIB0 |
| H14 | VCCIB0 |
| H15 | VMV1 |
| H16 | GBC2/IO62PDB1 |
| H17 | IO65RSB1 |
| H18 | IO52RSB0 |
| H19 | IO66PDB1 |
| H20 | VCC |
| H21 | NC |
| H22 | NC |
| J1 | NC |
| J2 | NC |
| J3 | NC |
| J4 | IO150NDB3 |
| J5 | IO149NPB3 |
| J6 | IO09RSB0 |
| J7 | IO152UDB3 |
| J8 | VCCIB3 |
| J9 | GND |
| J10 | VCC |
| J11 | VCC |
| J12 | VCC |
| J13 | VCC |
| J14 | GND |
| J15 | VCCIB1 |
| J16 | IO62NDB1 |
| J17 | IO49RSB0 |
| J18 | IO64PPB1 |
| J19 | IO66NDB1 |
| J20 | NC |
| J21 | NC |
| J22 | NC |
| K1 | NC |
| K2 | NC |
| K3 | NC |
| K4 | IO148NDB3 |
| K5 | IO148PDB3 |
| K6 | IO149PPB3 |
| K7 | GFC1/IO147PPB3 |
| K8 | VCCIB3 |
| K9 | VCC |
| K10 | GND |
| K11 | GND |
| K12 | GND |
| K13 | GND |
| K14 | VCC |
| K15 | VCCIB1 |
| K16 | GCC1/IO67PPB1 |
| K17 | IO64NPB1 |
| K18 | IO73PDB1 |

| Revision | Changes | Page |
|---|---|---|
| v2.0<br>(continued) | Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated. | 3-20 to 3-20 |
| | Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated. | 3-9 |
| | Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated. | 3-22 to 3-22 |
| | Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated. | 3-18 |
| | Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated. | 3-24 to 3-26 |
| | The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated. | 3-27 |
| | Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new. | 3-82 to 3-84 |
| | Figure 3-43 • Timing Diagram was updated. | 3-96 |
| | Ambient was deleted from the "Speed Grade and Temperature Grade Matrix". | iv |
| | Notes were added to the package diagrams identifying if they were top or bottom view. | N/A |
| | The A3P030 "132-Pin QFN" table is new. | 4-2 |
| | The A3P060 "132-Pin QFN" table is new. | 4-4 |
| | The A3P125 "132-Pin QFN" table is new. | 4-6 |
| | The A3P250 "132-Pin QFN" table is new. | 4-8 |
| | The A3P030 "100-Pin VQFP" table is new. | 4-11 |
| Advance v0.7<br>(January 2007) | In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77. | ii |
| Advance v0.6<br>(April 2006) | The term flow-through was changed to pass-through. | N/A |
| | Table 1 was updated to include the QN132. | ii |
| | The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated. | ii |
| | "Automotive ProASIC3 Ordering Information" was updated with the QN132. | iii |
| | "Temperature Grade Offerings" was updated with the QN132. | iii |
| | B-LVDS and M-LDVS are new I/O standards added to the datasheet. | N/A |
| | The term flow-through was changed to pass-through. | N/A |
| | Figure 2-7 • Efficient Long-Line Resources was updated. | 2-7 |
| | The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated. | 2-16 |
| | The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options. | 2-24 |
| | The "SRAM and FIFO" section was updated. | 2-21 |

# Datasheet Categories

### Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3 Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

### Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

### Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

### Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

### Unmarked (production)

This version contains information that is considered to be final.

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