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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	151
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p400-1pqg208

Table 2-44 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
4 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
6 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
8 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
12 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns
16 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-45 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
4 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
6 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	–2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
8 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns

Table 2-61 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.51	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.45	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
6 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
8 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.60	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.51	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.45	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.60	5.76	0.04	1.31	0.43	5.87	5.53	3.36	3.44	8.11	7.76	ns
	–1	0.51	4.90	0.04	1.11	0.36	4.99	4.70	2.86	2.92	6.90	6.60	ns
	–2	0.45	4.30	0.03	0.98	0.32	4.38	4.13	2.51	2.57	6.05	5.80	ns
24 mA	Std.	0.60	5.51	0.04	1.31	0.43	5.50	5.51	3.43	3.87	7.74	7.74	ns
	–1	0.51	4.68	0.04	1.11	0.36	4.68	4.68	2.92	3.29	6.58	6.59	ns
	–2	0.45	4.11	0.03	0.98	0.32	4.11	4.11	2.56	2.89	5.78	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

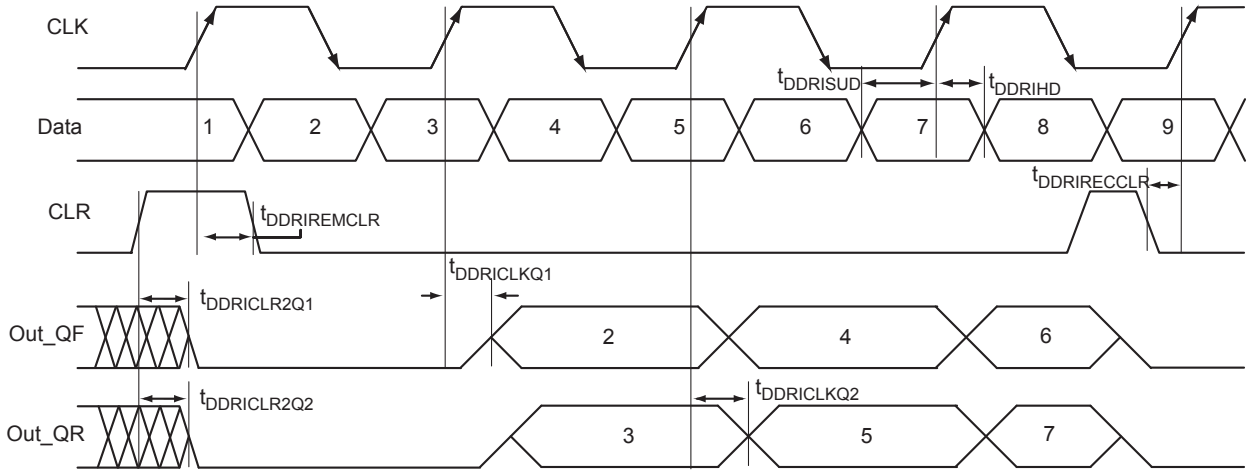


Figure 2-21 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-102 • **Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.27	0.31	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.39	0.44	0.52	ns
$t_{DDRISUD}$	Data Setup for Input DDR (Fall)	0.25	0.28	0.33	ns
	Data Setup for Input DDR (Rise)	0.25	0.28	0.33	ns
t_{DDRIHD}	Data Hold for Input DDR (Fall)	0.00	0.00	0.00	ns
	Data Hold for Input DDR (Rise)	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.46	0.53	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	309	263	MHz

Note: For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.

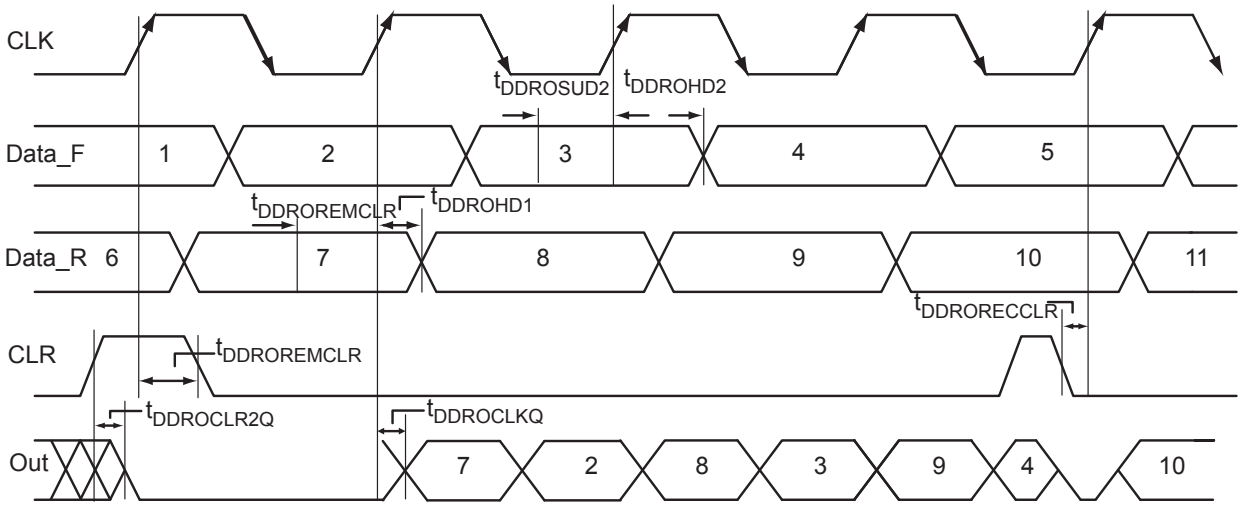


Figure 2-23 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-104 • **Output DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.

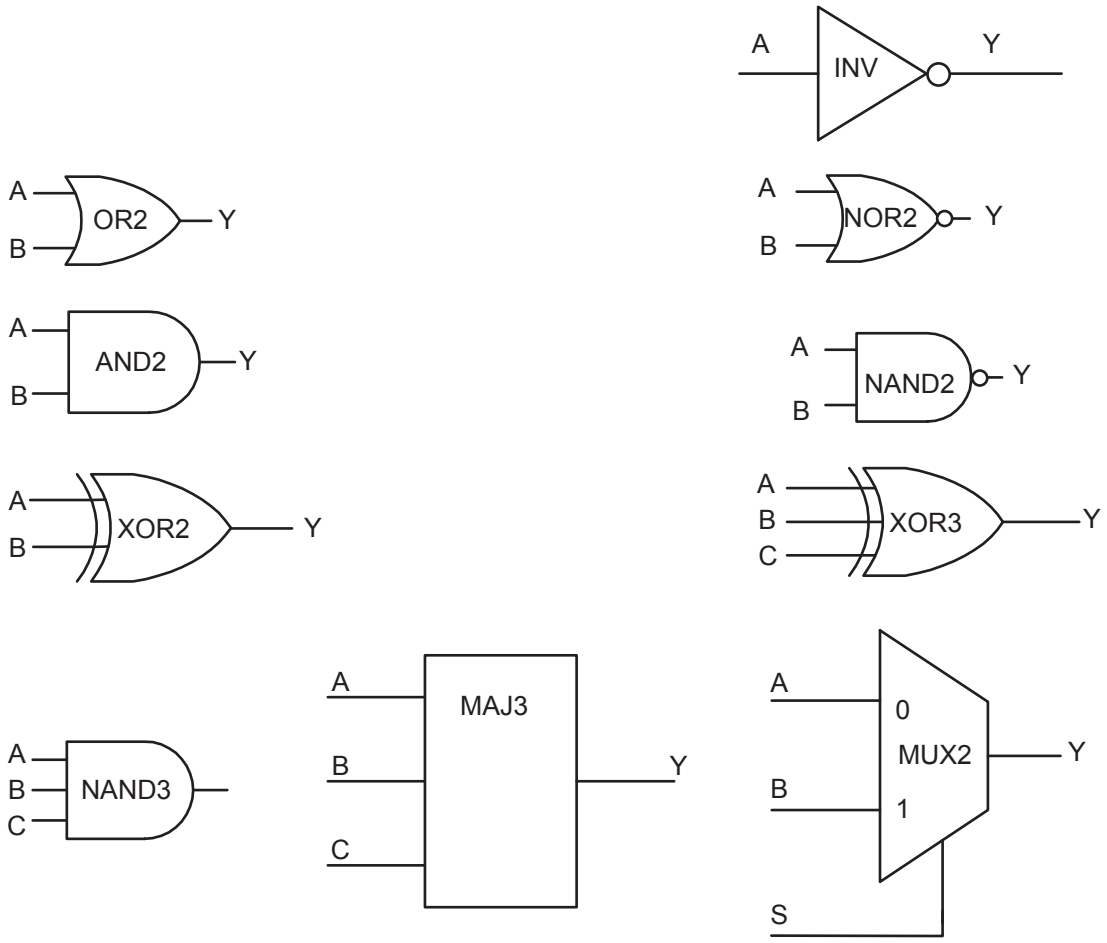
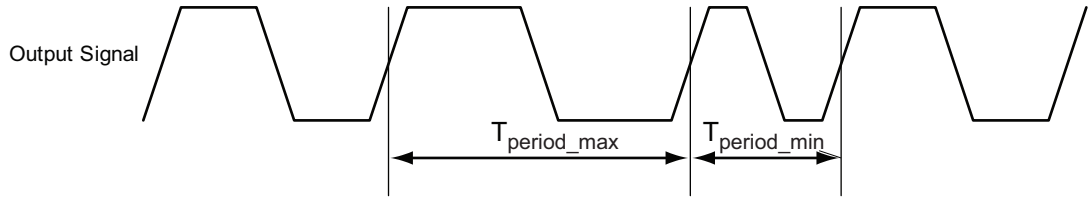


Figure 2-24 • **Sample of Combinatorial Cells**



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-29 • **Peak-to-Peak Jitter Definition**

3 – Pin Descriptions

Supply Pins

GND **Ground**

Ground supply voltage to the core, I/O outputs, and I/O logic.

GNDQ **Ground (quiet)**

Quiet ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ must always be connected to GND on the board.

VCC **Core Supply Voltage**

Supply voltage to the FPGA core, nominally 1.5 V. VCC is required for powering the JTAG state machine in addition to VJTAG. Even when a device is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the device.

VCCIBx **I/O Supply Voltage**

Supply voltage to the bank's I/O output buffers and I/O logic. Bx is the I/O bank number. There are up to eight I/O banks on low power flash devices plus a dedicated VJTAG bank. Each bank can have a separate VCCI connection. All I/Os in a bank will run off the same VCCIBx supply. VCCI can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. In general, unused I/O banks should have their corresponding VCCIX pins tied to GND. If an output pad is terminated to ground through any resistor and if the corresponding VCCIX is left floating, then the leakage current to ground is ~ 0uA. However, if an output pad is terminated to ground through any resistor and the corresponding VCCIX grounded, then the leakage current to ground is ~ 3 uA. For unused banks the aforementioned behavior is to be taken into account while deciding if it's better to float VCCIX of unused bank or tie it to GND.

VMVx **I/O Supply Voltage (quiet)**

Quiet supply voltage to the input buffers of each I/O bank. *x* is the bank number. Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks. This minimizes the noise transfer within the package and improves input signal integrity. Each bank must have at least one VMV connection, and no VMV should be left unconnected. All I/Os in a bank run off the same VMVx supply. VMV is used to provide a quiet supply voltage to the input buffers of each I/O bank. VMVx can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VMV pins tied to GND. VMV and VCCI should be at the same voltage within a given I/O bank. Used VMV pins must be connected to the corresponding VCCI pins of the same bank (i.e., VMV0 to VCCIB0, VMV1 to VCCIB1, etc.).

VCCPLA/B/C/D/E/F **PLL Supply Voltage**

Supply voltage to analog PLL, nominally 1.5 V.

When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground. Microsemi recommends tying VCCPLx to VCC and using proper filtering circuits to decouple VCC noise from the PLLs. Refer to the PLL Power Supply Decoupling section of the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for a complete board solution for the PLL analog power supply and ground.

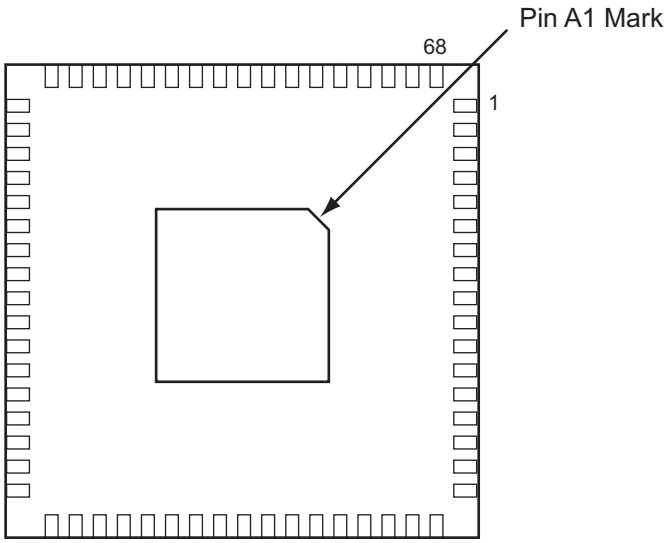
There is one VCCPLF pin on ProASIC3 devices.

VCOMPLA/B/C/D/E/F PLL Ground

Ground to analog PLL power supplies. When the PLLs are not used, the Designer place-and-route tool automatically disables the unused PLLs to lower power consumption. The user should tie unused VCCPLx and VCOMPLx pins to ground.

There is one VCOMPLF pin on ProASIC3 devices.

QN68 – Bottom View



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

QN132	
Pin Number	A3P030 Function
A1	IO01RSB1
A2	IO81RSB1
A3	NC
A4	IO80RSB1
A5	GEC0/IO77RSB1
A6	NC
A7	GEB0/IO75RSB1
A8	IO73RSB1
A9	NC
A10	VCC
A11	IO71RSB1
A12	IO68RSB1
A13	IO63RSB1
A14	IO60RSB1
A15	NC
A16	IO59RSB1
A17	IO57RSB1
A18	VCC
A19	IO54RSB1
A20	IO52RSB1
A21	IO49RSB1
A22	IO48RSB1
A23	IO47RSB1
A24	TDI
A25	TRST
A26	IO44RSB0
A27	NC
A28	IO43RSB0
A29	IO42RSB0
A30	IO40RSB0
A31	IO39RSB0
A32	GDC0/IO36RSB0
A33	NC
A34	VCC
A35	IO34RSB0
A36	IO31RSB0

QN132	
Pin Number	A3P030 Function
A37	IO26RSB0
A38	IO23RSB0
A39	NC
A40	IO22RSB0
A41	IO20RSB0
A42	IO18RSB0
A43	VCC
A44	IO15RSB0
A45	IO12RSB0
A46	IO10RSB0
A47	IO09RSB0
A48	IO06RSB0
B1	IO02RSB1
B2	IO82RSB1
B3	GND
B4	IO79RSB1
B5	NC
B6	GND
B7	IO74RSB1
B8	NC
B9	GND
B10	IO70RSB1
B11	IO67RSB1
B12	IO64RSB1
B13	IO61RSB1
B14	GND
B15	IO58RSB1
B16	IO56RSB1
B17	GND
B18	IO53RSB1
B19	IO50RSB1
B20	GND
B21	IO46RSB1
B22	TMS
B23	TDO
B24	IO45RSB0

QN132	
Pin Number	A3P030 Function
B25	GND
B26	NC
B27	IO41RSB0
B28	GND
B29	GDA0/IO37RSB0
B30	NC
B31	GND
B32	IO33RSB0
B33	IO30RSB0
B34	IO27RSB0
B35	IO24RSB0
B36	GND
B37	IO21RSB0
B38	IO19RSB0
B39	GND
B40	IO16RSB0
B41	IO13RSB0
B42	GND
B43	IO08RSB0
B44	IO05RSB0
C1	IO03RSB1
C2	IO00RSB1
C3	NC
C4	IO78RSB1
C5	GEA0/IO76RSB1
C6	NC
C7	NC
C8	VCCIB1
C9	IO69RSB1
C10	IO66RSB1
C11	IO65RSB1
C12	IO62RSB1
C13	NC
C14	NC
C15	IO55RSB1
C16	VCCIB1

QN132	
Pin Number	**A3P030 Function**
C17	IO51RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO38RSB0
C27	NC
C28	VCCIB0
C29	IO32RSB0
C30	IO29RSB0
C31	IO28RSB0
C32	IO25RSB0
C33	NC
C34	NC
C35	VCCIB0
C36	IO17RSB0
C37	IO14RSB0
C38	IO11RSB0
C39	IO07RSB0
C40	IO04RSB0
D1	GND
D2	GND
D3	GND
D4	GND

PQ208	
Pin Number	A3P1000 Function
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1

PQ208	
Pin Number	A3P1000 Function
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

PQ208	
Pin Number	A3P1000 Function
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG144	
Pin Number	**A3P060 Function**
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	**A3P1000 Function**
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

FG256	
Pin Number	**A3P250 Function**
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

FG256	
Pin Number	**A3P250 Function**
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P600 Function
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0

FG484	
Pin Number	A3P600 Function
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3

FG484	
Pin Number	A3P600 Function
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1

FG484	
Pin Number	**A3P600 Function**
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2

FG484	
Pin Number	**A3P600 Function**
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND

Revision	Changes	Page
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-2
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).	2-90
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933).	2-31
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 11 (March 2012)	Note indicating that A3P015 is not recommended for new designs has been added. The "Devices Not Recommended For New Designs" section is new (SAR 36760).	I to IV
	The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687).	NA
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide* (SAR 34734).	2-12
	Figure 2-4 • Input Buffer Timing Model and Delays (Example) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34883).	2-32
	Added values for minimum pulse width and removed the FRMAX row from Table 2-107 through Table 2-114 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269).	2-85

Revision	Changes	Page
v2.0 (April 2007)	In the "Packaging Tables", Ambient was deleted.	ii
	The timing characteristics tables were updated.	N/A
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-11 • ProASIC3 CCC/PLL Specification was updated.	2-29
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	PCI-X 3.3 V was added to Table 2-11 • VCCI Voltages and Compatible Standards.	2-29
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	V_{JTAG} was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1.	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951.	3-5
	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-6
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated.	3-17 to 3-17