Microchip Technology - A3P400-2FG144I Datasheet

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	97
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p400-2fg144i

Table 2-33 • I/O Short Currents IOSH/IOSL
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range[2]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-52 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.60	11.14	0.04	1.52	0.43	11.14	9.54	3.51	3.61	14.53	12.94	ns
		–1	0.51	9.48	0.04	1.29	0.36	9.48	8.12	2.99	3.07	12.36	11.00	ns
		–2	0.45	8.32	0.03	1.14	0.32	8.32	7.13	2.62	2.70	10.85	9.66	ns
100 µA	4 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 µA	6 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		–1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		–2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 µA	8 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
100 µA	16 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		–1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		–2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-62 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	–1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	–2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	–1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	–2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-63 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	–2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	–1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	–2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-66 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA[3]	Max mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-67 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA[3]	Max mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	44	35	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-68 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

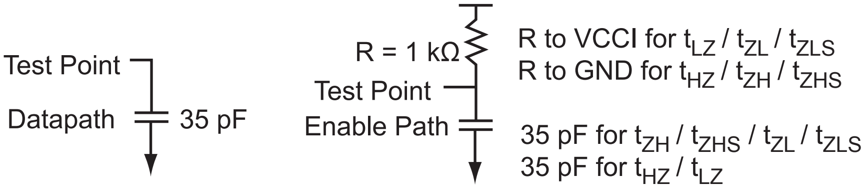


Figure 2-9 • **AC Loading**

Table 2-69 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	35

Note: **Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.*

***Table 2-93* • Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

***Table 2-94* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: _*Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points._

Timing Characteristics

***Table 2-95* • LVPECL**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.80	0.04	1.40	ns
–1	0.56	1.53	0.04	1.19	ns
–2	0.49	1.34	0.03	1.05	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Output Register

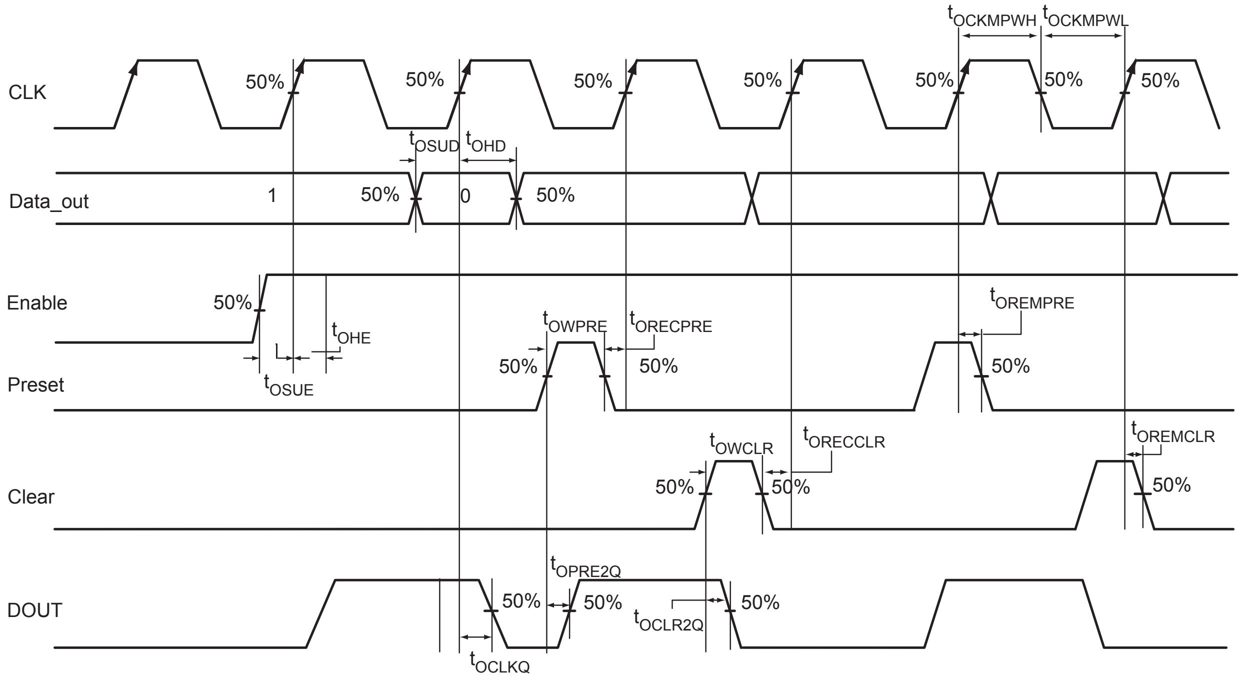


Figure 2-18 • **Output Register Timing Diagram**

Timing Characteristics

Table 2-99 • **Output Data Register Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

FIFO

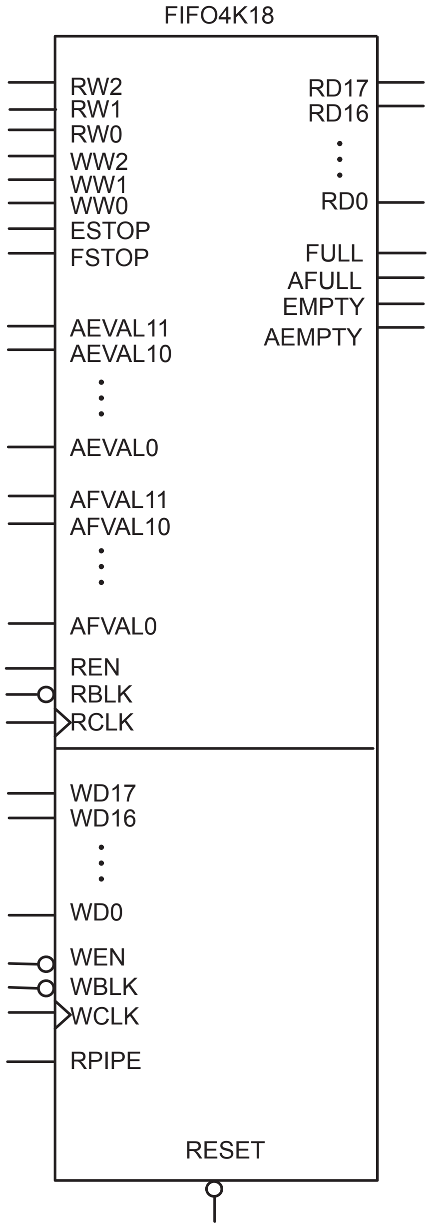


***Figure 2-36* • FIFO Model**

mode is not used in the design, the FF pin is available as a regular I/O. For IGLOOe, ProASIC3EL, and RT ProASIC3 only, the FF pin can be configured as a Schmitt trigger input.

When Flash*Freeze mode is used, the FF pin must not be left floating to avoid accidentally entering Flash*Freeze mode. While in Flash*Freeze mode, the Flash*Freeze pin should be constantly asserted.

The Flash*Freeze pin can be used with any single-ended I/O standard supported by the I/O bank in which the pin is located, and input signal levels compatible with the I/O standard selected. The FF pin should be treated as a sensitive asynchronous signal. When defining pin placement and board layout, simultaneously switching outputs (SSOs) and their effects on sensitive asynchronous pins must be considered.

Unused FF or I/O pins are tristated with weak pull-up. This default configuration applies to both Flash*Freeze mode and normal operation mode. No user intervention is required.

JTAG Pins

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the part must be supplied to allow JTAG signals to transition the device. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

TCK Test Clock

Test clock input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, Microsemi recommends tying off TCK to GND through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 1 for more information.

***Table 1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance
3.3 V	200 Ω –1 kΩ
2.5 V	200 Ω –1 kΩ
1.8 V	500 Ω –1 kΩ
1.5 V	500 Ω –1 kΩ

Notes:

1. *Equivalent parallel resistance if more than one device is on the JTAG chain*
2. *The TCK pin can be pulled up/down.*
3. *The TRST pin is pulled down.*

TDI Test Data Input

Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.

TDO Test Data Output

Serial output for JTAG boundary scan, ISP, and UJTAG usage.

TMS Test Mode Select

The TMS pin controls the use of the IEEE 1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin.

TRST Boundary Scan Reset Pin

The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the test access port (TAP) is held in reset mode. The resistor values must be chosen from Table 1 and must satisfy the parallel resistance value requirement. The values in Table 1 correspond to the resistor recommended when a single device is used, and the equivalent parallel resistor when multiple devices are connected via a JTAG chain.

QN48	
Pin Number	A3P030 Function
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

QN132	
Pin Number	**A3P125 Function**
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

CS121	
Pin Number	**A3P060 Function**
A1	GNDQ
A2	IO01RSB0
A3	GAA1/IO03RSB0
A4	GAC1/IO07RSB0
A5	IO15RSB0
A6	IO13RSB0
A7	IO17RSB0
A8	GBB1/IO22RSB0
A9	GBA1/IO24RSB0
A10	GNDQ
A11	VMV0
B1	GAA2/IO95RSB1
B2	IO00RSB0
B3	GAA0/IO02RSB0
B4	GAC0/IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO16RSB0
B8	GBC1/IO20RSB0
B9	GBB0/IO21RSB0
B10	GBB2/IO27RSB0
B11	GBA2/IO25RSB0
C1	IO89RSB1
C2	GAC2/IO91RSB1
C3	GAB1/IO05RSB0
C4	GAB0/IO04RSB0
C5	IO09RSB0
C6	IO14RSB0
C7	GBA0/IO23RSB0
C8	GBC0/IO19RSB0
C9	IO26RSB0
C10	IO28RSB0
C11	GBC2/IO29RSB0
D1	IO88RSB1
D2	IO90RSB1
D3	GAB2/IO93RSB1

CS121	
Pin Number	**A3P060 Function**
D4	IO10RSB0
D5	IO11RSB0
D6	IO18RSB0
D7	IO32RSB0
D8	IO31RSB0
D9	GCA2/IO41RSB0
D10	IO30RSB0
D11	IO33RSB0
E1	IO87RSB1
E2	GFC0/IO85RSB1
E3	IO92RSB1
E4	IO94RSB1
E5	VCC
E6	VCCIB0
E7	GND
E8	GCC0/IO36RSB0
E9	IO34RSB0
E10	GCB1/IO37RSB0
E11	GCC1/IO35RSB0
F1	VCOMPLF
F2	GFB0/IO83RSB1
F3	GFA0/IO82RSB1
F4	GFC1/IO86RSB1
F5	VCCIB1
F6	VCC
F7	VCCIB0
F8	GCB2/IO42RSB0
F9	GCC2/IO43RSB0
F10	GCB0/IO38RSB0
F11	GCA1/IO39RSB0
G1	VCCPLF
G2	GFB2/IO79RSB1
G3	GFA1/IO81RSB1
G4	GFB1/IO84RSB1
G5	GND
G6	VCCIB1

CS121	
Pin Number	**A3P060 Function**
G7	VCC
G8	GDC0/IO46RSB0
G9	GDA1/IO49RSB0
G10	GDB0/IO48RSB0
G11	GCA0/IO40RSB0
H1	IO75RSB1
H2	IO76RSB1
H3	GFC2/IO78RSB1
H4	GFA2/IO80RSB1
H5	IO77RSB1
H6	GEC2/IO66RSB1
H7	IO54RSB1
H8	GDC2/IO53RSB1
H9	VJTAG
H10	TRST
H11	IO44RSB0
J1	GEC1/IO74RSB1
J2	GEC0/IO73RSB1
J3	GEB1/IO72RSB1
J4	GEA0/IO69RSB1
J5	GEB2/IO67RSB1
J6	IO62RSB1
J7	GDA2/IO51RSB1
J8	GDB2/IO52RSB1
J9	TDI
J10	TDO
J11	GDC1/IO45RSB0
K1	GEB0/IO71RSB1
K2	GEA1/IO70RSB1
K3	GEA2/IO68RSB1
K4	IO64RSB1
K5	IO60RSB1
K6	IO59RSB1
K7	IO56RSB1
K8	TCK
K9	TMS

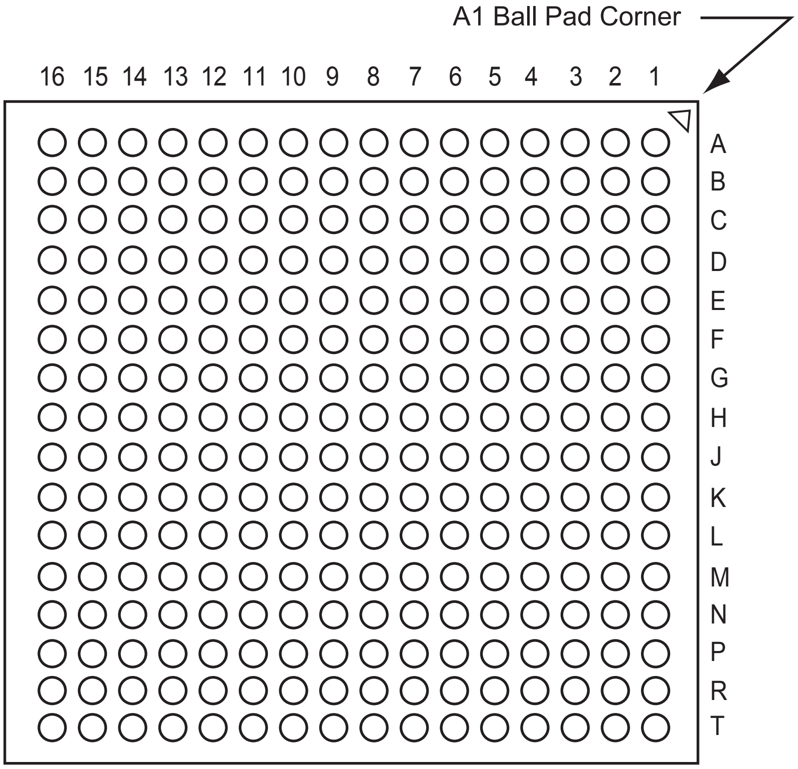
CS121	
Pin Number	**A3P060 Function**
K10	VPUMP
K11	GDB1/IO47RSB0
L1	VMV1
L2	GNDQ
L3	IO65RSB1
L4	IO63RSB1
L5	IO61RSB1
L6	IO58RSB1
L7	IO57RSB1
L8	IO55RSB1
L9	GNDQ
L10	GDA0/IO50RSB0
L11	VMV1

VQ100	
Pin Number	**A3P030 Function**
1	GND
2	IO82RSB1
3	IO81RSB1
4	IO80RSB1
5	IO79RSB1
6	IO78RSB1
7	IO77RSB1
8	IO76RSB1
9	GND
10	IO75RSB1
11	IO74RSB1
12	GEC0/IO73RSB1
13	GEA0/IO72RSB1
14	GEB0/IO71RSB1
15	IO70RSB1
16	IO69RSB1
17	VCC
18	VCCIB1
19	IO68RSB1
20	IO67RSB1
21	IO66RSB1
22	IO65RSB1
23	IO64RSB1
24	IO63RSB1
25	IO62RSB1
26	IO61RSB1
27	IO60RSB1
28	IO59RSB1
29	IO58RSB1
30	IO57RSB1
31	IO56RSB1
32	IO55RSB1
33	IO54RSB1
34	IO53RSB1
35	IO52RSB1
36	IO51RSB1
37	VCC
38	GND
39	VCCIB1
40	IO49RSB1
41	IO47RSB1
42	IO46RSB1
43	IO45RSB1
44	IO44RSB1
45	IO43RSB1
46	IO42RSB1
47	TCK
48	TDI
49	TMS
50	NC
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	IO41RSB0
58	IO40RSB0
59	IO39RSB0
60	IO38RSB0
61	IO37RSB0
62	IO36RSB0
63	GDB0/IO34RSB0
64	GDA0/IO33RSB0
65	GDC0/IO32RSB0
66	VCCIB0
67	GND
68	VCC
69	IO31RSB0
70	IO30RSB0
71	IO29RSB0
72	IO28RSB0
73	IO27RSB0
74	IO26RSB0
75	IO25RSB0
76	IO24RSB0
77	IO23RSB0
78	IO22RSB0
79	IO21RSB0
80	IO20RSB0
81	IO19RSB0
82	IO18RSB0
83	IO17RSB0
84	IO16RSB0
85	IO15RSB0
86	IO14RSB0
87	VCCIB0
88	GND
89	VCC
90	IO12RSB0
91	IO10RSB0
92	IO08RSB0
93	IO07RSB0
94	IO06RSB0
95	IO05RSB0
96	IO04RSB0
97	IO03RSB0
98	IO02RSB0
99	IO01RSB0
100	IO00RSB0

TQ144	
Pin Number	**A3P125 Function**
1	GAA2/IO67RSB1
2	IO68RSB1
3	GAB2/IO69RSB1
4	IO132RSB1
5	GAC2/IO131RSB1
6	IO130RSB1
7	IO129RSB1
8	IO128RSB1
9	VCC
10	GND
11	VCCIB1
12	IO127RSB1
13	GFC1/IO126RSB1
14	GFC0/IO125RSB1
15	GFB1/IO124RSB1
16	GFB0/IO123RSB1
17	VCOMPLF
18	GFA0/IO122RSB1
19	VCCPLF
20	GFA1/IO121RSB1
21	GFA2/IO120RSB1
22	GFB2/IO119RSB1
23	GFC2/IO118RSB1
24	IO117RSB1
25	IO116RSB1
26	IO115RSB1
27	GND
28	VCCIB1
29	GEC1/IO112RSB1
30	GEC0/IO111RSB1
31	GEB1/IO110RSB1
32	GEB0/IO109RSB1
33	GEA1/IO108RSB1
34	GEA0/IO107RSB1
35	VMV1
36	GNDQ
37	NC
38	GEA2/IO106RSB1
39	GEB2/IO105RSB1
40	GEC2/IO104RSB1
41	IO103RSB1
42	IO102RSB1
43	IO101RSB1
44	IO100RSB1
45	VCC
46	GND
47	VCCIB1
48	IO99RSB1
49	IO97RSB1
50	IO95RSB1
51	IO93RSB1
52	IO92RSB1
53	IO90RSB1
54	IO88RSB1
55	IO86RSB1
56	IO84RSB1
57	IO83RSB1
58	IO82RSB1
59	IO81RSB1
60	IO80RSB1
61	IO79RSB1
62	VCC
63	GND
64	VCCIB1
65	GDC2/IO72RSB1
66	GDB2/IO71RSB1
67	GDA2/IO70RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1
73	VPUMP
74	NC
75	TDO
76	TRST
77	VJTAG
78	GDA0/IO66RSB0
79	GDB0/IO64RSB0
80	GDB1/IO63RSB0
81	VCCIB0
82	GND
83	IO60RSB0
84	GCC2/IO59RSB0
85	GCB2/IO58RSB0
86	GCA2/IO57RSB0
87	GCA0/IO56RSB0
88	GCA1/IO55RSB0
89	GCB0/IO54RSB0
90	GCB1/IO53RSB0
91	GCC0/IO52RSB0
92	GCC1/IO51RSB0
93	IO50RSB0
94	IO49RSB0
95	NC
96	NC
97	NC
98	VCCIB0
99	GND
100	VCC
101	IO47RSB0
102	GBC2/IO45RSB0
103	IO44RSB0
104	GBB2/IO43RSB0
105	IO42RSB0
106	GBA2/IO41RSB0
107	VMV0
108	GNDQ

FG144	
Pin Number	**A3P250 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO29RSB0
A8	VCC
A9	IO33RSB0
A10	GBA0/IO39RSB0
A11	GBA1/IO40RSB0
A12	GNDQ
B1	GAB2/IO117UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO22RSB0
B8	IO30RSB0
B9	GBB0/IO37RSB0
B10	GBB1/IO38RSB0
B11	GND
B12	VMV1
C1	IO117VDB3
C2	GFA2/IO107PPB3
C3	GAC2/IO116UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO24RSB0
C8	IO31RSB0
C9	IO34RSB0
C10	GBA2/IO41PDB1
C11	IO41NDB1
C12	GBC2/IO43PPB1
D1	IO112NDB3
D2	IO112PDB3
D3	IO116VDB3
D4	GAA2/IO118UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO35RSB0
D8	GBC1/IO36RSB0
D9	GBB2/IO42PDB1
D10	IO42NDB1
D11	IO43NPB1
D12	GCB1/IO49PPB1
E1	VCC
E2	GFC0/IO110NDB3
E3	GFC1/IO110PDB3
E4	VCCIB3
E5	IO118VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO48PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO50NDB1
E12	IO51NDB1
F1	GFB0/IO109NPB3
F2	VCOMPLF
F3	GFB1/IO109PPB3
F4	IO107NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO48NDB1
F9	GCB0/IO49NPB1
F10	GND
F11	GCA1/IO50PDB1
F12	GCA2/IO51PDB1
G1	GFA1/IO108PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO108NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO58UPB1
G9	IO53NDB1
G10	GCC2/IO53PDB1
G11	IO52NDB1
G12	GCB2/IO52PDB1
H1	VCC
H2	GFB2/IO106PDB3
H3	GFC2/IO105PSB3
H4	GEC1/IO100PDB3
H5	VCC
H6	IO79RSB2
H7	IO65RSB2
H8	GDB2/IO62RSB2
H9	GDC0/IO58VPB1
H10	VCCIB1
H11	IO54PSB1
H12	VCC
J1	GEB1/IO99PDB3
J2	IO106NDB3
J3	VCCIB3
J4	GEC0/IO100NDB3
J5	IO88RSB2
J6	IO81RSB2
J7	VCC
J8	TCK
J9	GDA2/IO61RSB2
J10	TDO
J11	GDA1/IO60UDB1
J12	GDB1/IO59UDB1

FG256 – Bottom View



Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the ProASIC3 datasheet.

Revision	Changes	Page
Revision 18 (March 2016)	Updated 3.3 V DC supply voltage's maximum Commercial and Industrial values from 3.3 V to 3.6 V in Table 2-2 (SAR 72693).	2-2
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833).	NA
Revision 17 (June 2015)	Removed PQFP embedded heat spreader info. from Table 2-5 (SAR 52320).	2-6
	Updated "VCCIBx I/O Supply Voltage" (SAR 43323).	3-1
Revision 16 (December 2014)	Updated "ProASIC3 Ordering Information". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079). Added Note "Only devices with package size greater than or equal to 5x5 are supported".	1-IV
	Updated Table Note (2) in Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature so that the Table Note is not applicable for Maximum Storage Temperature T_{STG} (SAR 54297).	2-3
	Added values for Drive strength 2 mA in Table 2-41 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, Table 2-42 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew, Table 2-43 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew, and Table 2-44 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew (SAR 57184).	2-34, 2-35, 2-36, 2-37
	Added Figure 2-1 • High-Temperature Data Retention (HTR) (SAR 45466).	2-3
	Updates made to maintain the style and consistency of the document.	NA
Revision 15 (July 2014)	Added corner pad table note (3) to "QN132 – Bottom View" (SAR 47442).	4-6
	Ambient temperature removed in Table 2-2, table notes and "ProASIC3 Ordering Information" figure were modified (SAR 48343).	2-2 1-IV
	Other updates were made to maintain the style and consistency of the datasheet.	NA
Revision 14 (April 2014)	Note added for the discontinuance of QN132 package to the following tables and section: "ProASIC3 Devices", "I/Os Per Package 1", "ProASIC3 FPGAs Package Sizes Dimensions" and "QN132 – Bottom View" section (SAR 55118).	I, III, 4-6

Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21

Revision	Changes	Page
Advance v0.6 (continued)	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	The "Introduction" of the "Advanced I/Os" section was updated.	2-28
	The "I/O Banks" section is new. This section explains the following types of I/Os: Advanced Standard+ Standard Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above.	2-29
	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards	2-29
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-32
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-35
	Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices.	2-64
	The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated.	2-64
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-41
	A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected).	2-30
	Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications	2-45
	Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device)	2-83
	Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated.	2-84
	Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated.	2-84
	The "x" was updated in the "User I/O Naming Convention" section.	2-48
	The "VCC Core Supply Voltage" pin description was updated.	2-50
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-50
	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-50
	The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-50
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51