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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 55296 |
| Number of I/O | 151 |
| Number of Gates | 400000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | -40°C ~ 100°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p400-2pqg208i |

## User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

## SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

## PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

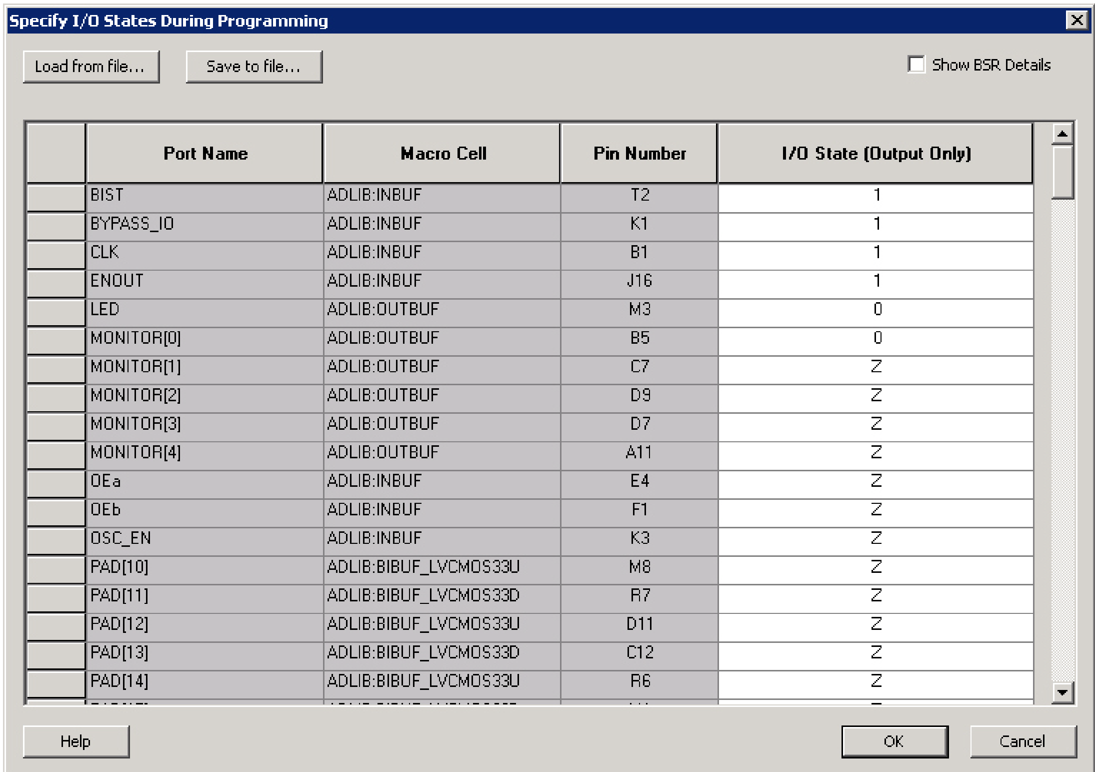
All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

0 – I/O is set to drive out logic Low

Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

Z -Tristate: I/O is tristated




| Port Name | Macro Cell | Pin Number | I/O State (Output Only) |
|---|---|---|---|
| BIST | ADLIB:INBUF | T2 | 1 |
| BYPASS_IO | ADLIB:INBUF | K1 | 1 |
| CLK | ADLIB:INBUF | B1 | 1 |
| ENOUT | ADLIB:INBUF | J16 | 1 |
| LED | ADLIB:OUTBUF | M3 | 0 |
| MONITOR[0] | ADLIB:OUTBUF | B5 | 0 |
| MONITOR[1] | ADLIB:OUTBUF | C7 | Z |
| MONITOR[2] | ADLIB:OUTBUF | D9 | Z |
| MONITOR[3] | ADLIB:OUTBUF | D7 | Z |
| MONITOR[4] | ADLIB:OUTBUF | A11 | Z |
| OEa | ADLIB:INBUF | E4 | Z |
| OEb | ADLIB:INBUF | F1 | Z |
| OSC_EN | ADLIB:INBUF | K3 | Z |
| PAD[10] | ADLIB:BIBUF_LVCMOS33U | M8 | Z |
| PAD[11] | ADLIB:BIBUF_LVCMOS33D | R7 | Z |
| PAD[12] | ADLIB:BIBUF_LVCMOS33U | D11 | Z |
| PAD[13] | ADLIB:BIBUF_LVCMOS33D | C12 | Z |
| PAD[14] | ADLIB:BIBUF_LVCMOS33U | R6 | Z |

***Figure 1-4 •*** **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

***Table 2-2 •*** **Recommended Operating Conditions [1]**

| Symbol | Parameters [1] | | Commercial | Industrial | Units |
|---|---|---|---|---|---|
| $T_J$ | Junction temperature | | 0 to 85[2] | -40 to 100[2] | °C |
| VCC[3] | 1.5 V DC core supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VJTAG | JTAG DC voltage | | 1.4 to 3.6 | 1.4 to 3.6 | V |
| VPUMP | Programming voltage | Programming Mode | 3.15 to 3.45 | 3.15 to 3.45 | V |
| | | Operation [4] | 0 to 3.6 | 0 to 3.6 | V |
| VCCPLL | Analog power supply (PLL) | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| VCCI and VMV [5] | 1.5 V DC supply voltage | | 1.425 to 1.575 | 1.425 to 1.575 | V |
| | 1.8 V DC supply voltage | | 1.7 to 1.9 | 1.7 to 1.9 | V |
| | 2.5 V DC supply voltage | | 2.3 to 2.7 | 2.3 to 2.7 | V |
| | 3.3 V DC supply voltage | | 3.0 to 3.6 | 3.0 to 3.6 | V |
| | 3.3 V wide range DC supply voltage [6] | | 2.7 to 3.6 | 2.7 to 3.6 | V |
| | LVDS/B-LVDS/M-LVDS differential I/O | | 2.375 to 2.625 | 2.375 to 2.625 | V |
| | LVPECL differential I/O | | 3.0 to 3.6 | 3.0 to 3.6 | V |

*Notes:*

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero® System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.*
4. *VPUMP can be left floating during operation (not programming mode).*
5. *VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

## Overview of I/O Performance

### Summary of I/O DC Input and Output Levels – Default I/O Software Settings

**Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks**

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option[2] | Slew Rate | VIL | | VIH | | VOL | VOH | IOL[1] mA | IOH[1] mA |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | Min V | Max V | Min V | Max V | Max V | Min V | | |
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 12 | 12 |
| 3.3 V LVCMOS Wide Range[3] | 100 µA | 12 mA | High | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VCCI – 0.2 | 0.1 | 0.1 |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.7 | 1.7 | 2.7 | 0.7 | 1.7 | 12 | 12 |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.9 | 0.45 | VCCI – 0.45 | 12 | 12 |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | –0.3 | 0.35 * VCCI | 0.65 * VCCI | 1.6 | 0.25 * VCCI | 0.75 * VCCI | 12 | 12 |
| 3.3 V PCI | Per PCI specifications | | | | | | | | | | |
| 3.3 V PCI-X | Per PCI-X specifications | | | | | | | | | | |

*Notes:*

1. *Currents are measured at 85°C junction temperature.*
2. *3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

**Table 2-30 • I/O Output Buffer Maximum Resistances[1] Applicable to Standard I/O Banks**

| Standard | Drive Strength | $R_{PULL\text{-}DOWN}$ ($\Omega$)[2] | $R_{PULL\text{-}UP}$ ($\Omega$)[3] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 100 | 300 |
| | 4 mA | 100 | 300 |
| | 6 mA | 50 | 150 |
| | 8 mA | 50 | 150 |
| 3.3 V LVCMOS Wide Range[4] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 100 | 200 |
| | 4 mA | 100 | 200 |
| | 6 mA | 50 | 100 |
| | 8 mA | 50 | 100 |
| 1.8 V LVCMOS | 2 mA | 200 | 225 |
| | 4 mA | 100 | 112 |
| 1.5 V LVCMOS | 2 mA | 200 | 224 |

*Notes:*

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / IOLspec$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

**Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values**

| VCCI | $R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$) | | $R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$) | |
|---|---|---|---|---|
| | Min | Max | Min | Max |
| 3.3 V | 10 k | 45 k | 10 k | 45 k |
| 3.3 V (wide range I/Os) | 10 k | 45 k | 10 k | 45 k |
| 2.5 V | 11 k | 55 k | 12 k | 74 k |
| 1.8 V | 18 k | 70 k | 17 k | 110 k |
| 1.5 V | 19 k | 90 k | 19 k | 140 k |

*Notes:*

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCI_{MAX} – VOH_{spec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOL_{spec}) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

**Table 2-32 • I/O Short Currents IOSH/IOSL Applicable to Advanced I/O Banks**

| | Drive Strength | IOSL (mA)[1] | IOSH (mA)[1] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| | 16 mA | 87 | 83 |
| | 24 mA | 124 | 169 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 51 | 45 |
| | 12 mA | 74 | 91 |
| | 16 mA | 74 | 91 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| | 6 mA | 39 | 32 |
| | 8 mA | 55 | 66 |
| | 12 mA | 55 | 66 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

*Notes:*

1. $T_J = 100°C$
2. *Applicable to 3.3 V LVCMOS Wide Range. $I_{OSL}/I_{OSH}$ dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

## 3.3 V LVCMOS Wide Range

**Table 2-47 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

| 3.3 V LVCMOS Wide Range | Equiv. Software Default Drive Strength Option[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min V | Max V | Min V | Max V | Max V | Min V | µA | µA | Max mA[4] | Max mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 132 | 127 | 10 | 10 |
| 100 µA | 24 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 268 | 181 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 85°C junction temperature.*
5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
6. *Software default selection highlighted in gray.*

**Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

| 3.3 V LVCMOS Wide Range | Equiv. Software Default Drive Strength Option[1] | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL[2] | IIH[3] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | | Min V | Max V | Min V | Max V | Max V | Min V | µA | µA | Max mA[4] | Max mA[4] | µA[5] | µA[5] |
| 100 µA | 2 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 4 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 25 | 27 | 10 | 10 |
| 100 µA | 6 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 8 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 51 | 54 | 10 | 10 |
| 100 µA | 12 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |
| 100 µA | 16 mA | –0.3 | 0.8 | 2 | 3.6 | 0.2 | VDD – 0.2 | 100 | 100 | 103 | 109 | 10 | 10 |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 85°C junction temperature.*
5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
6. *Software default selection highlighted in gray.*

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### Timing Characteristics

***Table 2-60 •*** **2.5 V LVCMOS High Slew**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V**
**Applicable to Advanced I/O Banks**

| Drive Strength | Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 4 mA | Std. | 0.60 | 8.66 | 0.04 | 1.31 | 0.43 | 7.83 | 8.66 | 2.68 | 2.30 | 10.07 | 10.90 | ns |
| | –1 | 0.51 | 7.37 | 0.04 | 1.11 | 0.36 | 6.66 | 7.37 | 2.28 | 1.96 | 8.56 | 9.27 | ns |
| | –2 | 0.45 | 6.47 | 0.03 | 0.98 | 0.32 | 5.85 | 6.47 | 2.00 | 1.72 | 7.52 | 8.14 | ns |
| 6 mA | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | –1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | –2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 8 mA | Std. | 0.60 | 5.17 | 0.04 | 1.31 | 0.43 | 5.04 | 5.17 | 3.05 | 3.00 | 7.27 | 7.40 | ns |
| | –1 | 0.51 | 4.39 | 0.04 | 1.11 | 0.36 | 4.28 | 4.39 | 2.59 | 2.55 | 6.19 | 6.30 | ns |
| | –2 | 0.45 | 3.86 | 0.03 | 0.98 | 0.32 | 3.76 | 3.86 | 2.28 | 2.24 | 5.43 | 5.53 | ns |
| 12 mA | Std. | 0.60 | 3.56 | 0.04 | 1.31 | 0.43 | 3.63 | 3.43 | 3.30 | 3.44 | 5.86 | 5.67 | ns |
| | –1 | 0.51 | 3.03 | 0.04 | 1.11 | 0.36 | 3.08 | 2.92 | 2.81 | 2.92 | 4.99 | 4.82 | ns |
| | –2 | 0.45 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 16 mA | Std. | 0.60 | 3.35 | 0.04 | 1.31 | 0.43 | 3.41 | 3.06 | 3.36 | 3.55 | 5.65 | 5.30 | ns |
| | –1 | 0.51 | 2.85 | 0.04 | 1.11 | 0.36 | 2.90 | 2.60 | 2.86 | 3.02 | 4.81 | 4.51 | ns |
| | –2 | 0.45 | 2.50 | 0.03 | 0.98 | 0.32 | 2.55 | 2.29 | 2.51 | 2.65 | 4.22 | 3.96 | ns |
| 24 mA | Std. | 0.60 | 3.09 | 0.04 | 1.31 | 0.43 | 3.15 | 2.44 | 3.44 | 4.00 | 5.38 | 4.68 | ns |
| | –1 | 0.51 | 2.63 | 0.04 | 1.11 | 0.36 | 2.68 | 2.08 | 2.92 | 3.40 | 4.58 | 3.98 | ns |
| | –2 | 0.45 | 2.31 | 0.03 | 0.98 | 0.32 | 2.35 | 1.82 | 2.57 | 2.98 | 4.02 | 3.49 | ns |

*Notes:*

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Microsemi LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Microsemi LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-92.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

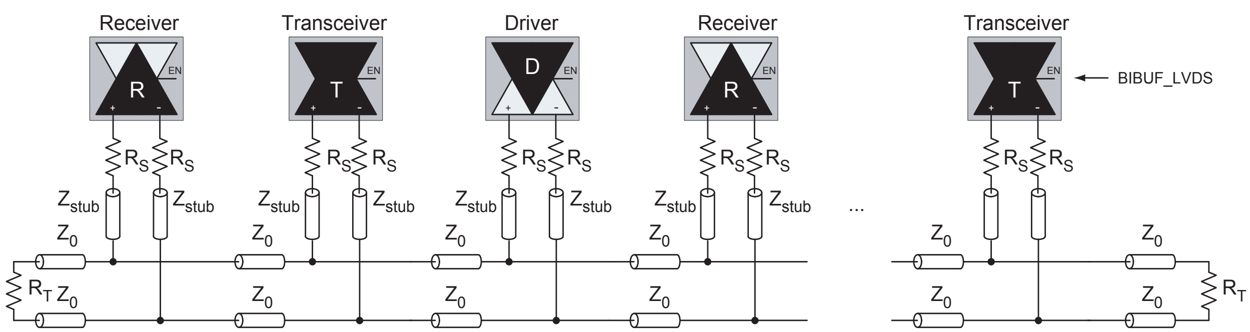


***Figure 2-13 •*** **B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

## LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

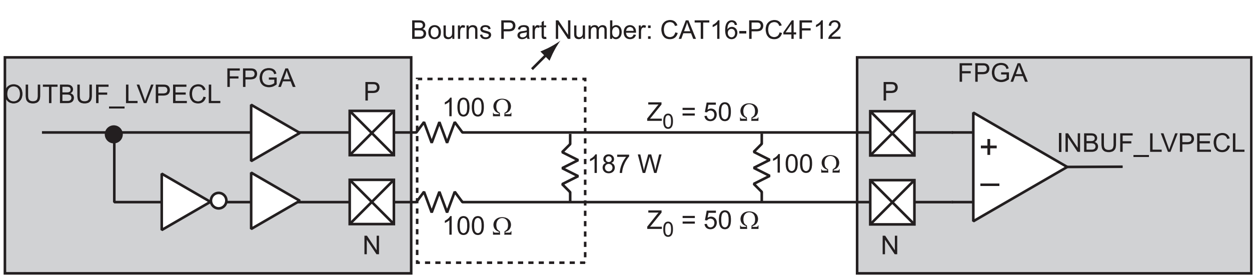


***Figure 2-14 •*** **LVPECL Circuit Diagram and Board-Level Implementation**

## Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

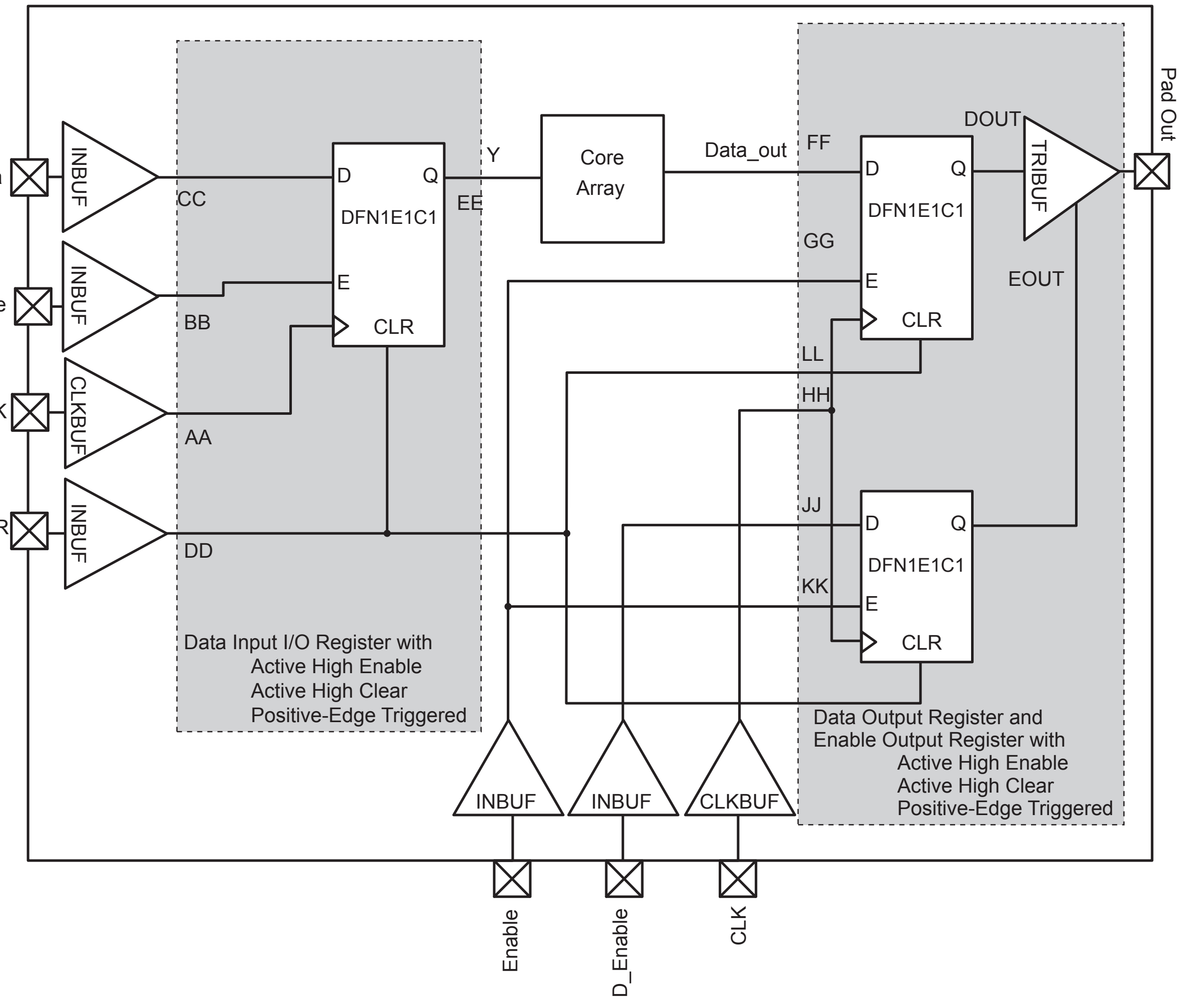


*Figure 2-16* • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

### Timing Characteristics

***Table 2-107* • A3P015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.66 | 0.81 | 0.75 | 0.92 | 0.88 | 1.08 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.67 | 0.84 | 0.76 | 0.96 | 0.89 | 1.13 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.25 | ns |

***Notes:***

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-108* • A3P030 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.67 | 0.81 | 0.76 | 0.92 | 0.89 | 1.09 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.68 | 0.85 | 0.77 | 0.97 | 0.91 | 1.14 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.24 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Waveforms

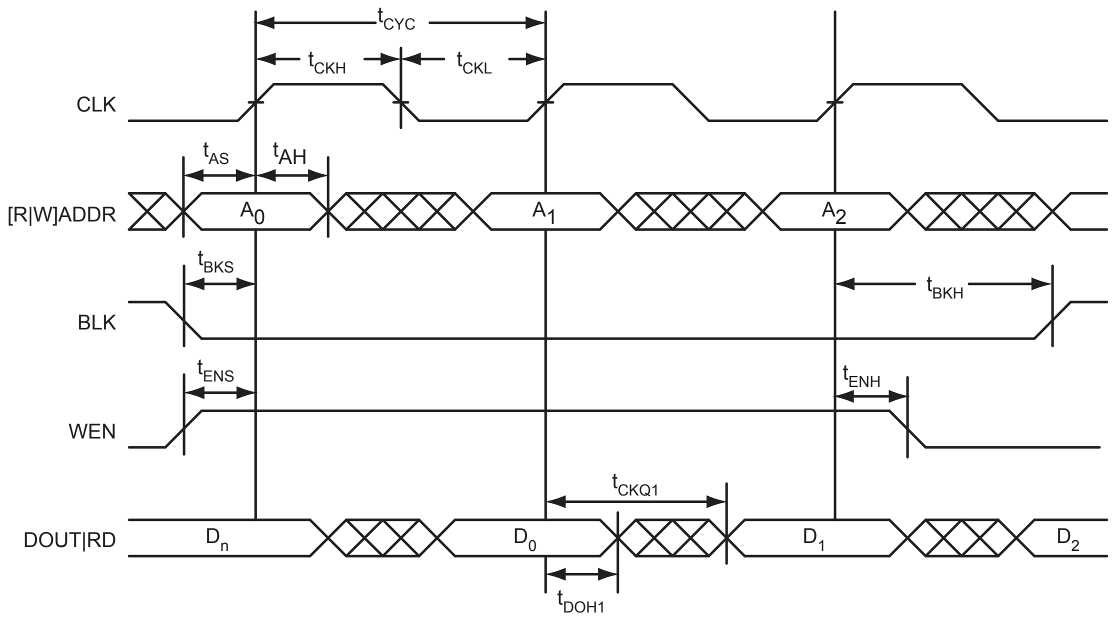


*Figure 2-31* • **RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

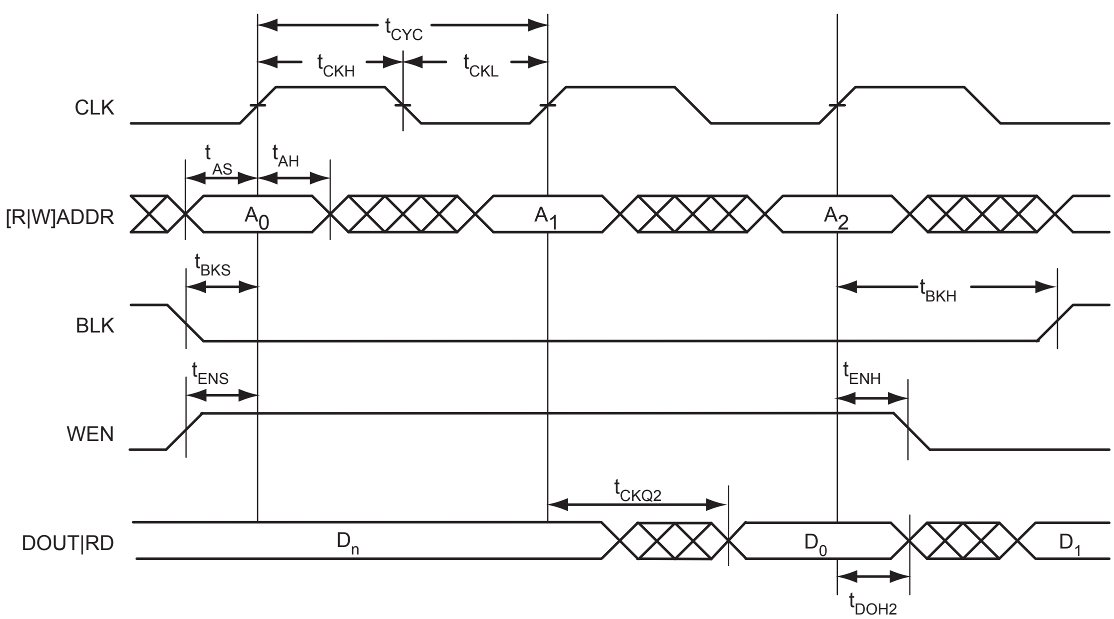


*Figure 2-32* • **RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

## *Timing Characteristics*

***Table 2-116* • RAM4K9**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{AS}$ | Address setup time | 0.25 | 0.28 | 0.33 | ns |
| $t_{AH}$ | Address hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{ENS}$ | REN, WEN setup time | 0.14 | 0.16 | 0.19 | ns |
| $t_{ENH}$ | REN, WEN hold time | 0.10 | 0.11 | 0.13 | ns |
| $t_{BKS}$ | BLK setup time | 0.23 | 0.27 | 0.31 | ns |
| $t_{BKH}$ | BLK hold time | 0.02 | 0.02 | 0.02 | ns |
| $t_{DS}$ | Input data (DIN) setup time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input data (DIN) hold time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to new data valid on DOUT (output retained, WMODE = 0) | 2.36 | 2.68 | 3.15 | ns |
| | Clock High to new data valid on DOUT (flow-through, WMODE = 1) | 1.79 | 2.03 | 2.39 | ns |
| $t_{CKQ2}$ | Clock High to new data valid on DOUT (pipelined) | 0.89 | 1.02 | 1.20 | ns |
| $t_{C2CWWL}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Closing Edge | 0.33 | 0.28 | 0.25 | ns |
| $t_{C2CWWH}$[1] | Address collision clk-to-clk delay for reliable write after write on same address—Applicable to Rising Edge | 0.30 | 0.26 | 0.23 | ns |
| $t_{C2CRWH}$[1] | Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge | 0.45 | 0.38 | 0.34 | ns |
| $t_{C2CWRH}$[1] | Address collision clk-to-clk delay for reliable write access after read on same address— Applicable to Opening Edge | 0.49 | 0.42 | 0.37 | ns |
| $t_{RSTBQ}$ | RESET Low to data out Low on DOUT (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on DOUT (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET minimum pulse width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock cycle time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum frequency | 310 | 272 | 231 | MHz |

*Notes:*

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

| CS121 | |
|---|---|
| **Pin Number** | **A3P060 Function** |
| K10 | VPUMP |
| K11 | GDB1/IO47RSB0 |
| L1 | VMV1 |
| L2 | GNDQ |
| L3 | IO65RSB1 |
| L4 | IO63RSB1 |
| L5 | IO61RSB1 |
| L6 | IO58RSB1 |
| L7 | IO57RSB1 |
| L8 | IO55RSB1 |
| L9 | GNDQ |
| L10 | GDA0/IO50RSB0 |
| L11 | VMV1 |

# PQ208 – Top View


### Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

| PQ208 | |
|---|---|
| Pin Number | A3P1000 Function |
| 109 | TRST |
| 110 | VJTAG |
| 111 | GDA0/IO113NDB1 |
| 112 | GDA1/IO113PDB1 |
| 113 | GDB0/IO112NDB1 |
| 114 | GDB1/IO112PDB1 |
| 115 | GDC0/IO111NDB1 |
| 116 | GDC1/IO111PDB1 |
| 117 | IO109NDB1 |
| 118 | IO109PDB1 |
| 119 | IO106NDB1 |
| 120 | IO106PDB1 |
| 121 | IO104PSB1 |
| 122 | GND |
| 123 | VCCIB1 |
| 124 | IO99NDB1 |
| 125 | IO99PDB1 |
| 126 | NC |
| 127 | IO96NDB1 |
| 128 | GCC2/IO96PDB1 |
| 129 | GCB2/IO95PSB1 |
| 130 | GND |
| 131 | GCA2/IO94PSB1 |
| 132 | GCA1/IO93PDB1 |
| 133 | GCA0/IO93NDB1 |
| 134 | GCB0/IO92NDB1 |
| 135 | GCB1/IO92PDB1 |
| 136 | GCC0/IO91NDB1 |
| 137 | GCC1/IO91PDB1 |
| 138 | IO88NDB1 |
| 139 | IO88PDB1 |
| 140 | VCCIB1 |
| 141 | GND |
| 142 | VCC |
| 143 | IO86PSB1 |
| 144 | IO84NDB1 |

| PQ208 | |
|---|---|
| Pin Number | A3P1000 Function |
| 145 | IO84PDB1 |
| 146 | IO82NDB1 |
| 147 | IO82PDB1 |
| 148 | IO80NDB1 |
| 149 | GBC2/IO80PDB1 |
| 150 | IO79NDB1 |
| 151 | GBB2/IO79PDB1 |
| 152 | IO78NDB1 |
| 153 | GBA2/IO78PDB1 |
| 154 | VMV1 |
| 155 | GNDQ |
| 156 | GND |
| 157 | VMV0 |
| 158 | GBA1/IO77RSB0 |
| 159 | GBA0/IO76RSB0 |
| 160 | GBB1/IO75RSB0 |
| 161 | GBB0/IO74RSB0 |
| 162 | GND |
| 163 | GBC1/IO73RSB0 |
| 164 | GBC0/IO72RSB0 |
| 165 | IO70RSB0 |
| 166 | IO67RSB0 |
| 167 | IO63RSB0 |
| 168 | IO60RSB0 |
| 169 | IO57RSB0 |
| 170 | VCCIB0 |
| 171 | VCC |
| 172 | IO54RSB0 |
| 173 | IO51RSB0 |
| 174 | IO48RSB0 |
| 175 | IO45RSB0 |
| 176 | IO42RSB0 |
| 177 | IO40RSB0 |
| 178 | GND |
| 179 | IO38RSB0 |
| 180 | IO35RSB0 |

| PQ208 | |
|---|---|
| Pin Number | A3P1000 Function |
| 181 | IO33RSB0 |
| 182 | IO31RSB0 |
| 183 | IO29RSB0 |
| 184 | IO27RSB0 |
| 185 | IO25RSB0 |
| 186 | VCCIB0 |
| 187 | VCC |
| 188 | IO22RSB0 |
| 189 | IO20RSB0 |
| 190 | IO18RSB0 |
| 191 | IO16RSB0 |
| 192 | IO15RSB0 |
| 193 | IO14RSB0 |
| 194 | IO13RSB0 |
| 195 | GND |
| 196 | IO12RSB0 |
| 197 | IO11RSB0 |
| 198 | IO10RSB0 |
| 199 | IO09RSB0 |
| 200 | VCCIB0 |
| 201 | GAC1/IO05RSB0 |
| 202 | GAC0/IO04RSB0 |
| 203 | GAB1/IO03RSB0 |
| 204 | GAB0/IO02RSB0 |
| 205 | GAA1/IO01RSB0 |
| 206 | GAA0/IO00RSB0 |
| 207 | GNDQ |
| 208 | VMV0 |

| FG144 | |
|---|---|
| Pin Number | A3P600 Function |
| A1 | GNDQ |
| A2 | VMV0 |
| A3 | GAB0/IO02RSB0 |
| A4 | GAB1/IO03RSB0 |
| A5 | IO10RSB0 |
| A6 | GND |
| A7 | IO34RSB0 |
| A8 | VCC |
| A9 | IO50RSB0 |
| A10 | GBA0/IO58RSB0 |
| A11 | GBA1/IO59RSB0 |
| A12 | GNDQ |
| B1 | GAB2/IO173PDB3 |
| B2 | GND |
| B3 | GAA0/IO00RSB0 |
| B4 | GAA1/IO01RSB0 |
| B5 | IO13RSB0 |
| B6 | IO19RSB0 |
| B7 | IO31RSB0 |
| B8 | IO39RSB0 |
| B9 | GBB0/IO56RSB0 |
| B10 | GBB1/IO57RSB0 |
| B11 | GND |
| B12 | VMV1 |
| C1 | IO173NDB3 |
| C2 | GFA2/IO161PPB3 |
| C3 | GAC2/IO172PDB3 |
| C4 | VCC |
| C5 | IO16RSB0 |
| C6 | IO25RSB0 |
| C7 | IO28RSB0 |
| C8 | IO42RSB0 |
| C9 | IO45RSB0 |
| C10 | GBA2/IO60PDB1 |
| C11 | IO60NDB1 |
| C12 | GBC2/IO62PPB1 |

| FG144 | |
|---|---|
| Pin Number | A3P600 Function |
| D1 | IO169PDB3 |
| D2 | IO169NDB3 |
| D3 | IO172NDB3 |
| D4 | GAA2/IO174PPB3 |
| D5 | GAC0/IO04RSB0 |
| D6 | GAC1/IO05RSB0 |
| D7 | GBC0/IO54RSB0 |
| D8 | GBC1/IO55RSB0 |
| D9 | GBB2/IO61PDB1 |
| D10 | IO61NDB1 |
| D11 | IO62NPB1 |
| D12 | GCB1/IO70PPB1 |
| E1 | VCC |
| E2 | GFC0/IO164NDB3 |
| E3 | GFC1/IO164PDB3 |
| E4 | VCCIB3 |
| E5 | IO174NPB3 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | GCC1/IO69PDB1 |
| E9 | VCCIB1 |
| E10 | VCC |
| E11 | GCA0/IO71NDB1 |
| E12 | IO72NDB1 |
| F1 | GFB0/IO163NPB3 |
| F2 | VCOMPLF |
| F3 | GFB1/IO163PPB3 |
| F4 | IO161NPB3 |
| F5 | GND |
| F6 | GND |
| F7 | GND |
| F8 | GCC0/IO69NDB1 |
| F9 | GCB0/IO70NPB1 |
| F10 | GND |
| F11 | GCA1/IO71PDB1 |
| F12 | GCA2/IO72PDB1 |

| FG144 | |
|---|---|
| Pin Number | A3P600 Function |
| G1 | GFA1/IO162PPB3 |
| G2 | GND |
| G3 | VCCPLF |
| G4 | GFA0/IO162NPB3 |
| G5 | GND |
| G6 | GND |
| G7 | GND |
| G8 | GDC1/IO86PPB1 |
| G9 | IO74NDB1 |
| G10 | GCC2/IO74PDB1 |
| G11 | IO73NDB1 |
| G12 | GCB2/IO73PDB1 |
| H1 | VCC |
| H2 | GFB2/IO160PDB3 |
| H3 | GFC2/IO159PSB3 |
| H4 | GEC1/IO146PDB3 |
| H5 | VCC |
| H6 | IO80PDB1 |
| H7 | IO80NDB1 |
| H8 | GDB2/IO90RSB2 |
| H9 | GDC0/IO86NPB1 |
| H10 | VCCIB1 |
| H11 | IO84PSB1 |
| H12 | VCC |
| J1 | GEB1/IO145PDB3 |
| J2 | IO160NDB3 |
| J3 | VCCIB3 |
| J4 | GEC0/IO146NDB3 |
| J5 | IO129RSB2 |
| J6 | IO131RSB2 |
| J7 | VCC |
| J8 | TCK |
| J9 | GDA2/IO89RSB2 |
| J10 | TDO |
| J11 | GDA1/IO88PDB1 |
| J12 | GDB1/IO87PDB1 |

| FG484 | |
|---|---|
| Pin Number | A3P600 Function |
| K19 | IO75NDB1 |
| K20 | NC |
| K21 | IO76NDB1 |
| K22 | IO76PDB1 |
| L1 | NC |
| L2 | IO155PDB3 |
| L3 | NC |
| L4 | GFB0/IO163NPB3 |
| L5 | GFA0/IO162NDB3 |
| L6 | GFB1/IO163PPB3 |
| L7 | VCOMPLF |
| L8 | GFC0/IO164NPB3 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO69NPB1 |
| L16 | GCB1/IO70PPB1 |
| L17 | GCA0/IO71NPB1 |
| L18 | IO67NPB1 |
| L19 | GCB0/IO70NPB1 |
| L20 | IO77PDB1 |
| L21 | IO77NDB1 |
| L22 | IO78NPB1 |
| M1 | NC |
| M2 | IO155NDB3 |
| M3 | IO158NPB3 |
| M4 | GFA2/IO161PPB3 |
| M5 | GFA1/IO162PDB3 |
| M6 | VCCPLF |
| M7 | IO160NDB3 |
| M8 | GFB2/IO160PDB3 |
| M9 | VCC |
| M10 | GND |

| FG484 | |
|---|---|
| Pin Number | A3P600 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO73PPB1 |
| M16 | GCA1/IO71PPB1 |
| M17 | GCC2/IO74PPB1 |
| M18 | IO80PPB1 |
| M19 | GCA2/IO72PDB1 |
| M20 | IO79PPB1 |
| M21 | IO78PPB1 |
| M22 | NC |
| N1 | IO154NDB3 |
| N2 | IO154PDB3 |
| N3 | NC |
| N4 | GFC2/IO159PDB3 |
| N5 | IO161NPB3 |
| N6 | IO156PPB3 |
| N7 | IO129RSB2 |
| N8 | VCCIB3 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB1 |
| N16 | IO73NPB1 |
| N17 | IO80NPB1 |
| N18 | IO74NPB1 |
| N19 | IO72NDB1 |
| N20 | NC |
| N21 | IO79NPB1 |
| N22 | NC |
| P1 | NC |
| P2 | IO153PDB3 |

| FG484 | |
|---|---|
| Pin Number | A3P600 Function |
| P3 | IO153NDB3 |
| P4 | IO159NDB3 |
| P5 | IO156NPB3 |
| P6 | IO151PPB3 |
| P7 | IO158PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO87NPB1 |
| P17 | IO85NDB1 |
| P18 | IO85PDB1 |
| P19 | IO84PDB1 |
| P20 | NC |
| P21 | IO81PDB1 |
| P22 | NC |
| R1 | NC |
| R2 | NC |
| R3 | VCC |
| R4 | IO150PDB3 |
| R5 | IO151NPB3 |
| R6 | IO147NPB3 |
| R7 | GEC0/IO146NPB3 |
| R8 | VMV3 |
| R9 | VCCIB2 |
| R10 | VCCIB2 |
| R11 | IO117RSB2 |
| R12 | IO110RSB2 |
| R13 | VCCIB2 |
| R14 | VCCIB2 |
| R15 | VMV2 |
| R16 | IO94RSB2 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB1 |
| AA1 | GND |
| AA2 | VCCIB3 |
| AA3 | NC |
| AA4 | IO181RSB2 |
| AA5 | IO178RSB2 |
| AA6 | IO175RSB2 |
| AA7 | IO169RSB2 |
| AA8 | IO166RSB2 |
| AA9 | IO160RSB2 |
| AA10 | IO152RSB2 |
| AA11 | IO146RSB2 |
| AA12 | IO139RSB2 |
| AA13 | IO133RSB2 |
| AA14 | NC |
| AA15 | NC |
| AA16 | IO122RSB2 |
| AA17 | IO119RSB2 |
| AA18 | IO117RSB2 |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB2 |
| AB4 | IO180RSB2 |
| AB5 | IO176RSB2 |
| AB6 | IO173RSB2 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| AB7 | IO167RSB2 |
| AB8 | IO162RSB2 |
| AB9 | IO156RSB2 |
| AB10 | IO150RSB2 |
| AB11 | IO145RSB2 |
| AB12 | IO144RSB2 |
| AB13 | IO132RSB2 |
| AB14 | IO127RSB2 |
| AB15 | IO126RSB2 |
| AB16 | IO123RSB2 |
| AB17 | IO121RSB2 |
| AB18 | IO118RSB2 |
| AB19 | NC |
| AB20 | VCCIB2 |
| AB21 | GND |
| AB22 | GND |

| Revision | Changes | Page |
|---|---|---|
| Revision 10 (continued) | "TBD" for 3.3 V LVCMOS Wide Range in Table 2-28 • I/O Output Buffer Maximum Resistances1 through Table 2-30 • I/O Output Buffer Maximum Resistances1 was replaced by "Same as regular 3.3 V" (SAR 33852). | 2-26 to 2-28 |
| | The equations in the notes for Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances were corrected (SAR 32470). | 2-28 |
| | "TBD" for 3.3 V LVCMOS Wide Range in Table 2-32 • I/O Short Currents IOSH/IOSL through Table 2-34 • I/O Short Currents IOSH/IOSL was replaced by "Same as regular 3.3 V LVCMOS" (SAR 33852). | 2-29 to 2-31 |
| | In the "3.3 V LVCMOS Wide Range" section, values were added to Table 2-47 through Table 2-49 for IOSL and IOSH, replacing "TBD" (SAR 33852). | 2-39 to 2-40 |
| | The following sentence was deleted from the "2.5 V LVCMOS" section (SAR 24916): "It uses a 5 V–tolerant input buffer and push-pull output buffer." | 2-47 |
| | The table notes were revised for Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels (SAR 33859). | 2-66 |
| | Values were added for $F_{DDRIMAX}$ and $F_{DDOMAX}$ in Table 2-102 • Input DDR Propagation Delays and Table 2-104 • Output DDR Propagation Delays (SAR 23919). | 2-78, 2-80 |
| | Table 2-115 • ProASIC3 CCC/PLL Specification was updated. A note was added to indicate that when the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available (SAR 25705). | 2-90 |
| | The following figures were deleted (SAR 29991). Reference was made to a new application note, *Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*, which covers these cases in detail (SAR 21770).<br>Figure 2-34 • Write Access after Write onto Same Address<br>Figure 2-35 • Read Access after Write onto Same Address<br>Figure 2-35 • Read Access after Write onto Same Address<br>The port names in the SRAM "Timing Waveforms", SRAM "Timing Characteristics" tables, Figure 2-39 • FIFO Reset, and the FIFO "Timing Characteristics" tables were revised to ensure consistency with the software names (SARs 29991, 30510). | 2-92, 2-94, 2-99 2-102 |
| | The "Pin Descriptions" chapter has been added (SAR 21642). | 3-1 |
| | Package names used in the "Package Pin Assignments" section were revised to match standards given in *Package Mechanical Drawings* (SAR 27395). | 4-1 |
| July 2010 | The versioning system for datasheets has been changed. Datasheets are assigned a revision number that increments each time the datasheet is revised. The "ProASIC3 Device Status" table on page IV indicates the status for each device in the device family. | N/A |