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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	55296
Number of I/O	97
Number of Gates	400000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p400-fg144i

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • **I/O Standards Supported**

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west Banks of A3P250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	✓	✓	Not supported
Standard	All banks of A3P015 and A3P030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

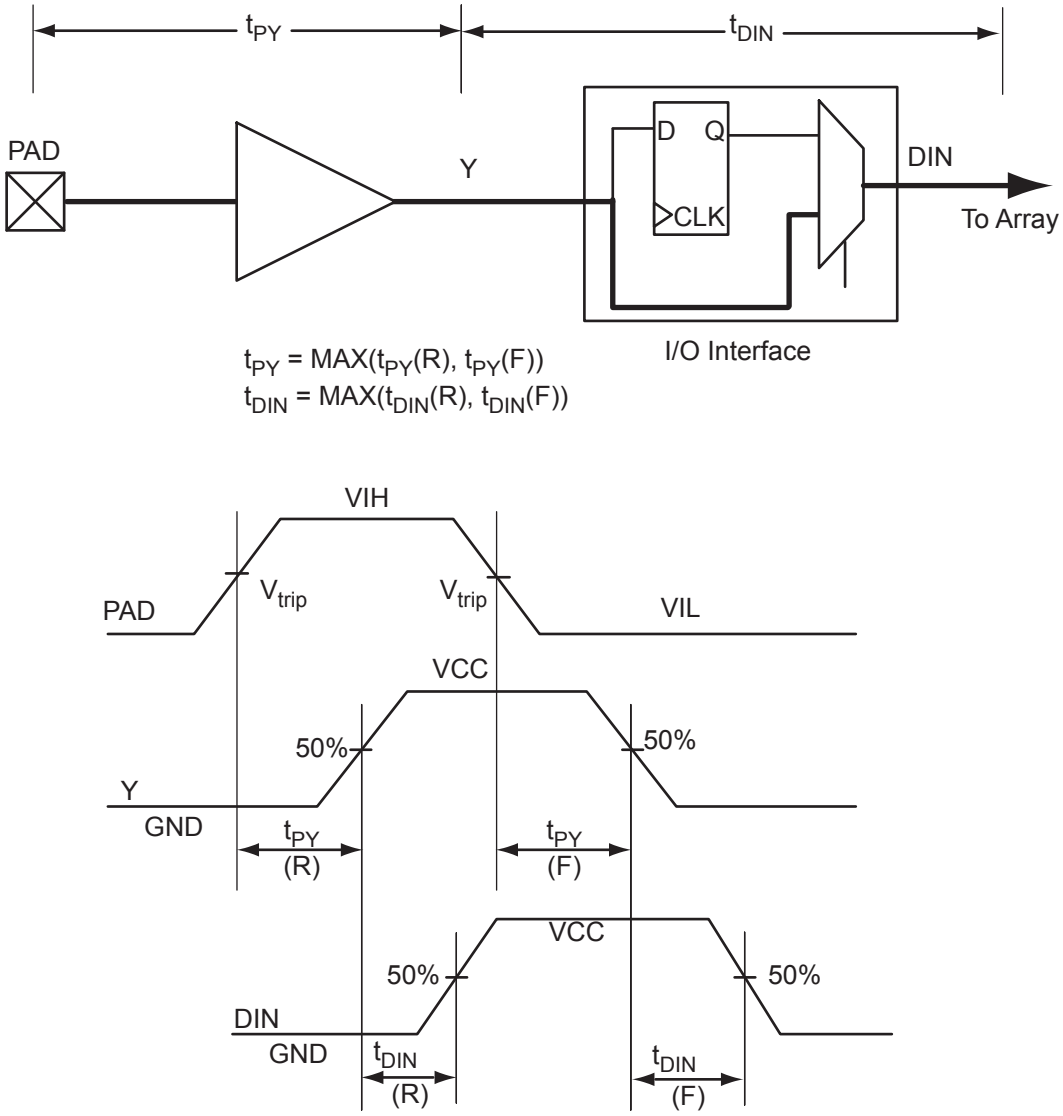


Figure 2-4 • **Input Buffer Timing Model and Delays (Example)**

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1] mA	IOH[1] mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	8 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8
1.5 V LVCMOS	4 mA	4 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	4	4
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

Table 2-23 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-34 • I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range[2]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Table 2-61 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.51	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.45	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
6 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
8 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.60	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.51	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.45	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.60	5.76	0.04	1.31	0.43	5.87	5.53	3.36	3.44	8.11	7.76	ns
	–1	0.51	4.90	0.04	1.11	0.36	4.99	4.70	2.86	2.92	6.90	6.60	ns
	–2	0.45	4.30	0.03	0.98	0.32	4.38	4.13	2.51	2.57	6.05	5.80	ns
24 mA	Std.	0.60	5.51	0.04	1.31	0.43	5.50	5.51	3.43	3.87	7.74	7.74	ns
	–1	0.51	4.68	0.04	1.11	0.36	4.68	4.68	2.92	3.29	6.58	6.59	ns
	–2	0.45	4.11	0.03	0.98	0.32	4.11	4.11	2.56	2.89	5.78	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-62 • 2.5 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	–1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	–2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	–1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	–2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-63 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	–2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	–1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	–2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

Table 2-70 • 1.8 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	–2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	–1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	–2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

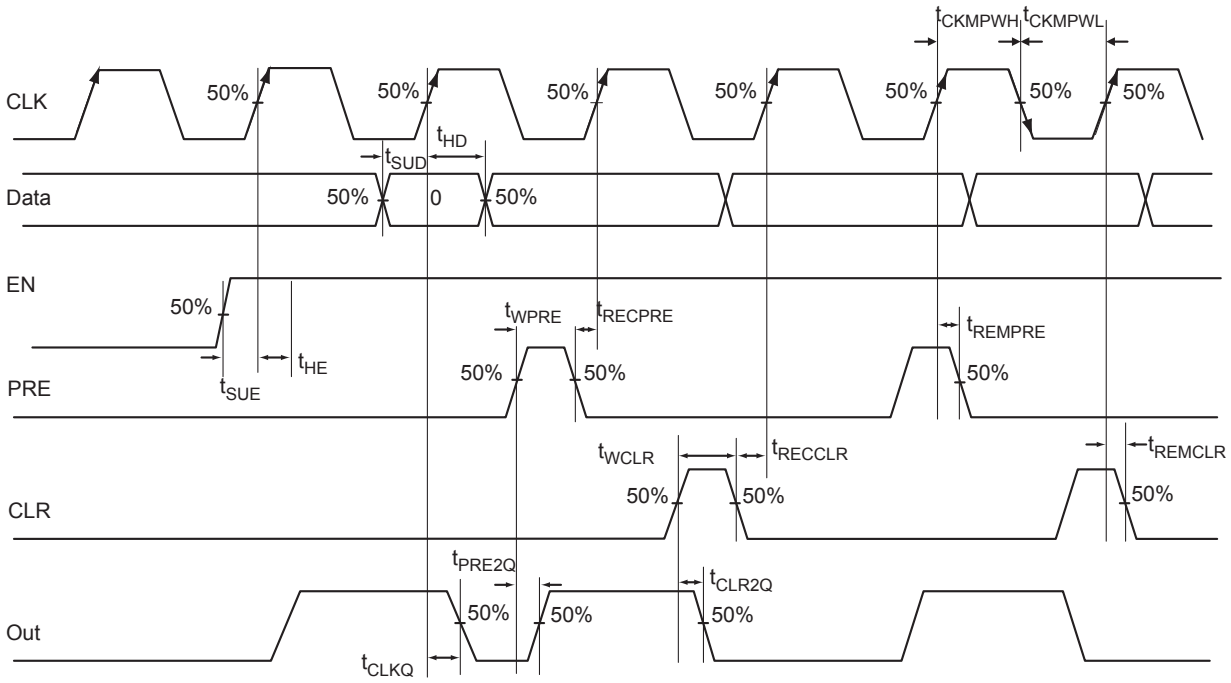


Figure 2-27 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-106 • **Register Delays**

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-113 • A3P600 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t_{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-114 • A3P1000 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-123 • A3P250 FIFO 4k×1 (continued)
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Embedded FlashROM Characteristics

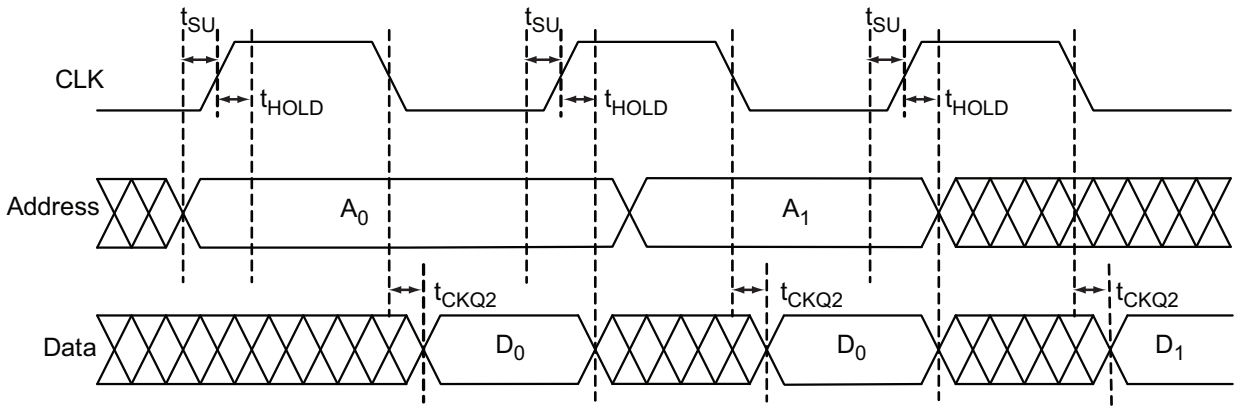


Figure 2-44 • Timing Diagram

Timing Characteristics

Table 2-124 • Embedded FlashROM Access Time

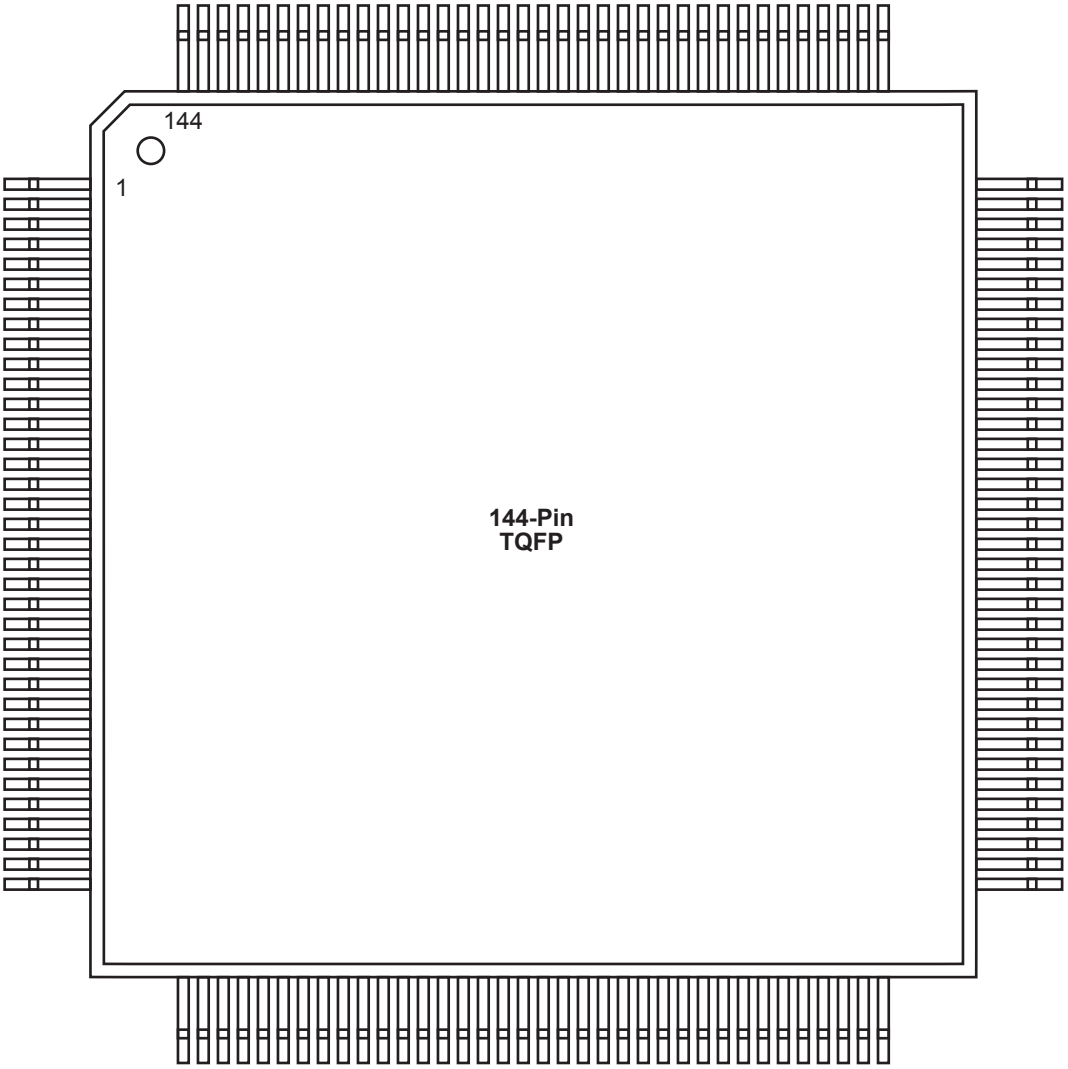
Parameter	Description	–2	–1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	21.42	24.40	28.68	ns
F_{MAX}	Maximum Clock Frequency	15	15	15	MHz

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

TQ144 – Top View



Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484	
Pin Number	A3P600 Function
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2

FG484	
Pin Number	A3P600 Function
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC

FG484	
Pin Number	A3P600 Function
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC

FG484	
Pin Number	A3P1000 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0

FG484	
Pin Number	A3P1000 Function
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

FG484	
Pin Number	A3P1000 Function
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GBA2/IO78PDB1
E19	IO81PDB1
E20	GND

Revision	Changes	Page
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient}$ = 0°C to 85°C.	2-2
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).	2-90
	Libero Integrated Design Environment (IDE) was changed to Libero System-on-Chip (SoC) throughout the document (SAR 40284). Live at Power-Up (LAPU) has been replaced with 'Instant On'.	NA
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933).	2-31
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Revision 9 (Oct 2009) Product Brief v1.3	The CS121 package was added to table under "Features and Benefits" section, the "I/Os Per Package 1" table, Table 1 • ProASIC3 FPGAs Package Sizes Dimensions, "ProASIC3 Ordering Information", and the "Temperature Grade Offerings" table.	I – IV
	"ProASIC3 Ordering Information" was revised to include the fact that some RoHS compliant packages are halogen-free.	IV
Packaging v1.5	The "CS121 – Bottom View" figure and pin table for A3P060 are new.	4-15
Revision 8 (Aug 2009) Product Brief v1.2	All references to M7 devices (CoreMP7) and speed grade –F were removed from this document.	N/A
	Table 1-1 I/O Standards supported is new.	1-7
	The I/Os with Advanced I/O Standards section was revised to add definitions of hot-swap and cold-sparing.	1-7
DC and Switching Characteristics v1.4	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	2-6
	In Table 2-116 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-96
	In Table 2-117 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-97
	In the title of Table 2-74 • 1.8 V LVCMOS High Slew, VCCI had a typo. It was changed from 3.0 V to 1.7 V.	2-58
Revision 7 (Feb 2009) Product Brief v1.1	The "Advanced I/O" section was revised to add a bullet regarding wide range power supply voltage support.	I
	The table under "Features and Benefits" section, was updated to include a value for typical equivalent macrocells for A3P250.	I
	The QN48 package was added to the following tables: the table under "Features and Benefits" section, "I/Os Per Package 1" "ProASIC3 FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings". The number of singled-ended I/Os for QN68 was added to the "I/Os Per Package 1" table.	N/A
	The Wide Range I/O Support section is new.	1-7
Revision 6 (Dec 2008) Packaging v1.4	The "QN48 – Bottom View" section is new.	4-1
	The "QN68" pin table for A3P030 is new.	4-5

Revision	Changes	Page
Revision 5 (Aug 2008) DC and Switching Characteristics v1.3	TJ, Maximum Junction Temperature, was changed to 100° from 110º in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.	2-6
	Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics.	2-7
	Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new.	2-11, 2-12
	The "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	Both fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 • Input DDR Propagation Delays.	2-78
	Table 2-107 • A3P015 Global Resource is new.	2-86
	The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
Revision 4 (Jun 2008) DC and Switching Characteristics v1.2	Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed.	2-2
	The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power.	2-7
	Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X.	2-27
	Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-66
Revision 3 (Jun 2008) Packaging v1.3	Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram.	4-3
	The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
Revision 2 (Feb 2008) Product Brief v1.0	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Flash Family FPGAs" "A3P015 and A3P030" note Introduction and Overview (NA)	N/A

Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21

Revision	Changes	Page
Advance v0.3	The "PLL Macro" section was updated. EXTFB information was removed from this section.	2-15
	The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-11 • ProASIC3 CCC/PLL Specification	2-29
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Hot-Swap Support" section was updated.	2-33
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to $VCC_I B1$.	2-97
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "JTAG Pins" section was updated.	2-51
	"128-Bit AES Decryption" section was updated to include M7 device information.	2-53
	Table 3-6 was updated.	3-6
	Table 3-7 was updated.	3-6
	In Table 3-11, PAC4 was updated.	3-93-8
	Table 3-20 was updated.	3-20
	The note in Table 3-32 was updated.	3-27
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-31 to 3-73
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-85 to 3-90
	F_{TCKMAX} was updated in Table 3-110.	3-97
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-13 was updated.	2-30
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34