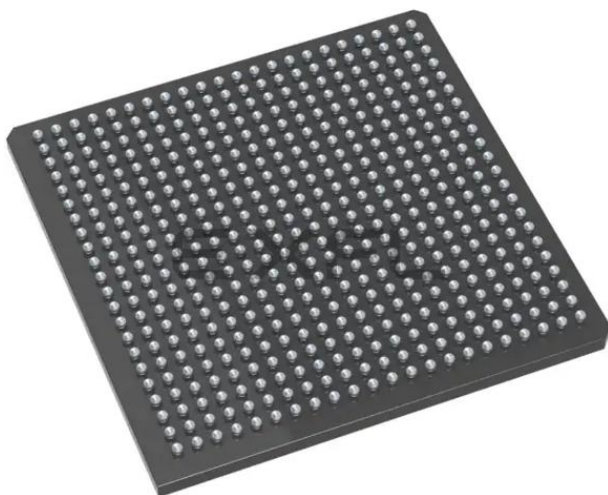




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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	235
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p600-1fg484

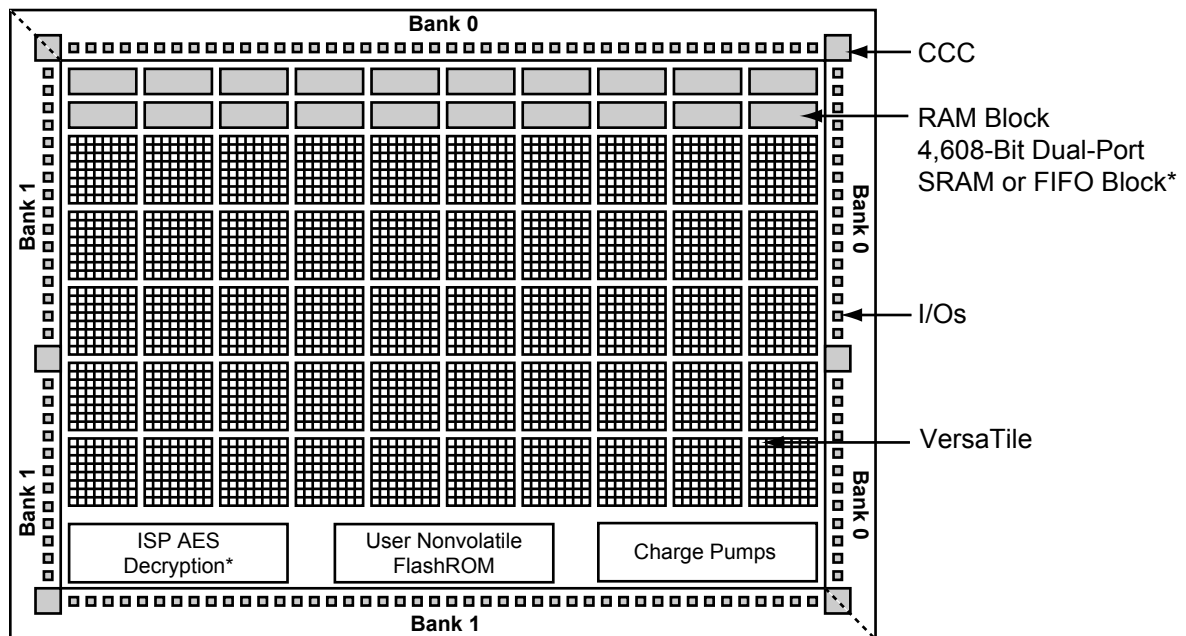
Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure



Note: *Not supported by A3P015 and A3P030 devices

Figure 1-1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)

[†] The A3P015 and A3P030 do not support PLL or SRAM.

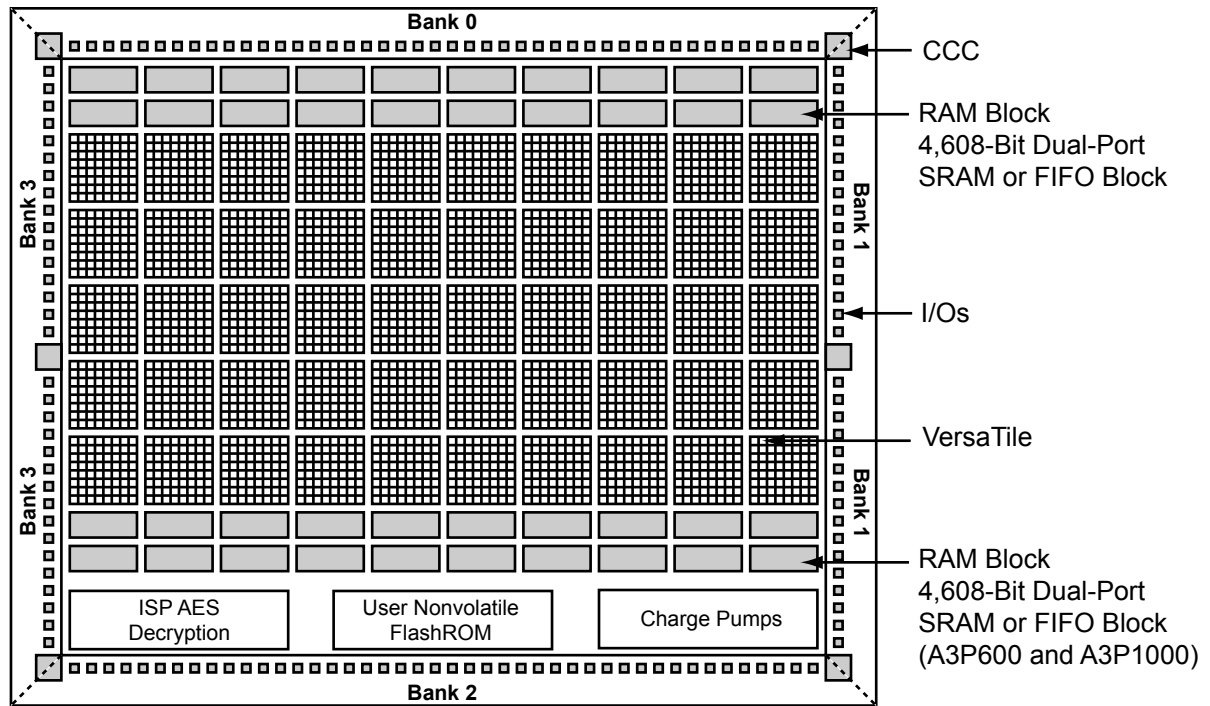


Figure 1-2 • ProASIC3 Device Architecture Overview with Four I/O Banks (A3P250, A3P600, and A3P1000)

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or as a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Microsemi ProASIC family of third-generation architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

VersaTiles

The ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.

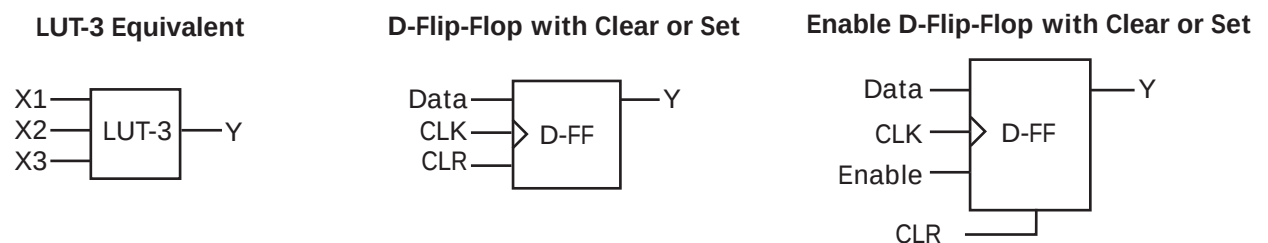


Figure 1-3 • VersaTile Configurations

Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-10 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range ³	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-33 • I/O Short Currents IOSH/IOSL
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range ²	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Notes:

1. $T_J = 100^{\circ}\text{C}$
2. Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Timing Characteristics

Table 2-60 • 2.5 V LVC MOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	–1	0.51	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	–2	0.45	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
6 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
8 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.60	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.51	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.60	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	–1	0.51	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	–2	0.45	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.60	3.09	0.04	1.31	0.43	3.15	2.44	3.44	4.00	5.38	4.68	ns
	–1	0.51	2.63	0.04	1.11	0.36	2.68	2.08	2.92	3.40	4.58	3.98	ns
	–2	0.45	2.31	0.03	0.98	0.32	2.35	1.82	2.57	2.98	4.02	3.49	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-68 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	9	11	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	17	22	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

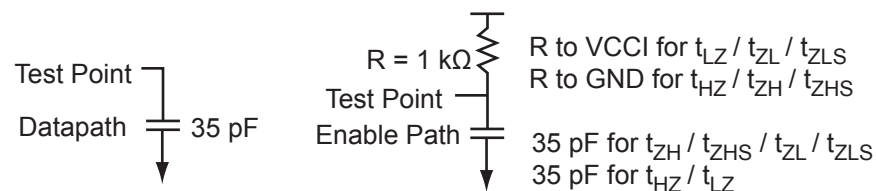


Figure 2-9 • AC Loading

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-22 for a complete table of trip points.

Table 2-93 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

Note: *Measuring point = V_{trip} . See [Table 2-22 on page 2-22](#) for a complete table of trip points.

Timing Characteristics

Table 2-95 • LVPECL

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.80	0.04	1.40	ns
–1	0.56	1.53	0.04	1.19	ns
–2	0.49	1.34	0.03	1.05	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

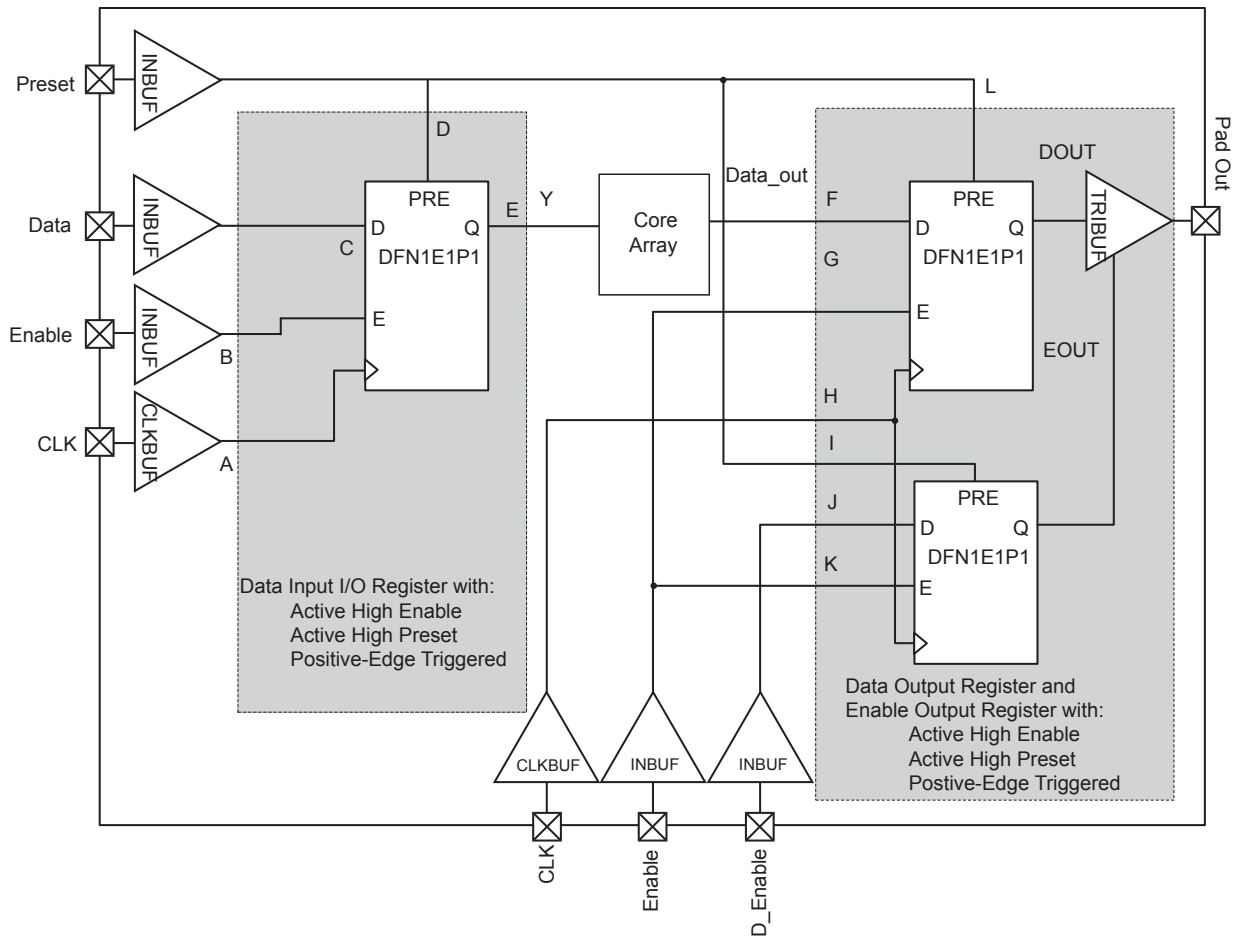


Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Output Register

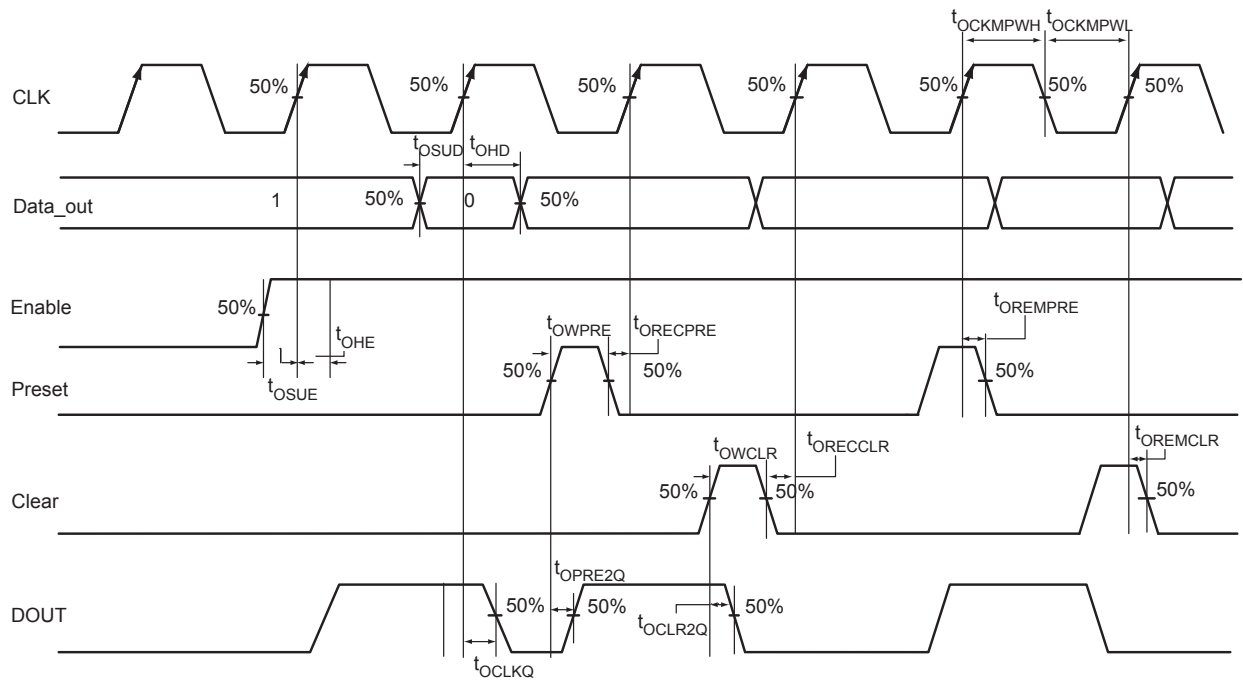


Figure 2-18 • Output Register Timing Diagram

Timing Characteristics

Table 2-99 • Output Data Register Propagation Delays

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.59	0.67	0.79	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.31	0.36	0.42	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.44	0.50	0.59	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.80	0.91	1.07	ns
t_{OEMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.22	0.25	0.30	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.25	0.30	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.41	0.48	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

Table 2-118 • FIFO (for all dies except A3P250)
Worst Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.34	1.52	1.79	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

VQ100	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

VQ100	
Pin Number	A3P125 Function
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

VQ100	
Pin Number	A3P125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

PQ208	
Pin Number	A3P250 Function
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO115UDB3
9	IO115VDB3
10	IO114UDB3
11	IO114VDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	VCC
17	GND
18	VCCIB3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	VCOMPLF
26	GFA0/IO108NPB3
27	VCCPLF
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC

PQ208	
Pin Number	A3P250 Function
37	IO104PDB3
38	IO104NDB3
39	IO103PSB3
40	VCCIB3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	VCCIB2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P250 Function
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	VCC
89	VCCIB2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

FG256	
Pin Number	A3P250 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC

FG256	
Pin Number	A3P250 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0

FG256	
Pin Number	A3P250 Function
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

FG256	
Pin Number	A3P250 Function
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

FG256	
Pin Number	A3P250 Function
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

FG256	
Pin Number	A3P250 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2

FG256	
Pin Number	A3P400 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO17RSB0
A7	IO22RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO154UDB3
B2	GAA2/IO155UDB3
B3	IO12RSB0
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO44RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO154VDB3
C2	IO155VDB3
C3	IO11RSB0
C4	IO07RSB0

FG256	
Pin Number	A3P400 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO45RSB0
C12	GBC0/IO54RSB0
C13	IO48RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO151VDB3
D2	IO151UDB3
D3	GAC2/IO153UDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO46RSB0
D12	GNDQ
D13	IO47RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO150PDB3
E2	IO08RSB0
E3	IO153VDB3
E4	IO152VDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0

FG256	
Pin Number	A3P400 Function
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO65RSB1
E15	IO52RSB0
E16	IO66PDB1
F1	IO150NDB3
F2	IO149NPB3
F3	IO09RSB0
F4	IO152UDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO49RSB0
F15	IO64PPB1
F16	IO66NDB1
G1	IO148NDB3
G2	IO148PDB3
G3	IO149PPB3
G4	GFC1/IO147PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

FG256	
Pin Number	A3P400 Function
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2

FG256	
Pin Number	A3P400 Function
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

FG256	
Pin Number	A3P600 Function
P9	IO107RSB2
P10	IO104RSB2
P11	IO97RSB2
P12	VMV1
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO88NDB1
R1	GEA1/IO144PDB3
R2	GEA0/IO144NDB3
R3	IO139RSB2
R4	GEC2/IO141RSB2
R5	IO132RSB2
R6	IO127RSB2
R7	IO121RSB2
R8	IO114RSB2
R9	IO109RSB2
R10	IO105RSB2
R11	IO98RSB2
R12	IO96RSB2
R13	GDB2/IO90RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO137RSB2
T3	GEB2/IO142RSB2
T4	IO134RSB2
T5	IO125RSB2
T6	IO123RSB2
T7	IO118RSB2
T8	IO115RSB2
T9	IO111RSB2
T10	IO106RSB2
T11	IO102RSB2
T12	GDC2/IO91RSB2

FG256	
Pin Number	A3P600 Function
T13	IO93RSB2
T14	GDA2/IO89RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P1000 Function
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND

FG484	
Pin Number	A3P1000 Function
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3

FG484	
Pin Number	A3P1000 Function
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	VCC
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1

Revision	Changes	Page								
Advance v0.6 (continued)	The "Programming" section was updated to include information concerning serialization.	2-53								
	The "JTAG 1532" section was updated to include SAMPLE/PRELOAD information.	2-54								
	"DC and Switching Characteristics" chapter was updated with new information.	3-1								
	The A3P060 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P125 "100-Pin VQFP" pin table was updated.	4-13								
	The A3P060 "144-Pin TQFP" pin table was updated.	4-16								
	The A3P125 "144-Pin TQFP" pin table was updated.	4-18								
	The A3P125 "208-Pin PQFP" pin table was updated.	4-21								
	The A3P400 "208-Pin PQFP" pin table was updated.	4-25								
	The A3P060 "144-Pin FBGA" pin table was updated.	4-32								
	The A3P125 "144-Pin FBGA" pin table is new.	4-34								
	The A3P400 "144-Pin FBGA" is new.	4-38								
	The A3P400 "256-Pin FBGA" was updated.	4-48								
	The A3P1000 "256-Pin FBGA" was updated.	4-54								
	The A3P400 "484-Pin FBGA" was updated.	4-58								
	The A3P1000 "484-Pin FBGA" was updated.	4-68								
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14								
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23								
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29								
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36								
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32								
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45								
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54								
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68								
Advance v0.5 (November 2005)	The "I/Os Per Package" table was updated for the following devices and packages: <table><tr><td>Device</td><td>Package</td></tr><tr><td>A3P250/M7ACP250</td><td>VQ100</td></tr><tr><td>A3P250/M7ACP250</td><td>FG144</td></tr><tr><td>A3P1000</td><td>FG256</td></tr></table>	Device	Package	A3P250/M7ACP250	VQ100	A3P250/M7ACP250	FG144	A3P1000	FG256	ii
Device	Package									
A3P250/M7ACP250	VQ100									
A3P250/M7ACP250	FG144									
A3P1000	FG256									
Advance v0.4	M7 device information is new.	N/A								
	The I/O counts in the "I/Os Per Package" table were updated.	ii								
Advance v0.3	The "I/Os Per Package" table was updated.	ii								
	M7 device information is new.	N/A								
	Table 2-4 • ProASIC3 Globals/Spines/Rows by Device was updated to include the number or rows in each top or bottom spine.	2-16								
	EXTFB was removed from Figure 2-24 • ProASIC3E CCC Options.	2-24								

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3 Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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