# Microchip Technology - A3P600-1PQG208 Datasheet

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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

| **Details** | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 110592 |
| Number of I/O | 154 |
| Number of Gates | 600000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 208-BFQFP |
| Supplier Device Package | 208-PQFP (28x28) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/a3p600-1pqg208 |

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong

# 1 – ProASIC3 Device Family Overview

## General Description

ProASIC3, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC$^{\text{PLUS}}$® family. Nonvolatile flash technology gives ProASIC3 devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P015 and A3P030 devices have no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

ProASIC3 devices support the ARM Cortex-M1 processor. The ARM-enabled devices have Microsemi ordering numbers that begin with M1A3P (Cortex-M1) and do not support AES decryption.

### Flash Advantages

#### *Reduced Cost of Ownership*

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3 devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

#### *Security*

The nonvolatile, flash-based ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

ARM-enabled ProASIC3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks.

$F_{CLK}$ is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$, $P_{AC2}$, $P_{AC3}$, and $P_{AC4}$ are device-dependent.

### Sequential Cells Contribution—$P_{S\text{-}CELL}$

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Combinatorial Cells Contribution—$P_{C\text{-}CELL}$

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### Routing Net Contribution—$P_{NET}$

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$ is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-16 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Input Buffer Contribution—$P_{INPUTS}$

$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$

$N_{INPUTS}$ is the number of I/O input buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

### I/O Output Buffer Contribution—$P_{OUTPUTS}$

$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

$\alpha_2$ is the I/O buffer toggle rate—guidelines are provided in Table 2-16 on page 2-14.

$\beta_1$ is the I/O buffer enable rate—guidelines are provided in Table 2-17 on page 2-14.

$F_{CLK}$ is the global clock signal frequency.

# User I/O Characteristics

## Timing Model

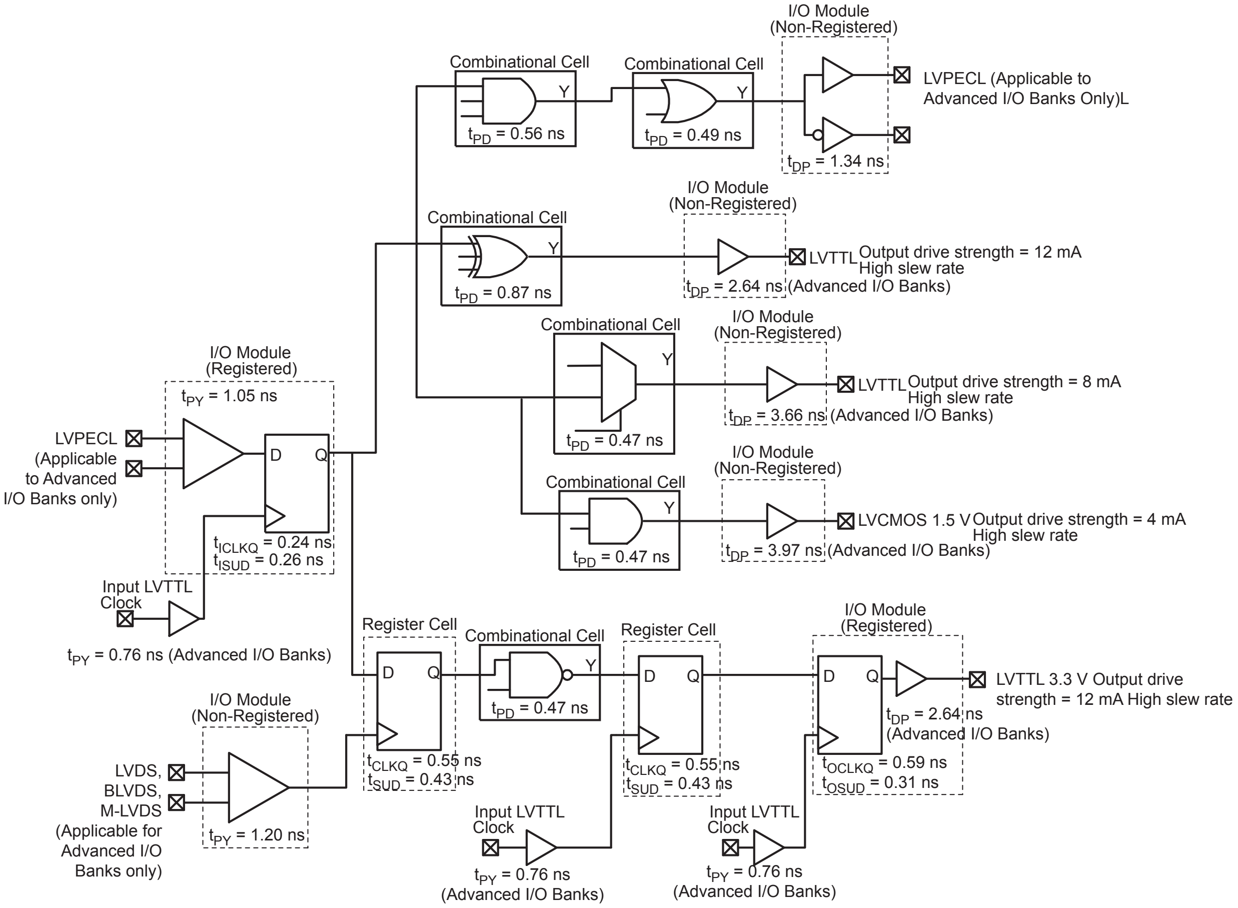

**Figure 2-3 • Timing Model**
**Operating Conditions: –2 Speed, Commercial Temperature Range ($T_J$ = 70°C), Worst Case VCC = 1.425 V**

**Table 2-32 • I/O Short Currents IOSH/IOSL Applicable to Advanced I/O Banks**

| | Drive Strength | IOSL (mA)[1] | IOSH (mA)[1] |
|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 2 mA | 27 | 25 |
| | 4 mA | 27 | 25 |
| | 6 mA | 54 | 51 |
| | 8 mA | 54 | 51 |
| | 12 mA | 109 | 103 |
| | 16 mA | 127 | 132 |
| | 24 mA | 181 | 268 |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | Same as regular 3.3 V LVCMOS | Same as regular 3.3 V LVCMOS |
| 2.5 V LVCMOS | 2 mA | 18 | 16 |
| | 4 mA | 18 | 16 |
| | 6 mA | 37 | 32 |
| | 8 mA | 37 | 32 |
| | 12 mA | 74 | 65 |
| | 16 mA | 87 | 83 |
| | 24 mA | 124 | 169 |
| 1.8 V LVCMOS | 2 mA | 11 | 9 |
| | 4 mA | 22 | 17 |
| | 6 mA | 44 | 35 |
| | 8 mA | 51 | 45 |
| | 12 mA | 74 | 91 |
| | 16 mA | 74 | 91 |
| 1.5 V LVCMOS | 2 mA | 16 | 13 |
| | 4 mA | 33 | 25 |
| | 6 mA | 39 | 32 |
| | 8 mA | 55 | 66 |
| | 12 mA | 55 | 66 |
| 3.3 V PCI/PCI-X | Per PCI/PCI-X specification | 109 | 103 |

*Notes:*

1. *$T_J$ = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. $I_{OSL}/I_{OSH}$ dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

### *3.3 V PCI, 3.3 V PCI-X*

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

***Table 2-86 •*** **Minimum and Maximum DC Input and Output Levels**

| **3.3 V PCI/PCI-X** | **VIL** | | **VIH** | | **VOL** | **VOH** | **IOL** | **IOH** | **IOSL** | **IOSH** | **IIL** | **IIH** |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| **Drive Strength** | **Min. V** | **Max. V** | **Min. V** | **Max. V** | **Max,. V** | **Min. V** | **mA** | **mA** | **Max. mA[1]** | **Max. mA[1]** | **µA[2]** | **µA[2]** |
| Per PCI specification | Per PCI curves | | | | | | | | | | 10 | 10 |

*Notes:*

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

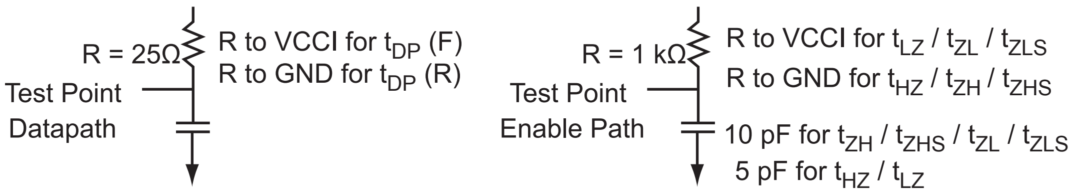

***Figure 2-11 •*** **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-87.

***Table 2-87 •*** **AC Waveforms, Measuring Points, and Capacitive Loads**

| **Input Low (V)** | **Input High (V)** | **Measuring Point* (V)** | **$C_{LOAD}$ (pF)** |
|---|---|---|---|
| 0 | 3.3 | 0.285 * VCCI for $t_{DP(R)}$<br>0.615 * VCCI for $t_{DP(F)}$ | 10 |

*Note: *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.*

### Timing Characteristics

**Table 2-88 • 3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Advanced I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.68 | 0.04 | 0.86 | 0.43 | 2.73 | 1.95 | 3.21 | 3.58 | 4.97 | 4.19 | ns |
| –1 | 0.56 | 2.28 | 0.04 | 0.73 | 0.36 | 2.32 | 1.66 | 2.73 | 3.05 | 4.22 | 3.56 | ns |
| –2 | 0.49 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

**Table 2-89 • 3.3 V PCI/PCI-X**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V**
**Applicable to Standard Plus I/O Banks**

| Speed Grade | $t_{DOUT}$ | $t_{DP}$ | $t_{DIN}$ | $t_{PY}$ | $t_{EOUT}$ | $t_{ZL}$ | $t_{ZH}$ | $t_{LZ}$ | $t_{HZ}$ | $t_{ZLS}$ | $t_{ZHS}$ | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Std. | 0.66 | 2.31 | 0.04 | 0.85 | 0.43 | 2.35 | 1.70 | 2.79 | 3.22 | 4.59 | 3.94 | ns |
| –1 | 0.56 | 1.96 | 0.04 | 0.72 | 0.36 | 2.00 | 1.45 | 2.37 | 2.74 | 3.90 | 3.35 | ns |
| –2 | 0.49 | 1.72 | 0.03 | 0.64 | 0.32 | 1.76 | 1.27 | 2.08 | 2.41 | 3.42 | 2.94 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Differential I/O Characteristics

### Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Microsemi Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

### LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

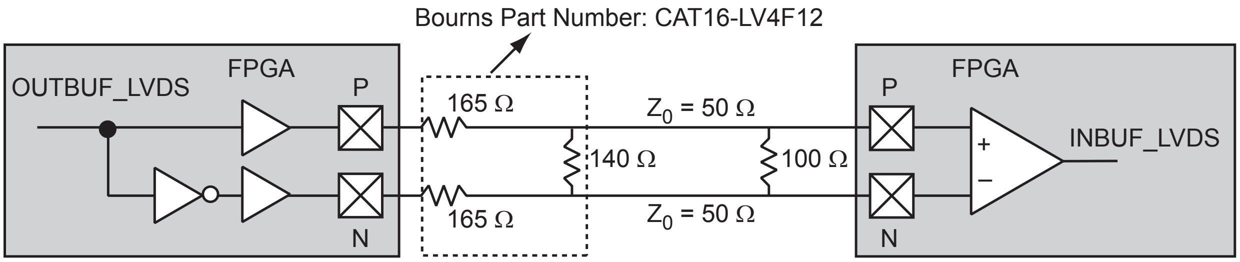

*Figure 2-12 •* **LVDS Circuit Diagram and Board-Level Implementation**

*Table 2-97 •* **Parameter Definition and Measuring Nodes**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to)* |
|---|---|---|
| $t_{OCLKQ}$ | Clock-to-Q of the Output Data Register | HH, DOUT |
| $t_{OSUD}$ | Data Setup Time for the Output Data Register | FF, HH |
| $t_{OHD}$ | Data Hold Time for the Output Data Register | FF, HH |
| $t_{OSUE}$ | Enable Setup Time for the Output Data Register | GG, HH |
| $t_{OHE}$ | Enable Hold Time for the Output Data Register | GG, HH |
| $t_{OCLR2Q}$ | Asynchronous Clear-to-Q of the Output Data Register | LL, DOUT |
| $t_{OREMCLR}$ | Asynchronous Clear Removal Time for the Output Data Register | LL, HH |
| $t_{ORECCLR}$ | Asynchronous Clear Recovery Time for the Output Data Register | LL, HH |
| $t_{OECLKQ}$ | Clock-to-Q of the Output Enable Register | HH, EOUT |
| $t_{OESUD}$ | Data Setup Time for the Output Enable Register | JJ, HH |
| $t_{OEHD}$ | Data Hold Time for the Output Enable Register | JJ, HH |
| $t_{OESUE}$ | Enable Setup Time for the Output Enable Register | KK, HH |
| $t_{OEHE}$ | Enable Hold Time for the Output Enable Register | KK, HH |
| $t_{OECLR2Q}$ | Asynchronous Clear-to-Q of the Output Enable Register | II, EOUT |
| $t_{OEREMCLR}$ | Asynchronous Clear Removal Time for the Output Enable Register | II, HH |
| $t_{OERECCLR}$ | Asynchronous Clear Recovery Time for the Output Enable Register | II, HH |
| $t_{ICLKQ}$ | Clock-to-Q of the Input Data Register | AA, EE |
| $t_{ISUD}$ | Data Setup Time for the Input Data Register | CC, AA |
| $t_{IHD}$ | Data Hold Time for the Input Data Register | CC, AA |
| $t_{ISUE}$ | Enable Setup Time for the Input Data Register | BB, AA |
| $t_{IHE}$ | Enable Hold Time for the Input Data Register | BB, AA |
| $t_{ICLR2Q}$ | Asynchronous Clear-to-Q of the Input Data Register | DD, EE |
| $t_{IREMCLR}$ | Asynchronous Clear Removal Time for the Input Data Register | DD, AA |
| $t_{IRECCLR}$ | Asynchronous Clear Recovery Time for the Input Data Register | DD, AA |

Note: *See Figure 2-16 on page 2-71 for more information.

## Output Enable Register

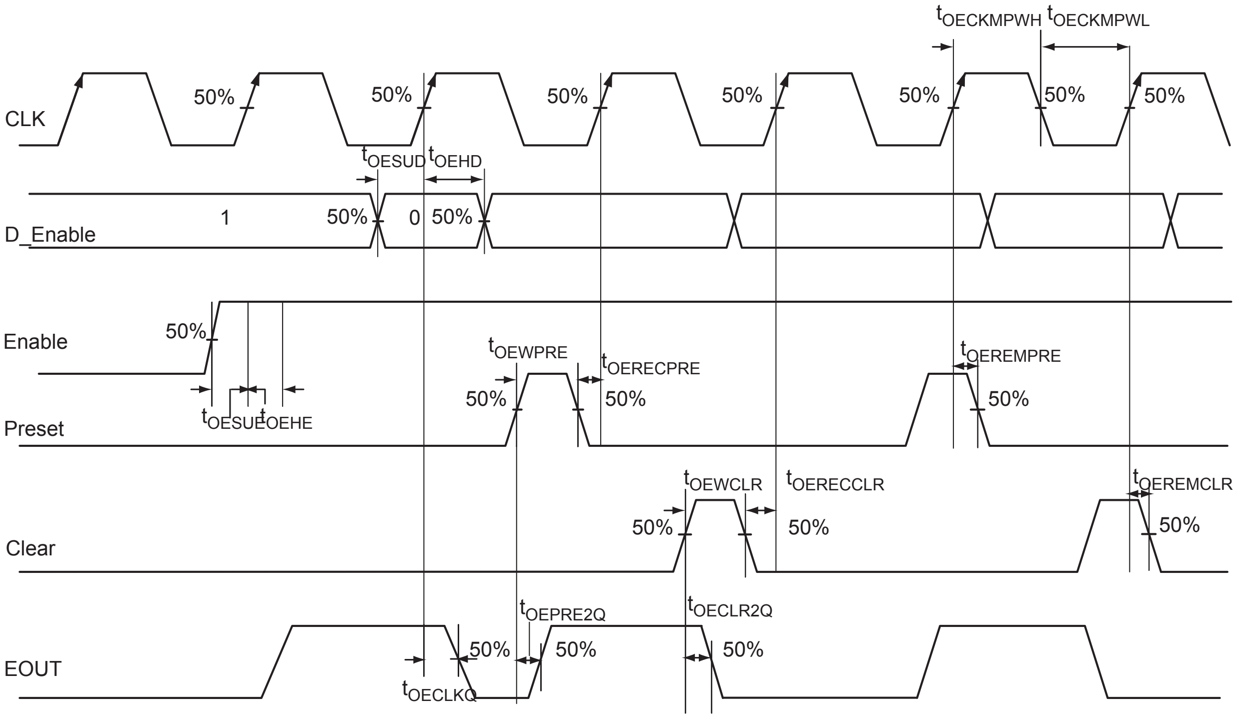

***Figure 2-19* • Output Enable Register Timing Diagram**

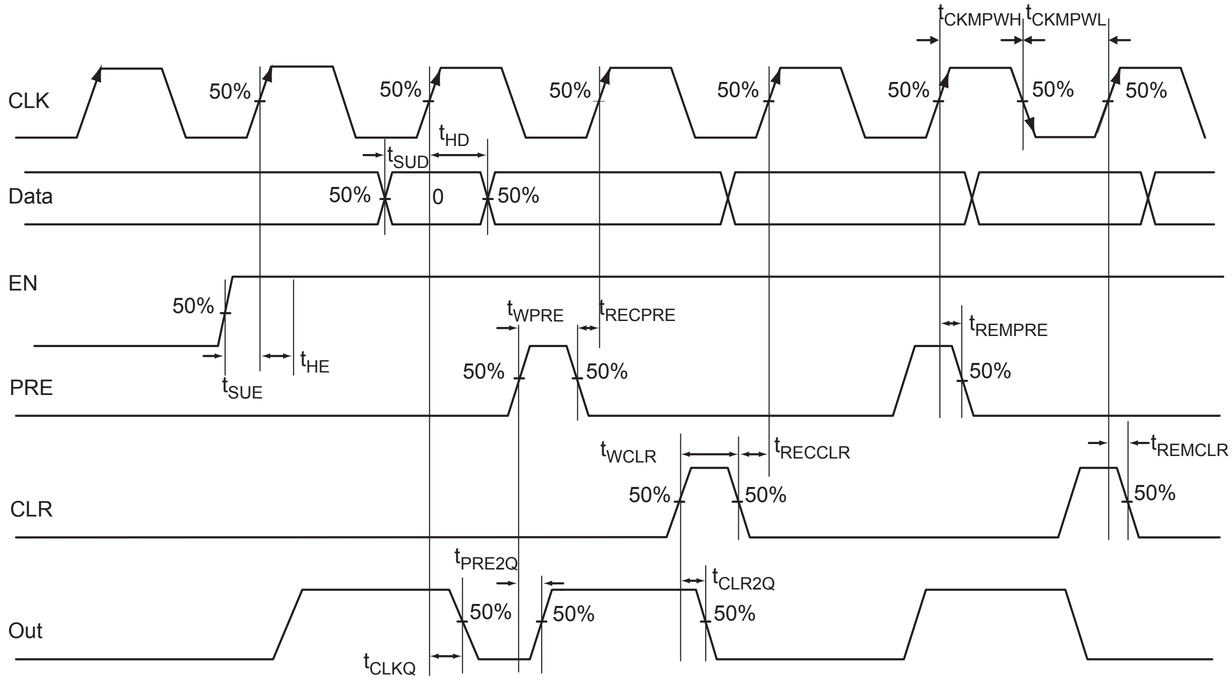

*Figure 2-27* • **Timing Model and Waveforms**

## *Timing Characteristics*

***Table 2-106* • Register Delays**
**Commercial-Case Conditions: $T_J$ = 70°C, Worst-Case VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{CLKQ}$ | Clock-to-Q of the Core Register | 0.55 | 0.63 | 0.74 | ns |
| $t_{SUD}$ | Data Setup Time for the Core Register | 0.43 | 0.49 | 0.57 | ns |
| $t_{HD}$ | Data Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{SUE}$ | Enable Setup Time for the Core Register | 0.45 | 0.52 | 0.61 | ns |
| $t_{HE}$ | Enable Hold Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{CLR2Q}$ | Asynchronous Clear-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{PRE2Q}$ | Asynchronous Preset-to-Q of the Core Register | 0.40 | 0.45 | 0.53 | ns |
| $t_{REMCLR}$ | Asynchronous Clear Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECCLR}$ | Asynchronous Clear Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{REMPRE}$ | Asynchronous Preset Removal Time for the Core Register | 0.00 | 0.00 | 0.00 | ns |
| $t_{RECPRE}$ | Asynchronous Preset Recovery Time for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WCLR}$ | Asynchronous Clear Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{WPRE}$ | Asynchronous Preset Minimum Pulse Width for the Core Register | 0.22 | 0.25 | 0.30 | ns |
| $t_{CKMPWH}$ | Clock Minimum Pulse Width High for the Core Register | 0.32 | 0.37 | 0.43 | ns |
| $t_{CKMPWL}$ | Clock Minimum Pulse Width Low for the Core Register | 0.36 | 0.41 | 0.48 | ns |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Waveforms

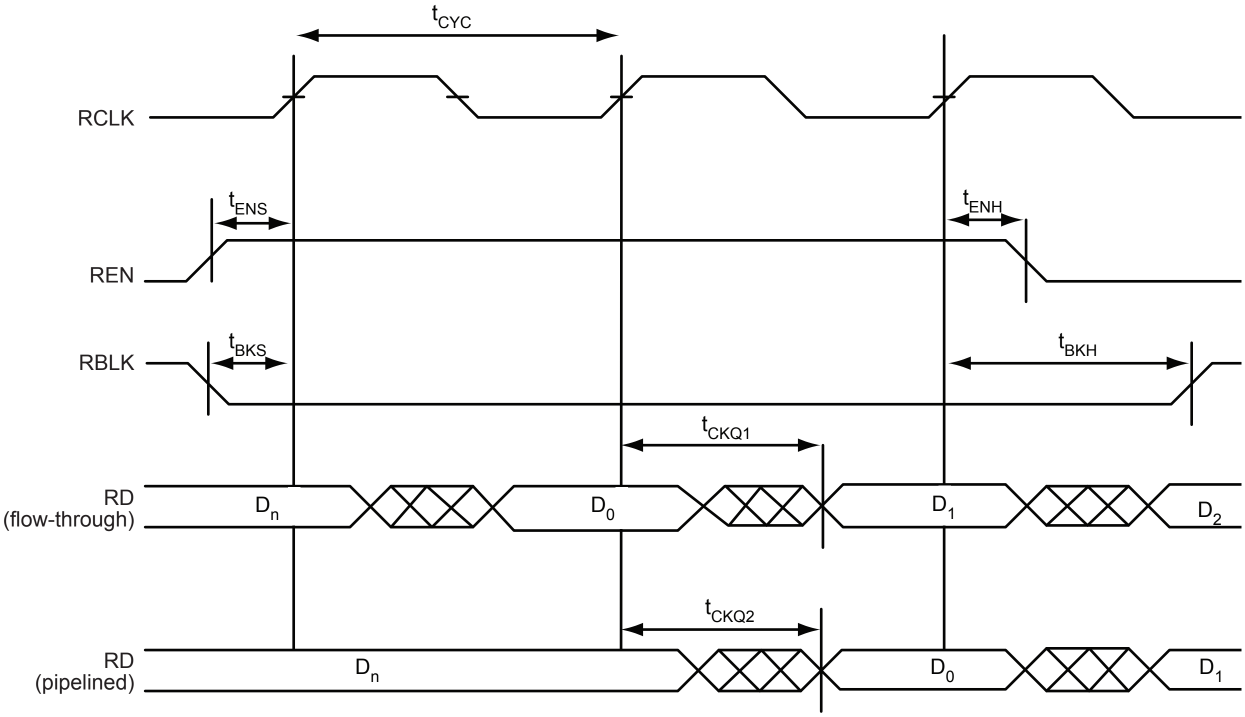

**Figure 2-37 • FIFO Read**

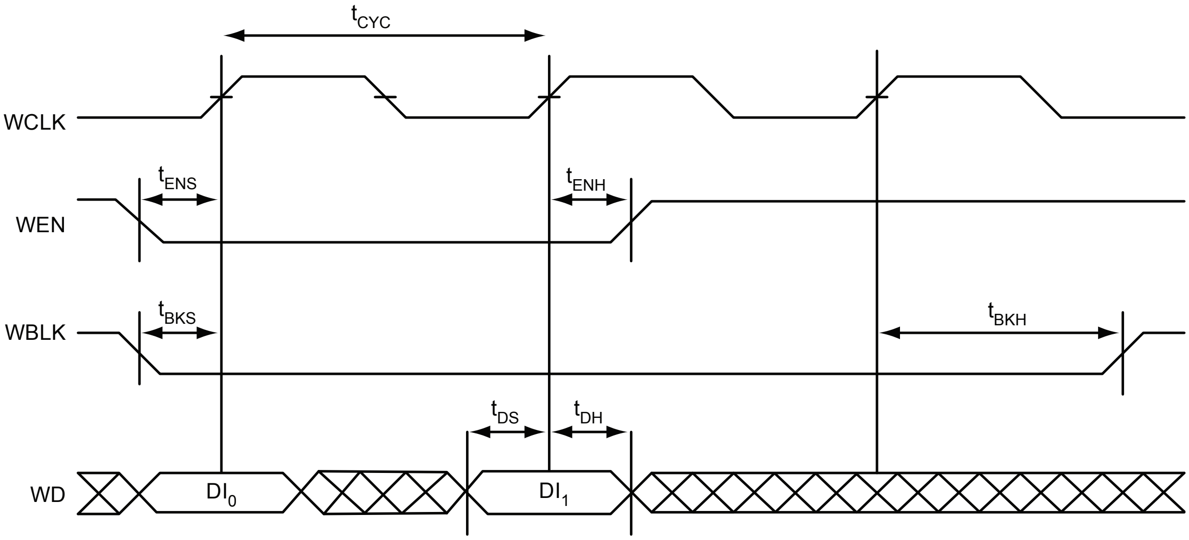

**Figure 2-38 • FIFO Write**

## Timing Characteristics

**Table 2-118 • FIFO (for all dies except A3P250)**
**Worst Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | –1 | Std. | Units |
|---|---|---|---|---|---|
| $t_{ENS}$ | REN, WEN Setup Time | 1.34 | 1.52 | 1.79 | ns |
| $t_{ENH}$ | REN, WEN Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{BKS}$ | BLK Setup Time | 0.19 | 0.22 | 0.26 | ns |
| $t_{BKH}$ | BLK Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{DS}$ | Input Data (WD) Setup Time | 0.18 | 0.21 | 0.25 | ns |
| $t_{DH}$ | Input Data (WD) Hold Time | 0.00 | 0.00 | 0.00 | ns |
| $t_{CKQ1}$ | Clock High to New Data Valid on RD (flow-through) | 2.17 | 2.47 | 2.90 | ns |
| $t_{CKQ2}$ | Clock High to New Data Valid on RD (pipelined) | 0.94 | 1.07 | 1.26 | ns |
| $t_{RCKEF}$ | RCLK High to Empty Flag Valid | 1.72 | 1.96 | 2.30 | ns |
| $t_{WCKFF}$ | WCLK High to Full Flag Valid | 1.63 | 1.86 | 2.18 | ns |
| $t_{CKAF}$ | Clock High to Almost Empty/Full Flag Valid | 6.19 | 7.05 | 8.29 | ns |
| $t_{RSTFG}$ | RESET Low to Empty/Full Flag Valid | 1.69 | 1.93 | 2.27 | ns |
| $t_{RSTAF}$ | RESET Low to Almost Empty/Full Flag Valid | 6.13 | 6.98 | 8.20 | ns |
| $t_{RSTBQ}$ | RESET Low to Data Out Low on RD (flow-through) | 0.92 | 1.05 | 1.23 | ns |
| | RESET Low to Data Out Low on RD (pipelined) | 0.92 | 1.05 | 1.23 | ns |
| $t_{REMRSTB}$ | RESET Removal | 0.29 | 0.33 | 0.38 | ns |
| $t_{RECRSTB}$ | RESET Recovery | 1.50 | 1.71 | 2.01 | ns |
| $t_{MPWRSTB}$ | RESET Minimum Pulse Width | 0.21 | 0.24 | 0.29 | ns |
| $t_{CYC}$ | Clock Cycle Time | 3.23 | 3.68 | 4.32 | ns |
| $F_{MAX}$ | Maximum Frequency for FIFO | 310 | 272 | 231 | MHz |

*Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

| QN68 | |
|---|---|
| **Pin Number** | **A3P015 Function** |
| 1 | IO82RSB1 |
| 2 | IO80RSB1 |
| 3 | IO78RSB1 |
| 4 | IO76RSB1 |
| 5 | GEC0/IO73RSB1 |
| 6 | GEA0/IO72RSB1 |
| 7 | GEB0/IO71RSB1 |
| 8 | VCC |
| 9 | GND |
| 10 | VCCIB1 |
| 11 | IO68RSB1 |
| 12 | IO67RSB1 |
| 13 | IO66RSB1 |
| 14 | IO65RSB1 |
| 15 | IO64RSB1 |
| 16 | IO63RSB1 |
| 17 | IO62RSB1 |
| 18 | IO60RSB1 |
| 19 | IO58RSB1 |
| 20 | IO56RSB1 |
| 21 | IO54RSB1 |
| 22 | IO52RSB1 |
| 23 | IO51RSB1 |
| 24 | VCC |
| 25 | GND |
| 26 | VCCIB1 |
| 27 | IO50RSB1 |
| 28 | IO48RSB1 |
| 29 | IO46RSB1 |
| 30 | IO44RSB1 |
| 31 | IO42RSB1 |
| 32 | TCK |
| 33 | TDI |
| 34 | TMS |
| 35 | VPUMP |
| 36 | TDO |
| 37 | TRST |
| 38 | VJTAG |
| 39 | IO40RSB0 |
| 40 | IO37RSB0 |
| 41 | GDB0/IO34RSB0 |
| 42 | GDA0/IO33RSB0 |
| 43 | GDC0/IO32RSB0 |
| 44 | VCCIB0 |
| 45 | GND |
| 46 | VCC |
| 47 | IO31RSB0 |
| 48 | IO29RSB0 |
| 49 | IO28RSB0 |
| 50 | IO27RSB0 |
| 51 | IO25RSB0 |
| 52 | IO24RSB0 |
| 53 | IO22RSB0 |
| 54 | IO21RSB0 |
| 55 | IO19RSB0 |
| 56 | IO17RSB0 |
| 57 | IO15RSB0 |
| 58 | IO14RSB0 |
| 59 | VCCIB0 |
| 60 | GND |
| 61 | VCC |
| 62 | IO12RSB0 |
| 63 | IO10RSB0 |
| 64 | IO08RSB0 |
| 65 | IO06RSB0 |
| 66 | IO04RSB0 |
| 67 | IO02RSB0 |
| 68 | IO00RSB0 |

| TQ144 | |
|---|---|
| **Pin Number** | **A3P125 Function** |
| 109 | GBA1/IO40RSB0 |
| 110 | GBA0/IO39RSB0 |
| 111 | GBB1/IO38RSB0 |
| 112 | GBB0/IO37RSB0 |
| 113 | GBC1/IO36RSB0 |
| 114 | GBC0/IO35RSB0 |
| 115 | IO34RSB0 |
| 116 | IO33RSB0 |
| 117 | VCCIB0 |
| 118 | GND |
| 119 | VCC |
| 120 | IO29RSB0 |
| 121 | IO28RSB0 |
| 122 | IO27RSB0 |
| 123 | IO25RSB0 |
| 124 | IO23RSB0 |
| 125 | IO21RSB0 |
| 126 | IO19RSB0 |
| 127 | IO17RSB0 |
| 128 | IO16RSB0 |
| 129 | IO14RSB0 |
| 130 | IO12RSB0 |
| 131 | IO10RSB0 |
| 132 | IO08RSB0 |
| 133 | IO06RSB0 |
| 134 | VCCIB0 |
| 135 | GND |
| 136 | VCC |
| 137 | GAC1/IO05RSB0 |
| 138 | GAC0/IO04RSB0 |
| 139 | GAB1/IO03RSB0 |
| 140 | GAB0/IO02RSB0 |
| 141 | GAA1/IO01RSB0 |
| 142 | GAA0/IO00RSB0 |
| 143 | GNDQ |
| 144 | VMV0 |

| FG256 | |
|---|---|
| Pin Number | A3P250 Function |
| G13 | GCC1/IO48PPB1 |
| G14 | IO47NPB1 |
| G15 | IO54PDB1 |
| G16 | IO54NDB1 |
| H1 | GFB0/IO109NPB3 |
| H2 | GFA0/IO108NDB3 |
| H3 | GFB1/IO109PPB3 |
| H4 | VCOMPLF |
| H5 | GFC0/IO110NPB3 |
| H6 | VCC |
| H7 | GND |
| H8 | GND |
| H9 | GND |
| H10 | GND |
| H11 | VCC |
| H12 | GCC0/IO48NPB1 |
| H13 | GCB1/IO49PPB1 |
| H14 | GCA0/IO50NPB1 |
| H15 | NC |
| H16 | GCB0/IO49NPB1 |
| J1 | GFA2/IO107PPB3 |
| J2 | GFA1/IO108PDB3 |
| J3 | VCCPLF |
| J4 | IO106NDB3 |
| J5 | GFB2/IO106PDB3 |
| J6 | VCC |
| J7 | GND |
| J8 | GND |
| J9 | GND |
| J10 | GND |
| J11 | VCC |
| J12 | GCB2/IO52PPB1 |
| J13 | GCA1/IO50PPB1 |
| J14 | GCC2/IO53PPB1 |
| J15 | NC |
| J16 | GCA2/IO51PDB1 |

| FG256 | |
|---|---|
| Pin Number | A3P250 Function |
| K1 | GFC2/IO105PDB3 |
| K2 | IO107NPB3 |
| K3 | IO104PPB3 |
| K4 | NC |
| K5 | VCCIB3 |
| K6 | VCC |
| K7 | GND |
| K8 | GND |
| K9 | GND |
| K10 | GND |
| K11 | VCC |
| K12 | VCCIB1 |
| K13 | IO52NPB1 |
| K14 | IO55RSB1 |
| K15 | IO53NPB1 |
| K16 | IO51NDB1 |
| L1 | IO105NDB3 |
| L2 | IO104NPB3 |
| L3 | NC |
| L4 | IO102RSB3 |
| L5 | VCCIB3 |
| L6 | GND |
| L7 | VCC |
| L8 | VCC |
| L9 | VCC |
| L10 | VCC |
| L11 | GND |
| L12 | VCCIB1 |
| L13 | GDB0/IO59VPB1 |
| L14 | IO57VDB1 |
| L15 | IO57UDB1 |
| L16 | IO56PDB1 |
| M1 | IO103PDB3 |
| M2 | NC |
| M3 | IO101NPB3 |
| M4 | GEC0/IO100NPB3 |

| FG256 | |
|---|---|
| Pin Number | A3P250 Function |
| M5 | VMV3 |
| M6 | VCCIB2 |
| M7 | VCCIB2 |
| M8 | NC |
| M9 | IO74RSB2 |
| M10 | VCCIB2 |
| M11 | VCCIB2 |
| M12 | VMV2 |
| M13 | NC |
| M14 | GDB1/IO59UPB1 |
| M15 | GDC1/IO58UDB1 |
| M16 | IO56NDB1 |
| N1 | IO103NDB3 |
| N2 | IO101PPB3 |
| N3 | GEC1/IO100PPB3 |
| N4 | NC |
| N5 | GNDQ |
| N6 | GEA2/IO97RSB2 |
| N7 | IO86RSB2 |
| N8 | IO82RSB2 |
| N9 | IO75RSB2 |
| N10 | IO69RSB2 |
| N11 | IO64RSB2 |
| N12 | GNDQ |
| N13 | NC |
| N14 | VJTAG |
| N15 | GDC0/IO58VDB1 |
| N16 | GDA1/IO60UDB1 |
| P1 | GEB1/IO99PDB3 |
| P2 | GEB0/IO99NDB3 |
| P3 | NC |
| P4 | NC |
| P5 | IO92RSB2 |
| P6 | IO89RSB2 |
| P7 | IO85RSB2 |
| P8 | IO81RSB2 |

| FG256 | |
|---|---|
| **Pin Number** | **A3P600 Function** |
| A1 | GND |
| A2 | GAA0/IO00RSB0 |
| A3 | GAA1/IO01RSB0 |
| A4 | GAB0/IO02RSB0 |
| A5 | IO11RSB0 |
| A6 | IO16RSB0 |
| A7 | IO18RSB0 |
| A8 | IO28RSB0 |
| A9 | IO34RSB0 |
| A10 | IO37RSB0 |
| A11 | IO41RSB0 |
| A12 | IO43RSB0 |
| A13 | GBB1/IO57RSB0 |
| A14 | GBA0/IO58RSB0 |
| A15 | GBA1/IO59RSB0 |
| A16 | GND |
| B1 | GAB2/IO173PDB3 |
| B2 | GAA2/IO174PDB3 |
| B3 | GNDQ |
| B4 | GAB1/IO03RSB0 |
| B5 | IO13RSB0 |
| B6 | IO14RSB0 |
| B7 | IO21RSB0 |
| B8 | IO27RSB0 |
| B9 | IO32RSB0 |
| B10 | IO38RSB0 |
| B11 | IO42RSB0 |
| B12 | GBC1/IO55RSB0 |
| B13 | GBB0/IO56RSB0 |
| B14 | IO52RSB0 |
| B15 | GBA2/IO60PDB1 |
| B16 | IO60NDB1 |
| C1 | IO173NDB3 |
| C2 | IO174NDB3 |
| C3 | VMV3 |
| C4 | IO07RSB0 |
| C5 | GAC0/IO04RSB0 |
| C6 | GAC1/IO05RSB0 |
| C7 | IO20RSB0 |
| C8 | IO24RSB0 |
| C9 | IO33RSB0 |
| C10 | IO39RSB0 |
| C11 | IO44RSB0 |
| C12 | GBC0/IO54RSB0 |
| C13 | IO51RSB0 |
| C14 | VMV0 |
| C15 | IO61NPB1 |
| C16 | IO63PDB1 |
| D1 | IO171NDB3 |
| D2 | IO171PDB3 |
| D3 | GAC2/IO172PDB3 |
| D4 | IO06RSB0 |
| D5 | GNDQ |
| D6 | IO10RSB0 |
| D7 | IO19RSB0 |
| D8 | IO26RSB0 |
| D9 | IO30RSB0 |
| D10 | IO40RSB0 |
| D11 | IO45RSB0 |
| D12 | GNDQ |
| D13 | IO50RSB0 |
| D14 | GBB2/IO61PPB1 |
| D15 | IO53RSB0 |
| D16 | IO63NDB1 |
| E1 | IO166PDB3 |
| E2 | IO167NPB3 |
| E3 | IO172NDB3 |
| E4 | IO169NDB3 |
| E5 | VMV0 |
| E6 | VCCIB0 |
| E7 | VCCIB0 |
| E8 | IO25RSB0 |
| E9 | IO31RSB0 |
| E10 | VCCIB0 |
| E11 | VCCIB0 |
| E12 | VMV1 |
| E13 | GBC2/IO62PDB1 |
| E14 | IO67PPB1 |
| E15 | IO64PPB1 |
| E16 | IO66PDB1 |
| F1 | IO166NDB3 |
| F2 | IO168NPB3 |
| F3 | IO167PPB3 |
| F4 | IO169PDB3 |
| F5 | VCCIB3 |
| F6 | GND |
| F7 | VCC |
| F8 | VCC |
| F9 | VCC |
| F10 | VCC |
| F11 | GND |
| F12 | VCCIB1 |
| F13 | IO62NDB1 |
| F14 | IO64NPB1 |
| F15 | IO65PPB1 |
| F16 | IO66NDB1 |
| G1 | IO165NDB3 |
| G2 | IO165PDB3 |
| G3 | IO168PPB3 |
| G4 | GFC1/IO164PPB3 |
| G5 | VCCIB3 |
| G6 | VCC |
| G7 | GND |
| G8 | GND |
| G9 | GND |
| G10 | GND |
| G11 | VCC |
| G12 | VCCIB1 |

| FG484 | |
|---|---|
| **Pin Number** | **A3P400 Function** |
| Y15 | VCC |
| Y16 | NC |
| Y17 | NC |
| Y18 | GND |
| Y19 | NC |
| Y20 | NC |
| Y21 | NC |
| Y22 | VCCIB1 |
| AA1 | GND |
| AA2 | VCCIB3 |
| AA3 | NC |
| AA4 | NC |
| AA5 | NC |
| AA6 | NC |
| AA7 | NC |
| AA8 | NC |
| AA9 | NC |
| AA10 | NC |
| AA11 | NC |
| AA12 | NC |
| AA13 | NC |
| AA14 | NC |
| AA15 | NC |
| AA16 | NC |
| AA17 | NC |
| AA18 | NC |
| AA19 | NC |
| AA20 | NC |
| AA21 | VCCIB1 |
| AA22 | GND |
| AB1 | GND |
| AB2 | GND |
| AB3 | VCCIB2 |
| AB4 | NC |
| AB5 | NC |
| AB6 | IO121RSB2 |
| AB7 | IO119RSB2 |
| AB8 | IO114RSB2 |
| AB9 | IO109RSB2 |
| AB10 | NC |
| AB11 | NC |
| AB12 | IO104RSB2 |
| AB13 | IO103RSB2 |
| AB14 | NC |
| AB15 | NC |
| AB16 | IO91RSB2 |
| AB17 | IO90RSB2 |
| AB18 | NC |
| AB19 | NC |
| AB20 | VCCIB2 |
| AB21 | GND |
| AB22 | GND |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| A1 | GND |
| A2 | GND |
| A3 | VCCIB0 |
| A4 | IO07RSB0 |
| A5 | IO09RSB0 |
| A6 | IO13RSB0 |
| A7 | IO18RSB0 |
| A8 | IO20RSB0 |
| A9 | IO26RSB0 |
| A10 | IO32RSB0 |
| A11 | IO40RSB0 |
| A12 | IO41RSB0 |
| A13 | IO53RSB0 |
| A14 | IO59RSB0 |
| A15 | IO64RSB0 |
| A16 | IO65RSB0 |
| A17 | IO67RSB0 |
| A18 | IO69RSB0 |
| A19 | NC |
| A20 | VCCIB0 |
| A21 | GND |
| A22 | GND |
| B1 | GND |
| B2 | VCCIB3 |
| B3 | NC |
| B4 | IO06RSB0 |
| B5 | IO08RSB0 |
| B6 | IO12RSB0 |
| B7 | IO15RSB0 |
| B8 | IO19RSB0 |
| B9 | IO24RSB0 |
| B10 | IO31RSB0 |
| B11 | IO39RSB0 |
| B12 | IO48RSB0 |
| B13 | IO54RSB0 |
| B14 | IO58RSB0 |
| B15 | IO63RSB0 |
| B16 | IO66RSB0 |
| B17 | IO68RSB0 |
| B18 | IO70RSB0 |
| B19 | NC |
| B20 | NC |
| B21 | VCCIB1 |
| B22 | GND |
| C1 | VCCIB3 |
| C2 | IO220PDB3 |
| C3 | NC |
| C4 | NC |
| C5 | GND |
| C6 | IO10RSB0 |
| C7 | IO14RSB0 |
| C8 | VCC |
| C9 | VCC |
| C10 | IO30RSB0 |
| C11 | IO37RSB0 |
| C12 | IO43RSB0 |
| C13 | NC |
| C14 | VCC |
| C15 | VCC |
| C16 | NC |
| C17 | NC |
| C18 | GND |
| C19 | NC |
| C20 | NC |
| C21 | NC |
| C22 | VCCIB1 |
| D1 | IO219PDB3 |
| D2 | IO220NDB3 |
| D3 | NC |
| D4 | GND |
| D5 | GAA0/IO00RSB0 |
| D6 | GAA1/IO01RSB0 |
| D7 | GAB0/IO02RSB0 |
| D8 | IO16RSB0 |
| D9 | IO22RSB0 |
| D10 | IO28RSB0 |
| D11 | IO35RSB0 |
| D12 | IO45RSB0 |
| D13 | IO50RSB0 |
| D14 | IO55RSB0 |
| D15 | IO61RSB0 |
| D16 | GBB1/IO75RSB0 |
| D17 | GBA0/IO76RSB0 |
| D18 | GBA1/IO77RSB0 |
| D19 | GND |
| D20 | NC |
| D21 | NC |
| D22 | NC |
| E1 | IO219NDB3 |
| E2 | NC |
| E3 | GND |
| E4 | GAB2/IO224PDB3 |
| E5 | GAA2/IO225PDB3 |
| E6 | GNDQ |
| E7 | GAB1/IO03RSB0 |
| E8 | IO17RSB0 |
| E9 | IO21RSB0 |
| E10 | IO27RSB0 |
| E11 | IO34RSB0 |
| E12 | IO44RSB0 |
| E13 | IO51RSB0 |
| E14 | IO57RSB0 |
| E15 | GBC1/IO73RSB0 |
| E16 | GBB0/IO74RSB0 |
| E17 | IO71RSB0 |
| E18 | GBA2/IO78PDB1 |
| E19 | IO81PDB1 |
| E20 | GND |

| Revision | Changes | Page |
|---|---|---|
| Revision 11 (March 2012) | Note indicating that A3P015 is not recommended for new designs has been added. The "Devices Not Recommended For New Designs" section is new (SAR 36760). | I to IV |
| | The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687). | NA |
| | The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide* (SAR 34734). | 2-12 |
| | Figure 2-4 • Input Buffer Timing Model and Delays (Example) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430). | 2-16 |
| | The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34883). | 2-32 |
| | Added values for minimum pulse width and removed the FRMAX row from Table 2-107 through Table 2-114 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269). | 2-85 |

| **Revision** | **Changes** | **Page** |
|---|---|---|
| **Revision 2 (cont'd)** | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | III |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | IV |
| | In the General Description section the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68 – Bottom View" section is new. | 4-3 |
| **Revision 1 (Feb 2008)**<br>DC and Switching Characteristics v1.1 | In Table 2-2 • Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$. | 2-2 |
| | In Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | In the "PLL Contribution—PPLL" section, the following was deleted:<br>FCLKIN is the input clock frequency. | 2-14 |
| | In Table 2-21 • Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$. | 2-21 |
| | In Table 2-115 • ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new. | 2-90 |
| | Table 2-125 • JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-108 |
| Packaging v1.1 | In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 4-19 |
| **Revision 0 (Jan 2008)** | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. | N/A |
| v2.2<br>(July 2007) | The M7 and M1 device part numbers have been updated in Table 1 • ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 • Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4–6 were added. | 3-2 |
| v2.1<br>(May 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii |
| | Table 3-5 • Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |

| Revision | Changes | Page |
|---|---|---|
| v2.0<br>(April 2007) | In the "Packaging Tables", Ambient was deleted. | ii |
| | The timing characteristics tables were updated. | N/A |
| | The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up. | 2-15 |
| | The "PLL Macro" section was updated to include power-up information. | 2-15 |
| | Table 2-11 • ProASIC3 CCC/PLL Specification was updated. | 2-29 |
| | Figure 2-19 • Peak-to-Peak Jitter Definition is new. | 2-18 |
| | The "SRAM and FIFO" section was updated with operation and timing requirement information. | 2-21 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "RESET" section was updated with read and write information. | 2-25 |
| | The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled. | 2-28 |
| | PCI-X 3.3 V was added to Table 2-11 • VCCI Voltages and Compatible Standards. | 2-29 |
| | In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4. | 2-34 |
| | Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated. | 2-64 |
| | Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7. | 2-40 |
| | The "VCCPLF PLL Supply Voltage" section was updated. | 2-50 |
| | The "VPUMP Programming Supply Voltage" section was updated. | 2-50 |
| | The "GL Globals" section was updated to include information about direct input into quadrant clocks. | 2-51 |
| | $V_{JTAG}$ was deleted from the "TCK Test Clock" section. | 2-51 |
| | In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated. | 2-51 |
| | Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45". | 3-2 |
| | Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1. | 3-2 |
| | In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951. | 3-5 |
| | Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated. | 3-6 |
| | Table 3-5 • Package Thermal Resistivities was updated. | 3-5 |
| | Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated. | 3-17 to 3-17 |