Welcome to E-XFL.COM

Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.
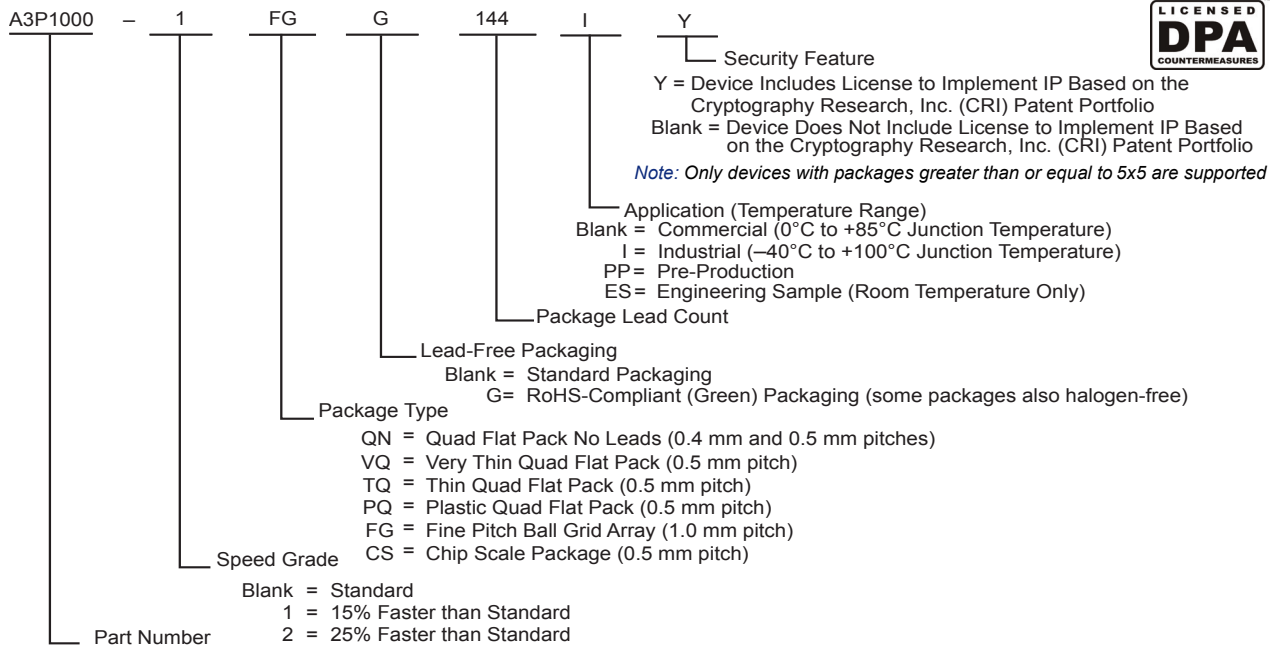
Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	177
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p600-2fg256i

ProASIC3 Ordering Information

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A3P1000    –    1    FG    G    144    I    Y
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Security Feature
Y = Device Includes License to Implement IP Based on the
    Cryptography Research, Inc. (CRI) Patent Portfolio
Blank = Device Does Not Include License to Implement IP Based
    on the Cryptography Research, Inc. (CRI) Patent Portfolio
Note: Only devices with packages greater than or equal to 5x5 are supported

Application (Temperature Range)
Blank = Commercial (0°C to +85°C Junction Temperature)
I = Industrial (−40°C to +100°C Junction Temperature)
PP = Pre-Production
ES = Engineering Sample (Room Temperature Only)

Package Lead Count

Lead-Free Packaging
Blank = Standard Packaging
G = RoHS-Compliant (Green) Packaging (some packages also halogen-free)

Package Type
QN = Quad Flat Pack No Leads (0.4 mm and 0.5 mm pitches)
VQ = Very Thin Quad Flat Pack (0.5 mm pitch)
TQ = Thin Quad Flat Pack (0.5 mm pitch)
PQ = Plastic Quad Flat Pack (0.5 mm pitch)
FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
CS = Chip Scale Package (0.5 mm pitch)

Speed Grade
Blank = Standard
1 = 15% Faster than Standard
2 = 25% Faster than Standard

Part Number

ProASIC3 Devices
A3P015 = 15,000 System Gates (A3P015 is not recommended for new designs.)
A3P030 = 30,000 System Gates
A3P060 = 60,000 System Gates
A3P125 = 125,000 System Gates
A3P250 = 250,000 System Gates
A3P400 = 400,000 System Gates
A3P600 = 600,000 System Gates
A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1
M1A3P250 = 250,000 System Gates
M1A3P400 = 400,000 System Gates
M1A3P600 = 600,000 System Gates
M1A3P1000 = 1,000,000 System Gates

ProASIC3 Device Status

ProASIC3 Devices	Status	Cortex-M1 Devices	Status
A3P015	Not recommended for new designs.		
A3P030	Production		
A3P060	Production		
A3P125	Production		
A3P250	Production	M1A3P250	Production
A3P400	Production	M1A3P400	Production
A3P600	Production	M1A3P600	Production
A3P1000	Production	M1A3P1000	Production

User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • I/O Standards Supported

		I/O Standards Supported		
I/O Bank Type	**Device and Bank Location**	**LVTTL/ LVCMOS**	**PCI/PCI-X**	**LVPECL, LVDS, B-LVDS, M-LVDS**
Advanced	East and west Banks of A3P250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	✓	✓	Not supported
Standard	All banks of A3P015 and A3P030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2
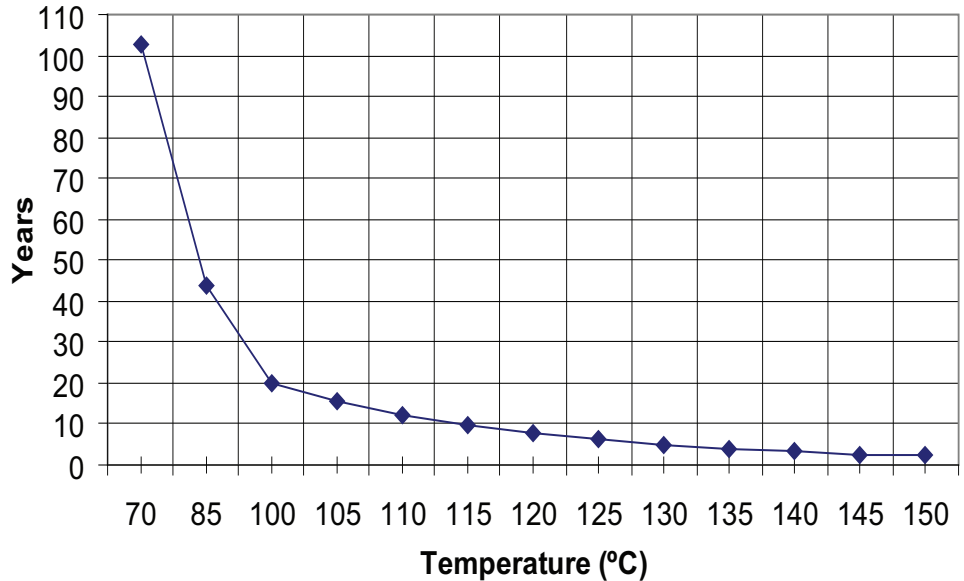
Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

Figure 2-1 • **High-Temperature Data Retention (HTR)**

Table 2-3 • **Flash Programming Limits – Retention, Storage and Operating Temperature[1]**

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T_{STG} (°C)	Maximum Operating Junction Temperature T_J (°C)[2]
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.
2. These limits apply for program/data retention only. Refer to Table 2-1 on page 2-1 and Table 2-2 for device operating conditions and absolute limits.

Table 2-4 • **Overshoot and Undershoot Limits [1]**

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[2]	Maximum Overshoot/ Undershoot[2]
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.

2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

3. This table does not provide PCI overshoot/undershoot limits.

Table 2-30 • **I/O Output Buffer Maximum Resistances[1]**
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range[4]	100 μA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL-DOWN-MAX)} = (VOLspec) / IOLspec$
3. $R_{(PULL-UP-MAX)} = (VCCImax – VOHspec) / IOHspec$
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-31 • **I/O Weak Pull-Up/Pull-Down Resistances**
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCI	$R_{(WEAK\ PULL-UP)}$[1] (Ω) Min	Max	$R_{(WEAK\ PULL-DOWN)}$[2] (Ω) Min	Max
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL-UP-MAX)} = (VCCI_{MAX} – VOH_{spec}) / I_{(WEAK\ PULL-UP-MIN)}$
2. $R_{(WEAK\ PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK\ PULL-DOWN-MIN)}$

Table 2-52 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	t$_{ZLS}$	t$_{ZHS}$	Units
100 µA	2 mA	Std.	0.60	11.14	0.04	1.52	0.43	11.14	9.54	3.51	3.61	14.53	12.94	ns
		−1	0.51	9.48	0.04	1.29	0.36	9.48	8.12	2.99	3.07	12.36	11.00	ns
		−2	0.45	8.32	0.03	1.14	0.32	8.32	7.13	2.62	2.70	10.85	9.66	ns
100 µA	4 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		−1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		−2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 µA	6 mA	Std.	0.60	6.96	0.04	1.52	0.43	6.96	5.79	3.99	4.45	10.35	9.19	ns
		−1	0.51	5.92	0.04	1.29	0.36	5.92	4.93	3.39	3.78	8.81	7.82	ns
		−2	0.45	5.20	0.03	1.14	0.32	5.20	4.33	2.98	3.32	7.73	6.86	ns
100 µA	8 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		−1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		−2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns
100 µA	16 mA	Std.	0.60	4.89	0.04	1.52	0.43	4.89	3.92	4.31	4.98	8.28	7.32	ns
		−1	0.51	4.16	0.04	1.29	0.36	4.16	3.34	3.67	4.24	7.04	6.22	ns
		−2	0.45	3.65	0.03	1.14	0.32	3.65	2.93	3.22	3.72	6.18	5.46	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *Software default selection highlighted in gray.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-64 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
2 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	−1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	−2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
4 mA	Std.	0.66	8.20	0.04	1.29	0.43	7.24	8.20	2.03	1.91	ns
	−1	0.56	6.98	0.04	1.10	0.36	6.16	6.98	1.73	1.62	ns
	−2	0.49	6.13	0.03	0.96	0.32	5.41	6.13	1.52	1.43	ns
6 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	−1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	−2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
8 mA	Std.	0.66	4.77	0.04	1.29	0.43	4.55	4.77	2.38	2.55	ns
	−1	0.56	4.05	0.04	1.10	0.36	3.87	4.05	2.03	2.17	ns
	−2	0.49	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-65 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T$_J$ = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t$_{DOUT}$	t$_{DP}$	t$_{DIN}$	t$_{PY}$	t$_{EOUT}$	t$_{ZL}$	t$_{ZH}$	t$_{LZ}$	t$_{HZ}$	Units
2 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	−1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	−2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
4 mA	Std.	0.66	11.00	0.04	1.29	0.43	10.37	11.00	2.03	1.83	ns
	−1	0.56	9.35	0.04	1.10	0.36	8.83	9.35	1.73	1.56	ns
	−2	0.49	8.21	0.03	0.96	0.32	7.75	8.21	1.52	1.37	ns
6 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	−1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	−2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns
8 mA	Std.	0.66	7.50	0.04	1.29	0.43	7.36	7.50	2.39	2.46	ns
	−1	0.56	6.38	0.04	1.10	0.36	6.26	6.38	2.03	2.10	ns
	−2	0.49	5.60	0.03	0.96	0.32	5.49	5.60	1.78	1.84	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

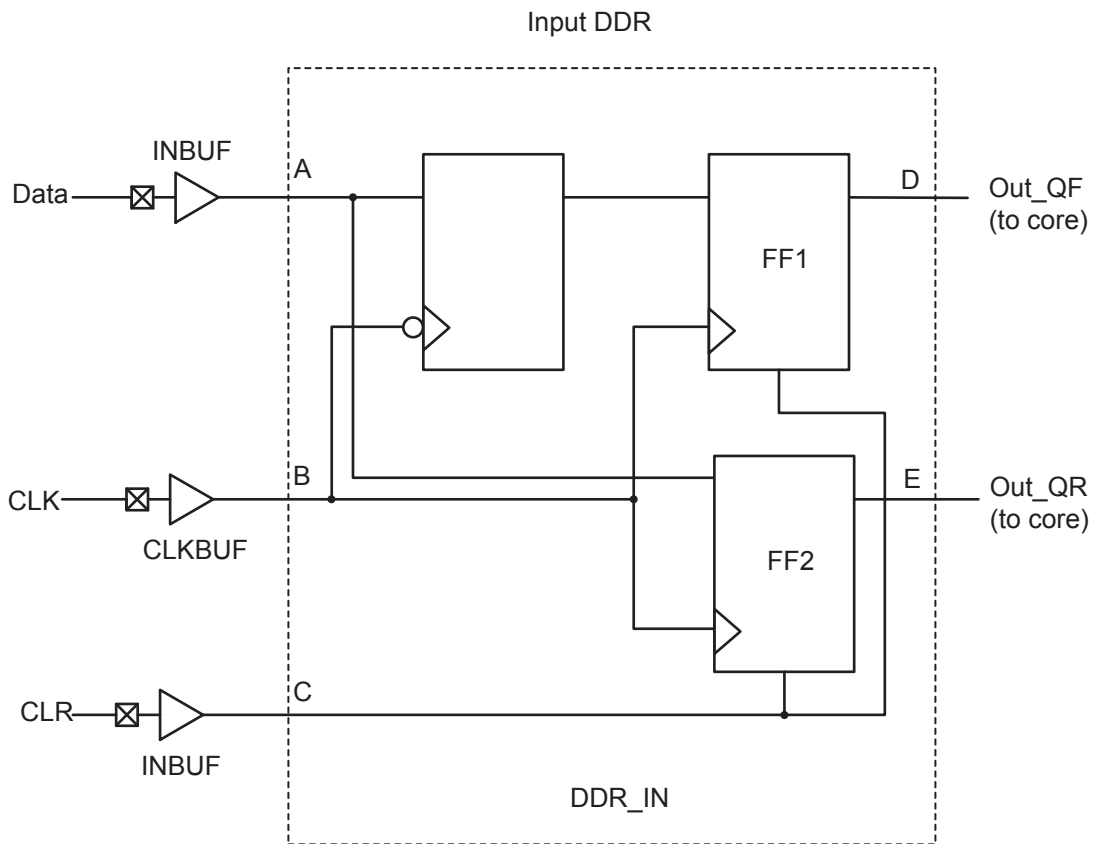## DDR Module Specifications

Input DDR Module

Figure 2-20 • **Input DDR Timing Model**

Table 2-101 • **Parameter Definitions**

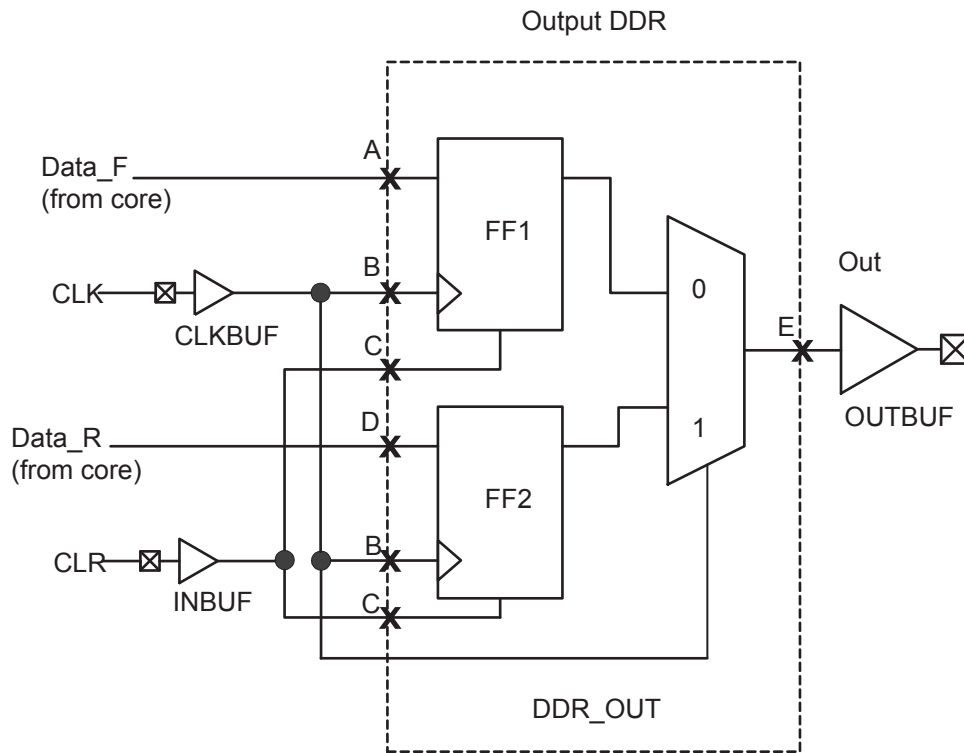| Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Output DDR Module

Figure 2-22 • **Output DDR Timing Model**

Table 2-103 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

QN132	
Pin Number	**A3P250 Function**
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TQ144	
Pin Number	**A3P125 Function**
109	GBA1/IO40RSB0
110	GBA0/IO39RSB0
111	GBB1/IO38RSB0
112	GBB0/IO37RSB0
113	GBC1/IO36RSB0
114	GBC0/IO35RSB0
115	IO34RSB0
116	IO33RSB0
117	VCCIB0
118	GND
119	VCC
120	IO29RSB0
121	IO28RSB0
122	IO27RSB0
123	IO25RSB0
124	IO23RSB0
125	IO21RSB0
126	IO19RSB0
127	IO17RSB0
128	IO16RSB0
129	IO14RSB0
130	IO12RSB0
131	IO10RSB0
132	IO08RSB0
133	IO06RSB0
134	VCCIB0
135	GND
136	VCC
137	GAC1/IO05RSB0
138	GAC0/IO04RSB0
139	GAB1/IO03RSB0
140	GAB0/IO02RSB0
141	GAA1/IO01RSB0
142	GAA0/IO00RSB0
143	GNDQ
144	VMV0

FG256	
Pin Number	**A3P250 Function**
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

FG256	
Pin Number	**A3P250 Function**
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

FG256	
Pin Number	**A3P250 Function**
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2

FG484 – Bottom View

A1 Ball Pad Corner
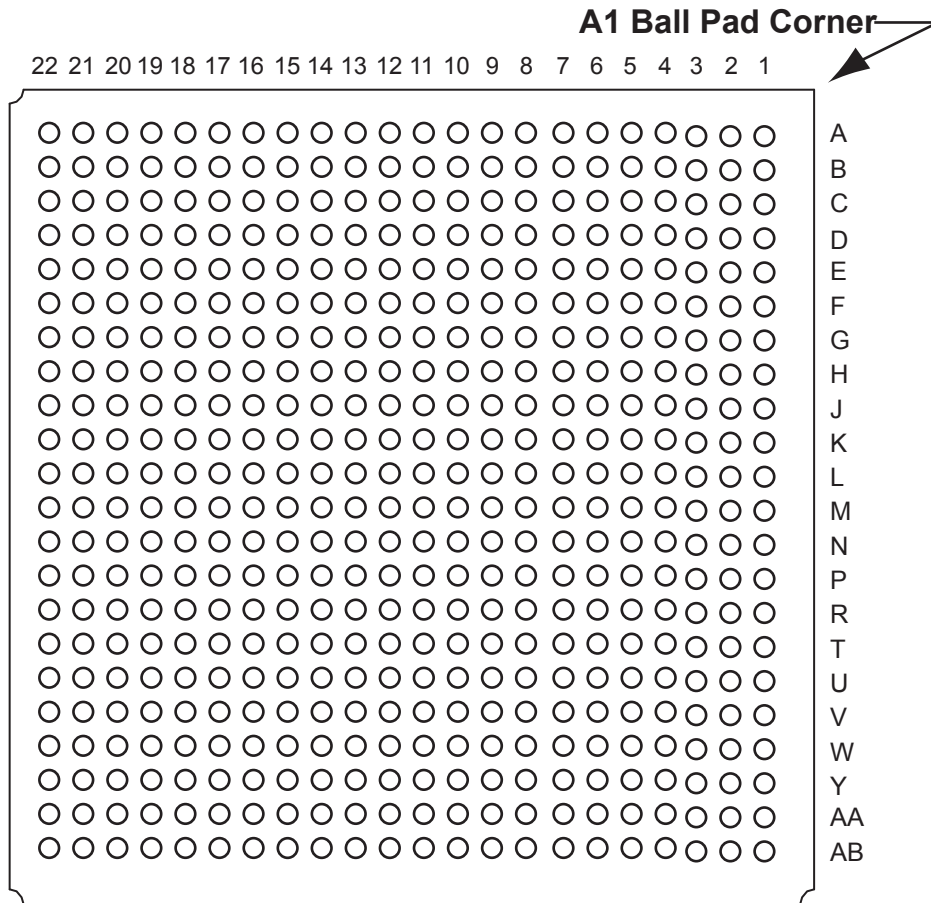
Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

FG484		FG484		FG484	
Pin Number	**A3P400 Function**	**Pin Number**	**A3P400 Function**	**Pin Number**	**A3P400 Function**
A1	GND	B15	NC	D7	GAB0/IO02RSB0
A2	GND	B16	NC	D8	IO16RSB0
A3	VCCIB0	B17	NC	D9	IO17RSB0
A4	NC	B18	NC	D10	IO22RSB0
A5	NC	B19	NC	D11	IO28RSB0
A6	IO15RSB0	B20	NC	D12	IO34RSB0
A7	IO18RSB0	B21	VCCIB1	D13	IO37RSB0
A8	NC	B22	GND	D14	IO41RSB0
A9	NC	C1	VCCIB3	D15	IO43RSB0
A10	IO23RSB0	C2	NC	D16	GBB1/IO57RSB0
A11	IO29RSB0	C3	NC	D17	GBA0/IO58RSB0
A12	IO35RSB0	C4	NC	D18	GBA1/IO59RSB0
A13	IO36RSB0	C5	GND	D19	GND
A14	NC	C6	NC	D20	NC
A15	NC	C7	NC	D21	NC
A16	IO50RSB0	C8	VCC	D22	NC
A17	IO51RSB0	C9	VCC	E1	NC
A18	NC	C10	NC	E2	NC
A19	NC	C11	NC	E3	GND
A20	VCCIB0	C12	NC	E4	GAB2/IO154UDB3
A21	GND	C13	NC	E5	GAA2/IO155UDB3
A22	GND	C14	VCC	E6	IO12RSB0
B1	GND	C15	VCC	E7	GAB1/IO03RSB0
B2	VCCIB3	C16	NC	E8	IO13RSB0
B3	NC	C17	NC	E9	IO14RSB0
B4	NC	C18	GND	E10	IO21RSB0
B5	NC	C19	NC	E11	IO27RSB0
B6	NC	C20	NC	E12	IO32RSB0
B7	NC	C21	NC	E13	IO38RSB0
B8	NC	C22	VCCIB1	E14	IO42RSB0
B9	NC	D1	NC	E15	GBC1/IO55RSB0
B10	NC	D2	NC	E16	GBB0/IO56RSB0
B11	NC	D3	NC	E17	IO44RSB0
B12	NC	D4	GND	E18	GBA2/IO60PDB1
B13	NC	D5	GAA0/IO00RSB0	E19	IO60NDB1
B14	NC	D6	GAA1/IO01RSB0	E20	GND

FG484		FG484		FG484	
Pin Number	**A3P400 Function**	**Pin Number**	**A3P400 Function**	**Pin Number**	**A3P400 Function**
E21	NC	G13	IO40RSB0	J5	IO149NPB3
E22	NC	G14	IO46RSB0	J6	IO09RSB0
F1	NC	G15	GNDQ	J7	IO152UDB3
F2	NC	G16	IO47RSB0	J8	VCCIB3
F3	NC	G17	GBB2/IO61PPB1	J9	GND
F4	IO154VDB3	G18	IO53RSB0	J10	VCC
F5	IO155VDB3	G19	IO63NDB1	J11	VCC
F6	IO11RSB0	G20	NC	J12	VCC
F7	IO07RSB0	G21	NC	J13	VCC
F8	GAC0/IO04RSB0	G22	NC	J14	GND
F9	GAC1/IO05RSB0	H1	NC	J15	VCCIB1
F10	IO20RSB0	H2	NC	J16	IO62NDB1
F11	IO24RSB0	H3	VCC	J17	IO49RSB0
F12	IO33RSB0	H4	IO150PDB3	J18	IO64PPB1
F13	IO39RSB0	H5	IO08RSB0	J19	IO66NDB1
F14	IO45RSB0	H6	IO153VDB3	J20	NC
F15	GBC0/IO54RSB0	H7	IO152VDB3	J21	NC
F16	IO48RSB0	H8	VMV0	J22	NC
F17	VMV0	H9	VCCIB0	K1	NC
F18	IO61NPB1	H10	VCCIB0	K2	NC
F19	IO63PDB1	H11	IO25RSB0	K3	NC
F20	NC	H12	IO31RSB0	K4	IO148NDB3
F21	NC	H13	VCCIB0	K5	IO148PDB3
F22	NC	H14	VCCIB0	K6	IO149PPB3
G1	NC	H15	VMV1	K7	GFC1/IO147PPB3
G2	NC	H16	GBC2/IO62PDB1	K8	VCCIB3
G3	NC	H17	IO65RSB1	K9	VCC
G4	IO151VDB3	H18	IO52RSB0	K10	GND
G5	IO151UDB3	H19	IO66PDB1	K11	GND
G6	GAC2/IO153UDB3	H20	VCC	K12	GND
G7	IO06RSB0	H21	NC	K13	GND
G8	GNDQ	H22	NC	K14	VCC
G9	IO10RSB0	J1	NC	K15	VCCIB1
G10	IO19RSB0	J2	NC	K16	GCC1/IO67PPB1
G11	IO26RSB0	J3	NC	K17	IO64NPB1
G12	IO30RSB0	J4	IO150NDB3	K18	IO73PDB1

FG484			FG484			FG484	
Pin Number	A3P600 Function		Pin Number	A3P600 Function		Pin Number	A3P600 Function
E21	NC		G13	IO40RSB0		J5	IO168NPB3
E22	NC		G14	IO45RSB0		J6	IO167PPB3
F1	NC		G15	GNDQ		J7	IO169PDB3
F2	NC		G16	IO50RSB0		J8	VCCIB3
F3	NC		G17	GBB2/IO61PPB1		J9	GND
F4	IO173NDB3		G18	IO53RSB0		J10	VCC
F5	IO174NDB3		G19	IO63NDB1		J11	VCC
F6	VMV3		G20	NC		J12	VCC
F7	IO07RSB0		G21	NC		J13	VCC
F8	GAC0/IO04RSB0		G22	NC		J14	GND
F9	GAC1/IO05RSB0		H1	NC		J15	VCCIB1
F10	IO20RSB0		H2	NC		J16	IO62NDB1
F11	IO24RSB0		H3	VCC		J17	IO64NPB1
F12	IO33RSB0		H4	IO166PDB3		J18	IO65PPB1
F13	IO39RSB0		H5	IO167NPB3		J19	IO66NDB1
F14	IO44RSB0		H6	IO172NDB3		J20	NC
F15	GBC0/IO54RSB0		H7	IO169NDB3		J21	IO68PDB1
F16	IO51RSB0		H8	VMV0		J22	IO68NDB1
F17	VMV0		H9	VCCIB0		K1	IO157PDB3
F18	IO61NPB1		H10	VCCIB0		K2	IO157NDB3
F19	IO63PDB1		H11	IO25RSB0		K3	NC
F20	NC		H12	IO31RSB0		K4	IO165NDB3
F21	NC		H13	VCCIB0		K5	IO165PDB3
F22	NC		H14	VCCIB0		K6	IO168PPB3
G1	IO170NDB3		H15	VMV1		K7	GFC1/IO164PPB3
G2	IO170PDB3		H16	GBC2/IO62PDB1		K8	VCCIB3
G3	NC		H17	IO67PPB1		K9	VCC
G4	IO171NDB3		H18	IO64PPB1		K10	GND
G5	IO171PDB3		H19	IO66PDB1		K11	GND
G6	GAC2/IO172PDB3		H20	VCC		K12	GND
G7	IO06RSB0		H21	NC		K13	GND
G8	GNDQ		H22	NC		K14	VCC
G9	IO10RSB0		J1	NC		K15	VCCIB1
G10	IO19RSB0		J2	NC		K16	GCC1/IO69PPB1
G11	IO26RSB0		J3	NC		K17	IO65NPB1
G12	IO30RSB0		J4	IO166NDB3		K18	IO75PDB1

FG484		FG484		FG484	
Pin Number	**A3P1000 Function**	**Pin Number**	**A3P1000 Function**	**Pin Number**	**A3P1000 Function**
E21	NC	G13	IO52RSB0	J5	IO218NDB3
E22	IO84PDB1	G14	IO60RSB0	J6	IO216PDB3
F1	NC	G15	GNDQ	J7	IO216NDB3
F2	IO215PDB3	G16	IO80NDB1	J8	VCCIB3
F3	IO215NDB3	G17	GBB2/IO79PDB1	J9	GND
F4	IO224NDB3	G18	IO79NDB1	J10	VCC
F5	IO225NDB3	G19	IO82NPB1	J11	VCC
F6	VMV3	G20	IO85PDB1	J12	VCC
F7	IO11RSB0	G21	IO85NDB1	J13	VCC
F8	GAC0/IO04RSB0	G22	NC	J14	GND
F9	GAC1/IO05RSB0	H1	NC	J15	VCCIB1
F10	IO25RSB0	H2	NC	J16	IO83NPB1
F11	IO36RSB0	H3	VCC	J17	IO86NPB1
F12	IO42RSB0	H4	IO217PDB3	J18	IO90PPB1
F13	IO49RSB0	H5	IO218PDB3	J19	IO87NDB1
F14	IO56RSB0	H6	IO221NDB3	J20	NC
F15	GBC0/IO72RSB0	H7	IO221PDB3	J21	IO89PDB1
F16	IO62RSB0	H8	VMV0	J22	IO89NDB1
F17	VMV0	H9	VCCIB0	K1	IO211PDB3
F18	IO78NDB1	H10	VCCIB0	K2	IO211NDB3
F19	IO81NDB1	H11	IO38RSB0	K3	NC
F20	IO82PPB1	H12	IO47RSB0	K4	IO210PPB3
F21	NC	H13	VCCIB0	K5	IO213NDB3
F22	IO84NDB1	H14	VCCIB0	K6	IO213PDB3
G1	IO214NDB3	H15	VMV1	K7	GFC1/IO209PPB3
G2	IO214PDB3	H16	GBC2/IO80PDB1	K8	VCCIB3
G3	NC	H17	IO83PPB1	K9	VCC
G4	IO222NDB3	H18	IO86PPB1	K10	GND
G5	IO222PDB3	H19	IO87PDB1	K11	GND
G6	GAC2/IO223PDB3	H20	VCC	K12	GND
G7	IO223NDB3	H21	NC	K13	GND
G8	GNDQ	H22	NC	K14	VCC
G9	IO23RSB0	J1	IO212NDB3	K15	VCCIB1
G10	IO29RSB0	J2	IO212PDB3	K16	GCC1/IO91PPB1
G11	IO33RSB0	J3	NC	K17	IO90NPB1
G12	IO46RSB0	J4	IO217NDB3	K18	IO88PDB1

Revision	Changes	Page
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68

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Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

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