



Welcome to [E-XFL.COM](https://www.e-xfl.com)

Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	97
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p600-fg144

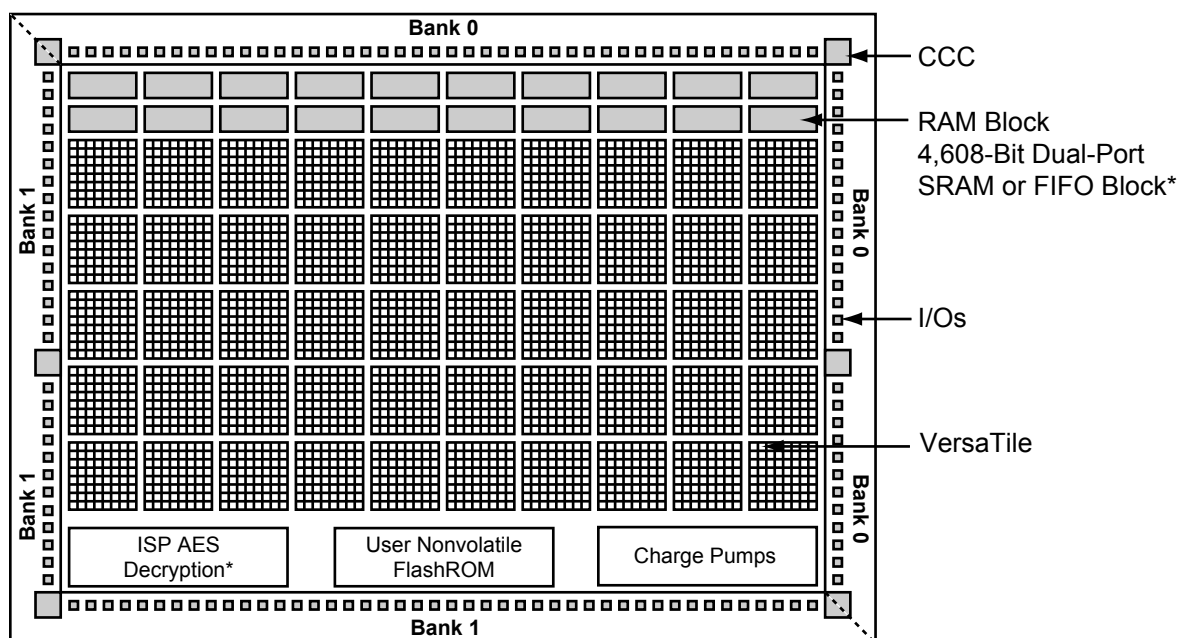
Advanced Flash Technology

The ProASIC3 family offers many benefits, including nonvolatility and reprogrammability through an advanced flash-based, 130-nm LVCMOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The ProASIC3 device consists of five distinct and programmable architectural features (Figure 1-1 and Figure 1-2 on page 1-4):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM/FIFO memory[†]
- Extensive CCCs and PLLs[†]
- Advanced I/O structure



Note: *Not supported by A3P015 and A3P030 devices

Figure 1-1 • ProASIC3 Device Architecture Overview with Two I/O Banks (A3P015, A3P030, A3P060, and A3P125)

[†] The A3P015 and A3P030 do not support PLL or SRAM.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

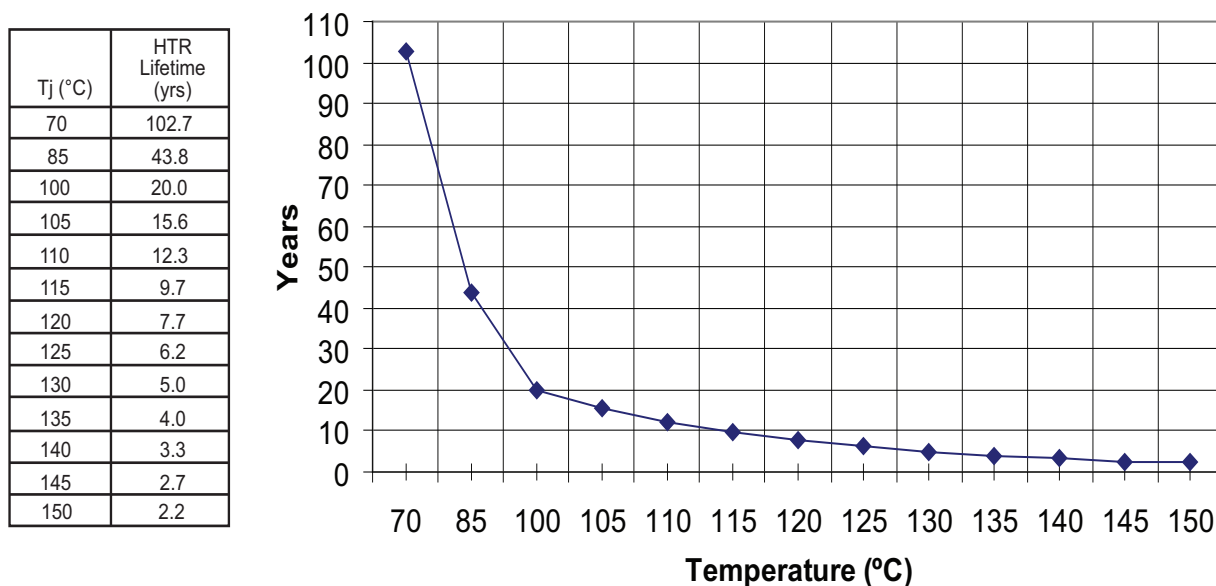
Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 300 μs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.



Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

Figure 2-1 • High-Temperature Data Retention (HTR)

Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature¹

Product Grade	Programming Cycles	Program Retention (biased/unbiased)	Maximum Storage Temperature T _{STG} (°C)	Maximum Operating Junction Temperature T _J (°C) ²
Commercial	500	20 years	110	100
Industrial	500	20 years	110	100

1. This is a stress rating only; functional operation at any condition other than those indicated is not implied.

2. These limits apply for program/data retention only. Refer to [Table 2-1 on page 2-1](#) and [Table 2-2](#) for device operating conditions and absolute limits.

Table 2-4 • Overshoot and Undershoot Limits¹

VCCI and VMV	Average VCCI–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle ²	Maximum Overshoot/Undershoot ²
2.7 V or less	10%	1.4 V
	5%	1.49 V
3 V	10%	1.1 V
	5%	1.19 V
3.3 V	10%	0.79 V
	5%	0.88 V
3.6 V	10%	0.45 V
	5%	0.54 V

Notes:

1. Based on reliability requirements at 85°C.

2. The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.

3. This table does not provide PCI overshoot/undershoot limits.

Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-10 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard I/O Banks

	VMV (V)	Static Power PDC2 (mW) ¹	Dynamic Power PAC9 (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range ³	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. PDC2 is the static power (where applicable) measured on VMV.
2. PAC9 is the total dynamic power measured on VCC and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	10.26	0.04	1.02	0.43	10.45	8.90	2.64	2.46	12.68	11.13	ns
	–1	0.56	8.72	0.04	0.86	0.36	8.89	7.57	2.25	2.09	10.79	9.47	ns
	–2	0.49	7.66	0.03	0.76	0.32	7.80	6.64	1.98	1.83	9.47	8.31	ns
4 mA	Std.	0.66	10.26	0.04	1.02	0.43	10.45	8.90	2.64	2.46	12.68	11.13	ns
	–1	0.56	8.72	0.04	0.86	0.36	8.89	7.57	2.25	2.09	10.79	9.47	ns
	–2	0.49	7.66	0.03	0.76	0.32	7.80	6.64	1.98	1.83	9.47	8.31	ns
6 mA	Std.	0.66	7.27	0.04	1.02	0.43	7.41	6.28	2.98	3.04	9.65	8.52	ns
	–1	0.56	6.19	0.04	0.86	0.36	6.30	5.35	2.54	2.59	8.20	7.25	ns
	–2	0.49	5.43	0.03	0.76	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
8 mA	Std.	0.66	7.27	0.04	1.02	0.43	7.41	6.28	2.98	3.04	9.65	8.52	ns
	–1	0.56	6.19	0.04	0.86	0.36	6.30	5.35	2.54	2.59	8.20	7.25	ns
	–2	0.49	5.43	0.03	0.76	0.32	5.53	4.69	2.23	2.27	7.20	6.36	ns
12 mA	Std.	0.66	5.58	0.04	1.02	0.43	5.68	4.87	3.21	3.42	7.92	7.11	ns
	–1	0.56	4.75	0.04	0.86	0.36	4.84	4.14	2.73	2.91	6.74	6.05	ns
	–2	0.49	4.17	0.03	0.76	0.32	4.24	3.64	2.39	2.55	5.91	5.31	ns
16 mA	Std.	0.66	5.21	0.04	1.02	0.43	5.30	4.56	3.26	3.51	7.54	6.80	ns
	–1	0.56	4.43	0.04	0.86	0.36	4.51	3.88	2.77	2.99	6.41	5.79	ns
	–2	0.49	3.89	0.03	0.76	0.32	3.96	3.41	2.43	2.62	5.63	5.08	ns
24 mA	Std.	0.66	4.85	0.04	1.02	0.43	4.94	4.54	3.32	3.88	7.18	6.78	ns
	–1	0.56	4.13	0.04	0.86	0.36	4.20	3.87	2.82	3.30	6.10	5.77	ns
	–2	0.49	3.62	0.03	0.76	0.32	3.69	3.39	2.48	2.90	5.36	5.06	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	15.86	0.04	1.54	0.43	15.86	13.51	4.09	3.80	19.25	16.90	ns
		–1	0.51	13.49	0.04	1.31	0.36	13.49	11.49	3.48	3.23	16.38	14.38	ns
		–2	0.45	11.84	0.03	1.15	0.32	11.84	10.09	3.05	2.84	14.38	12.62	ns
100 μA	4 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	6 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	8 mA	Std.	0.60	8.63	0.04	1.54	0.43	8.63	7.39	4.96	5.28	12.02	10.79	ns
		–1	0.51	7.34	0.04	1.31	0.36	7.34	6.29	4.22	4.49	10.23	9.18	ns
		–2	0.45	6.44	0.03	1.15	0.32	6.44	5.52	3.70	3.94	8.98	8.06	ns
100 μA	16 mA	Std.	0.60	8.05	0.04	1.54	0.43	8.05	6.93	5.03	5.43	11.44	10.32	ns
		–1	0.51	6.85	0.04	1.31	0.36	6.85	5.90	4.28	4.62	9.74	8.78	ns
		–2	0.45	6.01	0.03	1.15	0.32	6.01	5.18	3.76	4.06	8.55	7.71	ns
100 μA	24 mA	Std.	0.60	7.50	0.04	1.54	0.43	7.50	6.90	5.13	6.00	10.89	10.29	ns
		–1	0.51	6.38	0.04	1.31	0.36	6.38	5.87	4.36	5.11	9.27	8.76	ns
		–2	0.45	5.60	0.03	1.15	0.32	5.60	5.15	3.83	4.48	8.13	7.69	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-58 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

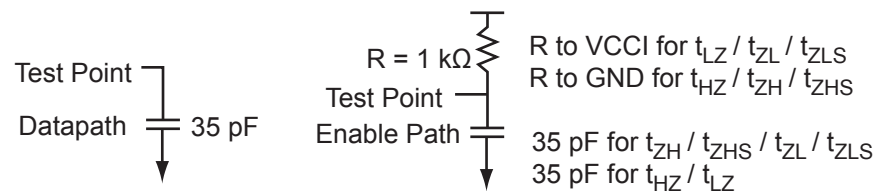


Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.

Table 2-96 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

Note: *See Figure 2-15 on page 2-69 for more information.

Table 2-109 • A3P060 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.71	0.93	0.81	1.05	0.95	1.24	ns
t_{RCKH}	Input High Delay for Global Clock	0.70	0.96	0.80	1.09	0.94	1.28	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-110 • A3P125 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.77	0.99	0.87	1.12	1.03	1.32	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.02	0.87	1.16	1.02	1.37	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-111 • A3P250 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.80	1.01	0.91	1.15	1.07	1.36	ns
t_{RCKH}	Input High Delay for Global Clock	0.78	1.04	0.89	1.18	1.04	1.39	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-112 • A3P400 Global Resource
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t_{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

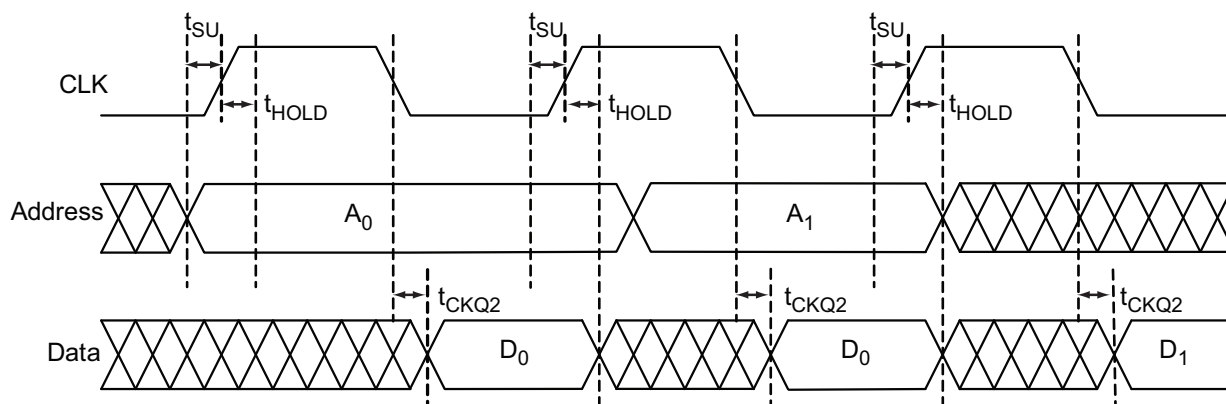
Table 2-121 • A3P250 FIFO 1k×4**Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.05	4.61	5.42	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

Table 2-123 • A3P250 FIFO 4k×1 (continued)**Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	-2	-1	Std.	Units
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on DO (pass-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on DO (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency	310	272	231	MHz

Embedded FlashROM Characteristics

**Figure 2-44 • Timing Diagram**

Timing Characteristics

Table 2-124 • Embedded FlashROM Access Time

Parameter	Description	-2	-1	Std.	Units
t_{SU}	Address Setup Time	0.53	0.61	0.71	ns
t_{HOLD}	Address Hold Time	0.00	0.00	0.00	ns
t_{CK2Q}	Clock to Out	21.42	24.40	28.68	ns
F_{MAX}	Maximum Clock Frequency	15	15	15	MHz

QN132	
Pin Number	A3P060 Function
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

PQ208	
Pin Number	A3P125 Function
109	TRST
110	VJTAG
111	GDA0/IO66RSB0
112	GDA1/IO65RSB0
113	GDB0/IO64RSB0
114	GDB1/IO63RSB0
115	GDC0/IO62RSB0
116	GDC1/IO61RSB0
117	NC
118	NC
119	NC
120	NC
121	NC
122	GND
123	VCCIB0
124	NC
125	NC
126	VCC
127	IO60RSB0
128	GCC2/IO59RSB0
129	GCB2/IO58RSB0
130	GND
131	GCA2/IO57RSB0
132	GCA0/IO56RSB0
133	GCA1/IO55RSB0
134	GCB0/IO54RSB0
135	GCB1/IO53RSB0
136	GCC0/IO52RSB0
137	GCC1/IO51RSB0
138	IO50RSB0
139	IO49RSB0
140	VCCIB0
141	GND
142	VCC
143	IO48RSB0
144	IO47RSB0

PQ208	
Pin Number	A3P125 Function
145	IO46RSB0
146	NC
147	NC
148	NC
149	GBC2/IO45RSB0
150	IO44RSB0
151	GBB2/IO43RSB0
152	IO42RSB0
153	GBA2/IO41RSB0
154	VMV0
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	VCCIB0
171	VCC
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0

PQ208	
Pin Number	A3P125 Function
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	VCCIB0
187	VCC
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

PQ208	
Pin Number	A3P250 Function
109	TRST
110	VJTAG
111	GDA0/IO60VDB1
112	GDA1/IO60UDB1
113	GDB0/IO59VDB1
114	GDB1/IO59UDB1
115	GDC0/IO58VDB1
116	GDC1/IO58UDB1
117	IO57VDB1
118	IO57UDB1
119	IO56NDB1
120	IO56PDB1
121	IO55RSB1
122	GND
123	VCCIB1
124	NC
125	NC
126	VCC
127	IO53NDB1
128	GCC2/IO53PDB1
129	GCB2/IO52PSB1
130	GND
131	GCA2/IO51PSB1
132	GCA1/IO50PDB1
133	GCA0/IO50NDB1
134	GCB0/IO49NDB1
135	GCB1/IO49PDB1
136	GCC0/IO48NDB1
137	GCC1/IO48PDB1
138	IO47NDB1
139	IO47PDB1
140	VCCIB1
141	GND
142	VCC
143	IO46RSB1
144	IO45NDB1

PQ208	
Pin Number	A3P250 Function
145	IO45PDB1
146	IO44NDB1
147	IO44PDB1
148	IO43NDB1
149	GBC2/IO43PDB1
150	IO42NDB1
151	GBB2/IO42PDB1
152	IO41NDB1
153	GBA2/IO41PDB1
154	VMV1
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	VCCIB0
171	VCC
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0

PQ208	
Pin Number	A3P250 Function
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	VCCIB0
187	VCC
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG144	
Pin Number	A3P060 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO04RSB0
A4	GAB1/IO05RSB0
A5	IO08RSB0
A6	GND
A7	IO11RSB0
A8	VCC
A9	IO16RSB0
A10	GBA0/IO23RSB0
A11	GBA1/IO24RSB0
A12	GNDQ
B1	GAB2/IO53RSB1
B2	GND
B3	GAA0/IO02RSB0
B4	GAA1/IO03RSB0
B5	IO00RSB0
B6	IO10RSB0
B7	IO12RSB0
B8	IO14RSB0
B9	GBB0/IO21RSB0
B10	GBB1/IO22RSB0
B11	GND
B12	VMV0
C1	IO95RSB1
C2	GFA2/IO83RSB1
C3	GAC2/IO94RSB1
C4	VCC
C5	IO01RSB0
C6	IO09RSB0
C7	IO13RSB0
C8	IO15RSB0
C9	IO17RSB0
C10	GBA2/IO25RSB0
C11	IO26RSB0
C12	GBC2/IO29RSB0

FG144	
Pin Number	A3P060 Function
D1	IO91RSB1
D2	IO92RSB1
D3	IO93RSB1
D4	GAA2/IO51RSB1
D5	GAC0/IO06RSB0
D6	GAC1/IO07RSB0
D7	GBC0/IO19RSB0
D8	GBC1/IO20RSB0
D9	GBB2/IO27RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	GCB1/IO37RSB0
E1	VCC
E2	GFC0/IO88RSB1
E3	GFC1/IO89RSB1
E4	VCCIB1
E5	IO52RSB1
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO35RSB0
E9	VCCIB0
E10	VCC
E11	GCA0/IO40RSB0
E12	IO30RSB0
F1	GFB0/IO86RSB1
F2	VCOMPLF
F3	GFB1/IO87RSB1
F4	IO90RSB1
F5	GND
F6	GND
F7	GND
F8	GCC0/IO36RSB0
F9	GCB0/IO38RSB0
F10	GND
F11	GCA1/IO39RSB0
F12	GCA2/IO41RSB0

FG144	
Pin Number	A3P060 Function
G1	GFA1/IO84RSB1
G2	GND
G3	VCCPLF
G4	GFA0/IO85RSB1
G5	GND
G6	GND
G7	GND
G8	GDC1/IO45RSB0
G9	IO32RSB0
G10	GCC2/IO43RSB0
G11	IO31RSB0
G12	GCB2/IO42RSB0
H1	VCC
H2	GFB2/IO82RSB1
H3	GFC2/IO81RSB1
H4	GEC1/IO77RSB1
H5	VCC
H6	IO34RSB0
H7	IO44RSB0
H8	GDB2/IO55RSB1
H9	GDC0/IO46RSB0
H10	VCCIB0
H11	IO33RSB0
H12	VCC
J1	GEB1/IO75RSB1
J2	IO78RSB1
J3	VCCIB1
J4	GEC0/IO76RSB1
J5	IO79RSB1
J6	IO80RSB1
J7	VCC
J8	TCK
J9	GDA2/IO54RSB1
J10	TDO
J11	GDA1/IO49RSB0
J12	GDB1/IO47RSB0

FG256	
Pin Number	A3P400 Function
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1

FG256	
Pin Number	A3P400 Function
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3

FG256	
Pin Number	A3P400 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2

FG484	
Pin Number	A3P600 Function
E21	NC
E22	NC
F1	NC
F2	NC
F3	NC
F4	IO173NDB3
F5	IO174NDB3
F6	VMV3
F7	IO07RSB0
F8	GAC0/IO04RSB0
F9	GAC1/IO05RSB0
F10	IO20RSB0
F11	IO24RSB0
F12	IO33RSB0
F13	IO39RSB0
F14	IO44RSB0
F15	GBC0/IO54RSB0
F16	IO51RSB0
F17	VMV0
F18	IO61NPB1
F19	IO63PDB1
F20	NC
F21	NC
F22	NC
G1	IO170NDB3
G2	IO170PDB3
G3	NC
G4	IO171NDB3
G5	IO171PDB3
G6	GAC2/IO172PDB3
G7	IO06RSB0
G8	GNDQ
G9	IO10RSB0
G10	IO19RSB0
G11	IO26RSB0
G12	IO30RSB0

FG484	
Pin Number	A3P600 Function
G13	IO40RSB0
G14	IO45RSB0
G15	GNDQ
G16	IO50RSB0
G17	GBB2/IO61PPB1
G18	IO53RSB0
G19	IO63NDB1
G20	NC
G21	NC
G22	NC
H1	NC
H2	NC
H3	VCC
H4	IO166PDB3
H5	IO167NPB3
H6	IO172NDB3
H7	IO169NDB3
H8	VMV0
H9	VCCIB0
H10	VCCIB0
H11	IO25RSB0
H12	IO31RSB0
H13	VCCIB0
H14	VCCIB0
H15	VMV1
H16	GBC2/IO62PDB1
H17	IO67PPB1
H18	IO64PPB1
H19	IO66PDB1
H20	VCC
H21	NC
H22	NC
J1	NC
J2	NC
J3	NC
J4	IO166NDB3

FG484	
Pin Number	A3P600 Function
J5	IO168NPB3
J6	IO167PPB3
J7	IO169PDB3
J8	VCCIB3
J9	GND
J10	VCC
J11	VCC
J12	VCC
J13	VCC
J14	GND
J15	VCCIB1
J16	IO62NDB1
J17	IO64NPB1
J18	IO65PPB1
J19	IO66NDB1
J20	NC
J21	IO68PDB1
J22	IO68NDB1
K1	IO157PDB3
K2	IO157NDB3
K3	NC
K4	IO165NDB3
K5	IO165PDB3
K6	IO168PPB3
K7	GFC1/IO164PPB3
K8	VCCIB3
K9	VCC
K10	GND
K11	GND
K12	GND
K13	GND
K14	VCC
K15	VCCIB1
K16	GCC1/IO69PPB1
K17	IO65NPB1
K18	IO75PDB1

FG484	
Pin Number	A3P600 Function
R17	GDB1/IO87PPB1
R18	GDC1/IO86PDB1
R19	IO84NDB1
R20	VCC
R21	IO81NDB1
R22	IO82PDB1
T1	IO152PDB3
T2	IO152NDB3
T3	NC
T4	IO150NDB3
T5	IO147PPB3
T6	GEC1/IO146PPB3
T7	IO140RSB2
T8	GNDQ
T9	GEA2/IO143RSB2
T10	IO126RSB2
T11	IO120RSB2
T12	IO108RSB2
T13	IO103RSB2
T14	IO99RSB2
T15	GNDQ
T16	IO92RSB2
T17	VJTAG
T18	GDC0/IO86NDB1
T19	GDA1/IO88PDB1
T20	NC
T21	IO83PDB1
T22	IO82NDB1
U1	IO149PDB3
U2	IO149NDB3
U3	NC
U4	GEB1/IO145PDB3
U5	GEB0/IO145NDB3
U6	VMV2
U7	IO138RSB2
U8	IO136RSB2

FG484	
Pin Number	A3P600 Function
U9	IO131RSB2
U10	IO124RSB2
U11	IO119RSB2
U12	IO107RSB2
U13	IO104RSB2
U14	IO97RSB2
U15	VMV1
U16	TCK
U17	VPUMP
U18	TRST
U19	GDA0/IO88NDB1
U20	NC
U21	IO83NDB1
U22	NC
V1	NC
V2	NC
V3	GND
V4	GEA1/IO144PDB3
V5	GEA0/IO144NDB3
V6	IO139RSB2
V7	GEC2/IO141RSB2
V8	IO132RSB2
V9	IO127RSB2
V10	IO121RSB2
V11	IO114RSB2
V12	IO109RSB2
V13	IO105RSB2
V14	IO98RSB2
V15	IO96RSB2
V16	GDB2/IO90RSB2
V17	TDI
V18	GNDQ
V19	TDO
V20	GND
V21	NC
V22	NC

FG484	
Pin Number	A3P600 Function
W1	NC
W2	IO148PDB3
W3	NC
W4	GND
W5	IO137RSB2
W6	GEB2/IO142RSB2
W7	IO134RSB2
W8	IO125RSB2
W9	IO123RSB2
W10	IO118RSB2
W11	IO115RSB2
W12	IO111RSB2
W13	IO106RSB2
W14	IO102RSB2
W15	GDC2/IO91RSB2
W16	IO93RSB2
W17	GDA2/IO89RSB2
W18	TMS
W19	GND
W20	NC
W21	NC
W22	NC
Y1	VCCIB3
Y2	IO148NDB3
Y3	NC
Y4	NC
Y5	GND
Y6	NC
Y7	NC
Y8	VCC
Y9	VCC
Y10	NC
Y11	NC
Y12	NC
Y13	NC
Y14	VCC

FG484	
Pin Number	A3P600 Function
Y15	VCC
Y16	NC
Y17	NC
Y18	GND
Y19	NC
Y20	NC
Y21	NC
Y22	VCCIB1
AA1	GND
AA2	VCCIB3
AA3	NC
AA4	NC
AA5	NC
AA6	IO135RSB2
AA7	IO133RSB2
AA8	NC
AA9	NC
AA10	NC
AA11	NC
AA12	NC
AA13	NC
AA14	NC
AA15	NC
AA16	IO101RSB2
AA17	NC
AA18	NC
AA19	NC
AA20	NC
AA21	VCCIB1
AA22	GND
AB1	GND
AB2	GND
AB3	VCCIB2
AB4	NC
AB5	NC
AB6	IO130RSB2

FG484	
Pin Number	A3P600 Function
AB7	IO128RSB2
AB8	IO122RSB2
AB9	IO116RSB2
AB10	NC
AB11	NC
AB12	IO113RSB2
AB13	IO112RSB2
AB14	NC
AB15	NC
AB16	IO100RSB2
AB17	IO95RSB2
AB18	NC
AB19	NC
AB20	VCCIB2
AB21	GND
AB22	GND