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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	110592
Number of I/O	97
Number of Gates	600000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/a3p600-fg144i

2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1] mA	IOH[1] mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points

Standard	Measuring Trip Point (V_{trip})
3.3 LTTL 3.3 LCMOS	1.4
3.3 LCMOS ide Range	1.4
2.5 LCMOS	1.2
1.8 LCMOS	0.90
1.5 LCMOS	0.75
3.3 PC	0.285 CC (RR)
	0.615 CC ()
3.3 PC	0.285 CC (RR)
	0.615 CC ()

Table 2-23 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay trough te Output uffer
t_{P}	Pad to Data delay trough te nput uffer
t_{DOUT}	Data to Output uffer delay trough te O interfae
t_{OUT}	nale to Output uffer Tristate Control delay trough te O interfae
t_{D}	nput uffer to Data delay trough te O interfae
t_{H}	nale to Pad delay trough te Output ufferHig to
t_{H}	nale to Pad delay trough te Output uffer to Hig
t_{L}	nale to Pad delay trough te Output ufferLo to
t_{L}	nale to Pad delay trough te Output uffer to Lo
t_{HS}	nale to Pad delay trough te Outp ut uffer it delayed enale to Hig
t_{LS}	nale to Pad delay trough te Outp ut uffer it delayed enale to Lo

Table 2-58 • Minimum and Maximum DC In put and Output Levels Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL [1]	IIH [2]
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA [3]	Max. mA [3]	µA [4]	µA [4]
2 mA	0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	0.3	0.7	1.7	3.6	0. 7	1.7	4	4	16	18	10	10
6 mA	0.3	0.7	1.7	3. 6	0.7	1.7	6	6	32	37	10	10
8 mA	0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

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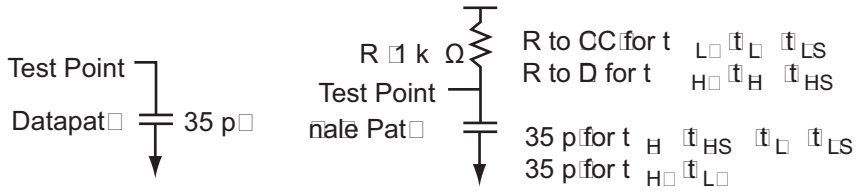

Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C LOAD (pF)
0	2.5	1.2	35

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Timing Characteristics

Table 2-70 • 1.8 V LVCMOS High Slew
Commercial-Case Conditions: T J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

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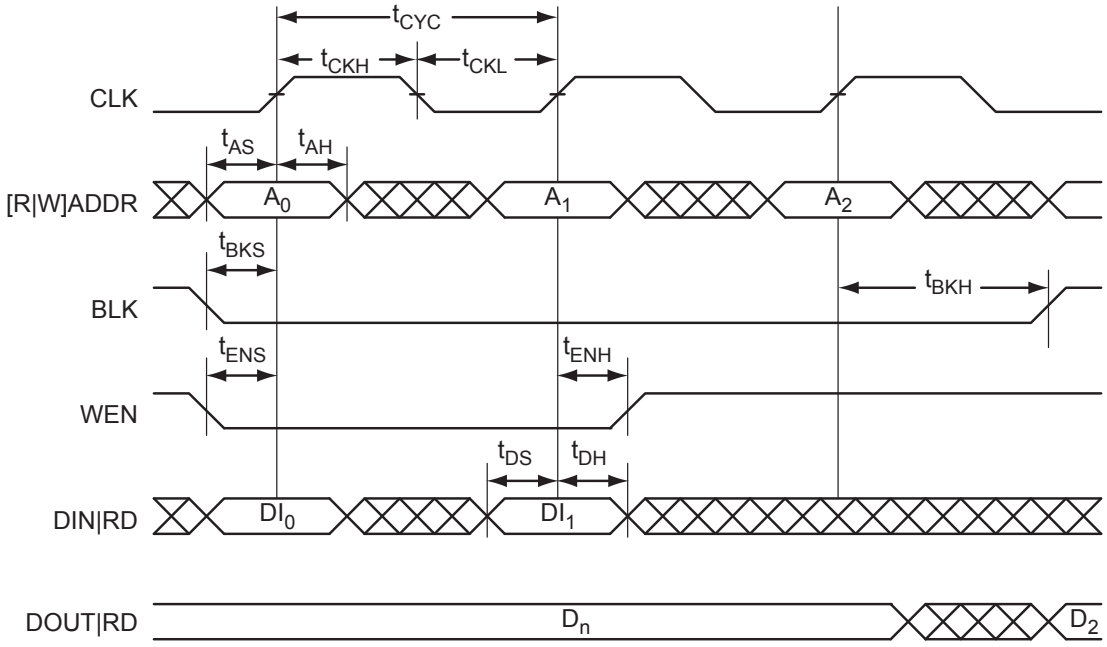

Figure 2-33 • **RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.**

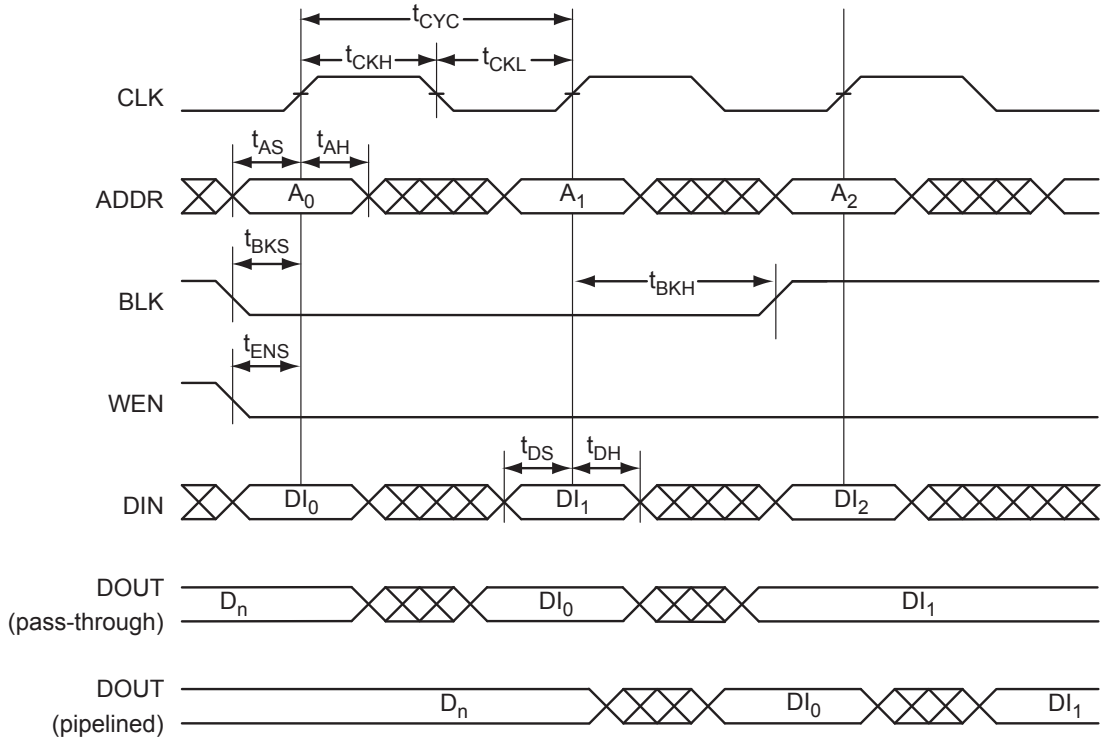

Figure 2-34 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 Only.**

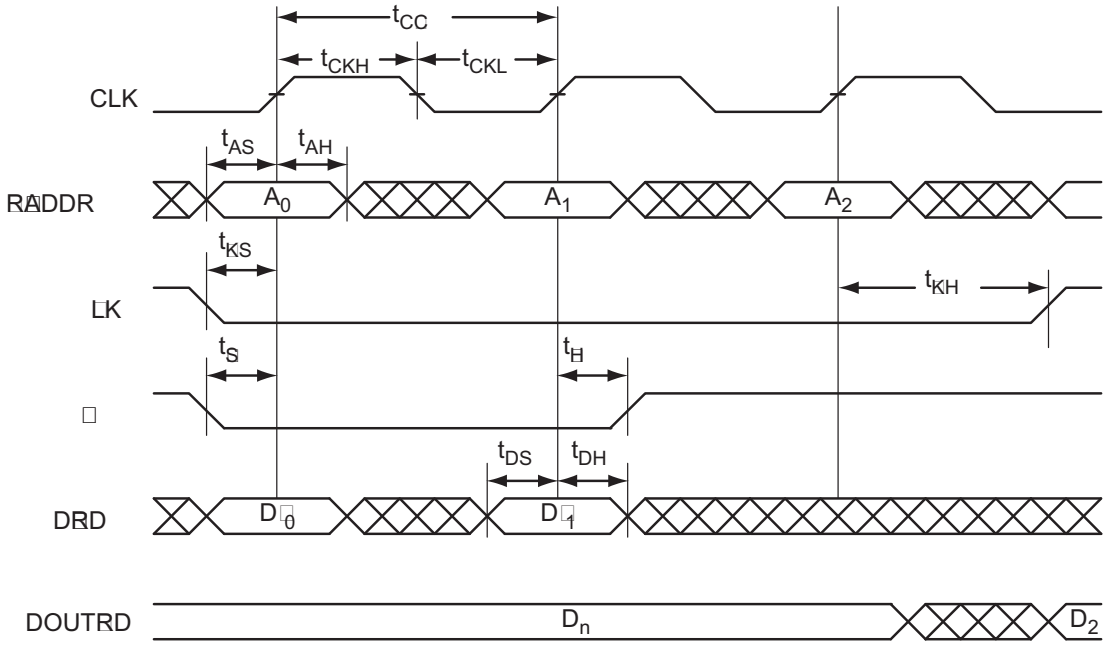

Figure 2-33 • RAM Write, Output Retained. Applicable to Both RAM4K9 and RAM512x18.

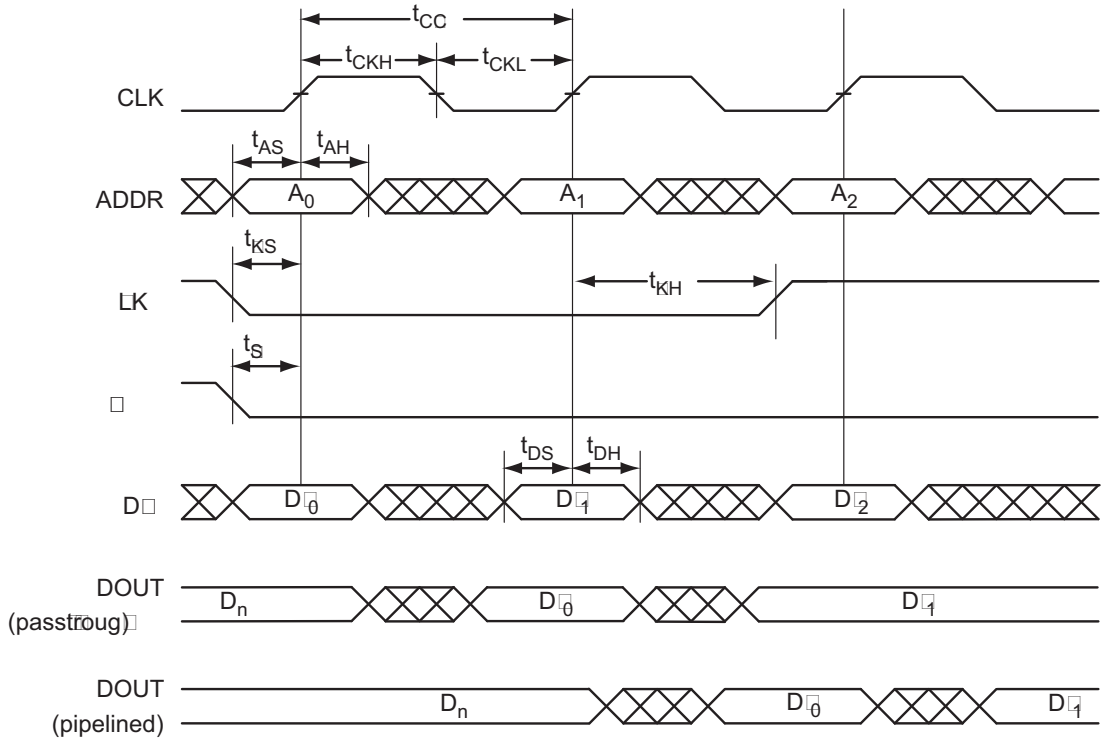

Figure 2-34 • RAM Write, Output as Write Data (WMO DE = 1). Applicable to RAM4K9 Only.

Timing Characteristics

Table 2-116 • RAM4K9
Commercial-Case Conditions: T J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	2	1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address old time	0.00	0.00	0.00	ns
t_{S}	R setup time	0.14	0.16	0.19	ns
t_{H}	R old time	0.10	0.11	0.13	ns
t_{KS}	LK setup time	0.23	0.27	0.31	ns
t_{KH}	LK old time	0.02	0.02	0.02	ns
t_{DS}	nput data (D) setup time	0.18	0.21	0.25	ns
t_{DH}	nput data (D) old time	0.00	0.00	0.00	ns
t_{CKQ1}	Clok Hig to ne data alid on DOUT (out put retained MOD 0)	2.36	2.68	3.15	ns
	Clok Hig to ne data alid on DOUT (f lotoug MOD 1)	1.79	2.03	2.39	ns
t_{CKQ2}	Clok Hig to ne data alid on DOUT (pipelined)	0.89	1.02	1.20	ns
t_{C2CL} [1]	Address ollision lktolk delay for reliale rite after rite on same addressAppliale to Closing dge	0.33	0.28	0.25	ns
t_{C2CH} [1]	Address ollision lktolk delay for reliale rite after rite on same addressAppliale to Rising dge	0.30	0.26	0.23	ns
t_{C2CRH} [1]	Address ollision lktolk delay for reliale read aess after rite on same addressAppliale to Opening dge	0.45	0.38	0.34	ns
t_{C2CRH} [1]	Address ollision lktolk delay for reliale rite aess after read on same address Appliale to Opening dge	0.49	0.42	0.37	ns
t_{RSTQ}	RST Lo to data out Lo on DOUT (flotoug)	0.92	1.05	1.23	ns
	RST Lo to Data Out Lo on DO UT (pipelined)	0.92	1.05	1.23	ns
t_{RMRST}	RST remoal	0.29	0.33	0.38	ns
t_{RCRST}	RST reoery	1.50	1.71	2.01	ns
t_{MPRST}	RST minimum pulse idt	0.21	0.24	0.29	ns
t_{CC}	Clok yle time	3.23	3.68	4.32	ns
MA	Maximum freueny	310	272	231	MH

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