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Understanding <u>Embedded - FPGAs (Field</u> <u>Programmable Gate Array)</u>

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	151
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p250-1pqg208i

Email: info@E-XFL.COM

Address: Room A, 16/F, Full Win Commercial Centre, 573 Nathan Road, Mongkok, Hong Kong



ProASIC3 Devices	A3P015 ¹	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Cortex-M1 Devices ²					M1A3P250	M1A3P400	M1A3P600	M1A3P1000
Package Pins QFN CS VQFP TQFP PQFP FBGA	QN68	QN48, QN68, QN132 ⁷ VQ100	QN132 ⁷ CS121 VQ100 TQ144 FG144	QN132 ⁷ VQ100 TQ144 PQ208 FG144	QN132 ⁷ VQ100 PQ208 FG144/256 ⁵	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484	PQ208 FG144/256/ 484

Notes:

- A3P015 is not recommended for new designs.
 Refer to the Cortex-M1 product brief for more information.
 AES is not available for Cortex-M1 ProASIC3 devices.
 Six chip (main) and three quadrant global networks are available for A3P060 and above.
 The M1A3P250 device does not support this package.
 For higher densities and support of additional features, refer to the ProASIC3E Flash Family FPGAs datasheet.
 Package not available.



2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 •	Absolute	Maximum	Ratings
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Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	-0.3 to 1.65	V
VJTAG	JTAG DC voltage	-0.3 to 3.75	V
VPUMP	Programming voltage	-0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	-0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	-0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	-0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V	V
		(when I/O hot insertion mode is enabled)	
		-0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.

2. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.

3. For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings

		Equiv.			VIL	VIH		VOL	VOH					
I/O Standard	Drive Strength	Software Default Drive Strength Option ²	Slew Rate	Min V	Max V	Min V	Max V	Max V	Min V	IOL ¹ mA	IOH ¹ mA			
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	-0.3	0.8	2	3.6	0.4	2.4	12	12			
3.3 V LVCMOS Wide Range ³	100 µA	12 mA	High	-0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1			
2.5 V LVCMOS	12 mA	12 mA	High	-0.3	0.7	1.7	2.7	0.7	1.7	12	12			
1.8 V LVCMOS	8 mA	8 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8			
1.5 V LVCMOS	4 mA	4 mA	High	-0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	4	4			
3.3 V PCI		Per PCI specifications												
3.3 V PCI-X		Per PCI-X specifications												

Applicable to Standard Plus I/O Banks

Notes:

1. Currents are measured at 85°C junction temperature.

2. 3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.

3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.



Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-37 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	-0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

- 3. Currents are measured at 100°C junction temperature and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Table 2-38 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

3.3 V LVTTL / 3.3 V LVCMOS	V	ΊL	V	ΊH	VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges

- 3. Currents are measured at 100°C junction temperature and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.



	745			O Dunk										
1.5 V LVCMOS	VIL		VIH		VIH		VOL	VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴		
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10		
4 mA	-0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10		

Table 2-77 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

Notes:

- 1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.
- 2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
- 3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.

Table 2-78 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.5 V LVCMOS		VIL	VIH	VIH		VOH	IOL	юн	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	-0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

2. IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.

3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.

- 4. Currents are measured at 85°C junction temperature.
- 5. Software default selection highlighted in gray.



Figure 2-10 • AC Loading

Table 2-79 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.5	0.75	35

Note: *Measuring point = V_{trip} . See Table 2-22 on page 2-22 for a complete table of trip points.



Table 2-83 • 1.5 V LVCMOS Low Slew

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{zHS}	Units
2 mA	Std.	0.66	12.08	0.04	1.42	0.43	12.01	12.08	2.72	2.43	14.24	14.31	ns
	-1	0.56	10.27	0.04	1.21	0.36	10.21	10.27	2.31	2.06	12.12	12.18	ns
	-2	0.49	9.02	0.03	1.06	0.32	8.97	9.02	2.03	1.81	10.64	10.69	ns
4 mA	Std.	0.66	9.28	0.04	1.42	0.43	9.45	8.91	3.04	3.00	11.69	11.15	ns
	-1	0.56	7.89	0.04	1.21	0.36	8.04	7.58	2.58	2.55	9.94	9.49	ns
	-2	0.49	6.93	0.03	1.06	0.32	7.06	6.66	2.27	2.24	8.73	8.33	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-84 • 1.5 V LVCMOS High Slew Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{zH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	7.65	0.04	1.42	0.43	6.31	7.65	2.45	2.45	ns
	-1	0.56	6.50	0.04	1.21	0.36	5.37	6.50	2.08	2.08	ns
	-2	0.49	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

Notes:

1. Software default selection highlighted in gray.

2. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-85 • 1.5 V LVCMOS Low Slew Commercial-Case Conditions

Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	Units
2 mA	Std.	0.66	12.33	0.04	1.42	0.43	11.79	12.33	2.45	2.32	ns
	–1	0.56	10.49	0.04	1.21	0.36	10.03	10.49	2.08	1.98	ns
	-2	0.49	9.21	0.03	1.06	0.32	8.81	9.21	1.83	1.73	ns



Input Register



Figure 2-17 • Input Register Timing Diagram

Timing Characteristics

Table 2-98 • Input Data Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ICLKQ}	Clock-to-Q of the Input Data Register	0.24	0.27	0.32	ns
t _{ISUD}	Data Setup Time for the Input Data Register	0.26	0.30	0.35	ns
t _{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t _{ISUE}	Enable Setup Time for the Input Data Register	0.37	0.42	0.50	ns
t _{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	0.00	ns
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.45	0.52	0.61	ns
t _{IREMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t _{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	0.00	ns
t _{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.22	0.25	0.30	ns
t _{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t _{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.25	0.30	ns
t _{ICKMPWH}	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.41	0.48	ns
t _{ICKMPWL}	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.37	0.43	ns



Timing Characteristics

Table 2-100 • Output Enable Register Propagation DelaysCommercial-Case Conditions: TJ = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{OECLKQ}	Clock-to-Q of the Output Enable Register	0.59	0.67	0.79	ns
t _{OESUD}	Data Setup Time for the Output Enable Register	0.31	0.36	0.42	ns
t _{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OESUE}	Enable Setup Time for the Output Enable Register	0.44	0.50	0.58	ns
t _{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OECLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	0.67	0.76	0.89	ns
t _{OEREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	0.00	ns
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.25	0.30	ns
t _{OECKMPWH}	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.41	0.48	ns
t _{OECKMPWL}	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.37	0.43	ns



VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.



Figure 2-24 • Sample of Combinatorial Cells



Timing Characteristics

Table 2-107 • A3P015 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		-2		-1		S	Std.	
Parameter	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.66	0.81	0.75	0.92	0.88	1.08	ns
t _{RCKH}	Input High Delay for Global Clock	0.67	0.84	0.76	0.96	0.89	1.13	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.25	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).

3. For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-108 • A3P030 Global Resource

Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

		-	-2		-1		Std.	
Parameter	Description	Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	Units
t _{RCKL}	Input Low Delay for Global Clock	0.67	0.81	0.76	0.92	0.89	1.09	ns
t _{RCKH}	Input High Delay for Global Clock	0.68	0.85	0.77	0.97	0.91	1.14	ns
t _{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t _{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t _{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.24	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).

2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).



Embedded SRAM and FIFO Characteristics

SRAM



Figure 2-30 • RAM Models



FIFO



Figure 2-36 • FIFO Model



Timing Characteristics

Table 2-118 • FIFO (for all dies except A3P250)Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
t _{ENS}	REN, WEN Setup Time	1.34	1.52	1.79	ns
t _{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t _{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t _{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t _{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t _{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t _{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t _{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t _{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t _{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t _{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t _{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t _{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t _{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t _{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t _{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t _{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t _{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F _{MAX}	Maximum Frequency for FIFO	310	272	231	MHz



VJTAG

JTAG Supply Voltage

Low power flash devices have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design.

If the JTAG interface is neither used nor planned for use, the VJTAG pin together with the TRST pin could be tied to GND.

It should be noted that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a device is in a JTAG chain of interconnected boards, the board containing the device can be powered down, provided both VJTAG and VCC to the part remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

VPUMP Programming Supply Voltage

ProASIC3 devices support single-voltage ISP of the configuration flash and FlashROM. For programming, VPUMP should be 3.3 V nominal. During normal device operation, VPUMP can be left floating or can be tied (pulled up) to any voltage between 0 V and the VPUMP maximum. Programming power supply voltage (VPUMP) range is listed in Table 2-2 on page 2-2.

When the VPUMP pin is tied to ground, it will shut off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry.

For proper programming, 0.01 μ F and 0.33 μ F capacitors (both rated at 16 V) are to be connected in parallel across VPUMP and GND, and positioned as close to the FPGA pins as possible.

Microsemi recommends that VPUMP and VJTAG power supplies be kept separate with independent filtering capacitors rather than supplying them from a common rail.

User Pins

I/O

User Input/Output

The I/O pin functions as an input, output, tristate, or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected.

During programming, I/Os become tristated and weakly pulled up to V_{CCI} . With V_{CCI} , VMV, and V_{CC} supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration.

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

GL Globals

GL I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities. Unused GL pins are configured as inputs with pull-up resistors.

See more detailed descriptions of global I/O connectivity in the "Clock Conditioning Circuits in IGLOO and ProASIC3 Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide*. All inputs labeled GC/GF are direct inputs into the quadrant clocks. For example, if GAA0 is used for an input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals. The inputs to the global network are multiplexed, and only one input can be used as a global input.

Refer to the I/O Structure section of the handbook for the device you are using for an explanation of the naming of global pins.

FF Flash*Freeze Mode Activation Pin

Flash*Freeze is available on IGLOO, ProASIC3L, and RT ProASIC3 devices. It is not supported on ProASIC3/E devices. The FF pin is a dedicated input pin used to enter and exit Flash*Freeze mode. The FF pin is active-low, has the same characteristics as a single-ended I/O, and must meet the maximum rise and fall times. When Flash*Freeze



Package Pin Assignments

QN132						
Pin Number	A3P060 Function					
C17	IO57RSB1					
C18	NC					
C19	ТСК					
C20	VMV1					
C21	VPUMP					
C22	VJTAG					
C23	VCCIB0					
C24	NC					
C25	NC					
C26	GCA1/IO42RSB0					
C27	GCC0/IO39RSB0					
C28	VCCIB0					
C29	IO29RSB0					
C30	GNDQ					
C31	GBA1/IO27RSB0					
C32	GBB0/IO24RSB0					
C33	VCC					
C34	IO19RSB0					
C35	IO16RSB0					
C36	IO13RSB0					
C37	GAC1/IO10RSB0					
C38	NC					
C39	GAA0/IO05RSB0					
C40	VMV0					
D1	GND					
D2	GND					
D3	GND					
D4	GND					

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Package Pin Assignments

PQ208			PQ208	PQ208		
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function	
109	TRST	145	IO45PDB1	181	IO21RSB0	
110	VJTAG	146	IO44NDB1	182	IO20RSB0	
111	GDA0/IO60VDB1	147	IO44PDB1	183	IO19RSB0	
112	GDA1/IO60UDB1	148	IO43NDB1	184	IO18RSB0	
113	GDB0/IO59VDB1	149	GBC2/IO43PDB1	185	IO17RSB0	
114	GDB1/IO59UDB1	150	IO42NDB1	186	VCCIB0	
115	GDC0/IO58VDB1	151	GBB2/IO42PDB1	187	VCC	
116	GDC1/IO58UDB1	152	IO41NDB1	188	IO16RSB0	
117	IO57VDB1	153	GBA2/IO41PDB1	189	IO15RSB0	
118	IO57UDB1	154	VMV1	190	IO14RSB0	
119	IO56NDB1	155	GNDQ	191	IO13RSB0	
120	IO56PDB1	156	GND	192	IO12RSB0	
121	IO55RSB1	157	NC	193	IO11RSB0	
122	GND	158	GBA1/IO40RSB0	194	IO10RSB0	
123	VCCIB1	159	GBA0/IO39RSB0	195	GND	
124	NC	160	GBB1/IO38RSB0	196	IO09RSB0	
125	NC	161	GBB0/IO37RSB0	197	IO08RSB0	
126	VCC	162	GND	198	IO07RSB0	
127	IO53NDB1	163	GBC1/IO36RSB0	199	IO06RSB0	
128	GCC2/IO53PDB1	164	GBC0/IO35RSB0	200	VCCIB0	
129	GCB2/IO52PSB1	165	IO34RSB0	201	GAC1/IO05RSB0	
130	GND	166	IO33RSB0	202	GAC0/IO04RSB0	
131	GCA2/IO51PSB1	167	IO32RSB0	203	GAB1/IO03RSB0	
132	GCA1/IO50PDB1	168	IO31RSB0	204	GAB0/IO02RSB0	
133	GCA0/IO50NDB1	169	IO30RSB0	205	GAA1/IO01RSB0	
134	GCB0/IO49NDB1	170	VCCIB0	206	GAA0/IO00RSB0	
135	GCB1/IO49PDB1	171	VCC	207	GNDQ	
136	GCC0/IO48NDB1	172	IO29RSB0	208	VMV0	
137	GCC1/IO48PDB1	173	IO28RSB0			
138	IO47NDB1	174	IO27RSB0			
139	IO47PDB1	175	IO26RSB0			
140	VCCIB1	176	IO25RSB0			
141	GND	177	IO24RSB0			
142	VCC	178	GND			
143	IO46RSB1	179	IO23RSB0			
144	IO45NDB1	180	IO22RSB0			

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Package Pin Assignments

PQ208		P	Q208	PQ208		
Pin Number	A3P400 Function	Pin Number	A3P400 Function	Pin Number	A3P400 Function	
109	TRST	145	IO64PDB1	181	IO27RSB0	
110	VJTAG	146	IO63NDB1	182	IO26RSB0	
111	GDA0/IO79VDB1	147	IO63PDB1	183	IO25RSB0	
112	GDA1/IO79UDB1	148	IO62NDB1	184	IO24RSB0	
113	GDB0/IO78VDB1	149	GBC2/IO62PDB1	185	IO23RSB0	
114	GDB1/IO78UDB1	150	IO61NDB1	186	VCCIB0	
115	GDC0/IO77VDB1	151	GBB2/IO61PDB1	187	VCC	
116	GDC1/IO77UDB1	152	IO60NDB1	188	IO21RSB0	
117	IO76VDB1	153	GBA2/IO60PDB1	189	IO20RSB0	
118	IO76UDB1	154	VMV1	190	IO19RSB0	
119	IO75NDB1	155	GNDQ	191	IO18RSB0	
120	IO75PDB1	156	GND	192	IO17RSB0	
121	IO74RSB1	157	VMV0	193	IO16RSB0	
122	GND	158	GBA1/IO59RSB0	194	IO15RSB0	
123	VCCIB1	159	GBA0/IO58RSB0	195	GND	
124	NC	160	GBB1/IO57RSB0	196	IO13RSB0	
125	NC	161	GBB0/IO56RSB0	197	IO11RSB0	
126	VCC	162	GND	198	IO09RSB0	
127	IO72NDB1	163	GBC1/IO55RSB0	199	IO07RSB0	
128	GCC2/IO72PDB1	164	GBC0/IO54RSB0	200	VCCIB0	
129	GCB2/IO71PSB1	165	IO52RSB0	201	GAC1/IO05RSB0	
130	GND	166	IO49RSB0	202	GAC0/IO04RSB0	
131	GCA2/IO70PSB1	167	IO46RSB0	203	GAB1/IO03RSB0	
132	GCA1/IO69PDB1	168	IO43RSB0	204	GAB0/IO02RSB0	
133	GCA0/IO69NDB1	169	IO40RSB0	205	GAA1/IO01RSB0	
134	GCB0/IO68NDB1	170	VCCIB0	206	GAA0/IO00RSB0	
135	GCB1/IO68PDB1	171	VCC	207	GNDQ	
136	GCC0/IO67NDB1	172	IO36RSB0	208	VMV0	
137	GCC1/IO67PDB1	173	IO35RSB0			
138	IO66NDB1	174	IO34RSB0			
139	IO66PDB1	175	IO33RSB0			
140	VCCIB1	176	IO32RSB0			
141	GND	177	IO31RSB0			
142	VCC	178	GND			
143	IO65RSB1	179	IO29RSB0			
144	IO64NDB1	180	IO28RSB0			



Revision	Changes	Page
Revision 13 (January 2013)	The "ProASIC3 Ordering Information" section has been updated to mention "Y" as "Blank" mentioning "Device Does Not Include License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio" (SAR 43104).	1-IV
	Added a note to Table 2-2 • Recommended Operating Conditions 1 (SAR 43644): The programming temperature range supported is $T_{ambient} = 0^{\circ}C$ to 85°C.	2-2
	The note in Table 2-115 • ProASIC3 CCC/PLL Specification referring the reader to SmartGen was revised to refer instead to the online help associated with the core (SAR 42569).	2-90
	Libero Integrated Design Environment (IDE) was changed to Libero System-on- Chip (SoC) throughout the document (SAR 40284).	NA
Revision 12 (September 2012)	The Security section was modified to clarify that Microsemi does not support read-back of programmed data.	1-1
	Added a Note stating "VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information" to Table 2-1 • Absolute Maximum Ratings and Table 2-2 • Recommended Operating Conditions 1 (SAR 38321).	2-1 2-2
	Table 2-35 • Duration of Short Circuit Event Before Failure was revised to change the maximum temperature from 110°C to 100°C, with an example of six months instead of three months (SAR 37933).	2-31
	In Table 2-93 • Minimum and Maximum DC Input and Output Levels, VIL and VIH were revised so that the maximum is 3.6 V for all listed values of VCCI (SAR 28549).	2-68
	Figure 2-37 • FIFO Read and Figure 2-38 • FIFO Write are new (SAR 28371).	2-99
	The following sentence was removed from the "VMVx I/O Supply Voltage (quiet)" section in the "Pin Descriptions" chapter: "Within the package, the VMV plane is decoupled from the simultaneous switching noise originating from the output buffer VCCI domain" and replaced with "Within the package, the VMV plane biases the input stage of the I/Os in the I/O banks" (SAR 38321). The datasheet mentions that "VMV pins must be connected to the corresponding VCCI pins" for an ESD enhancement.	3-1

Revision	Changes	Page
Advance v0.2,	Table 2-43 was updated.	2-64
(continued)	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68



Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3 Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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