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## Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

## Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

| Details | |
|---|---|
| Product Status | Active |
| Number of LABs/CLBs | - |
| Number of Logic Elements/Cells | - |
| Total RAM Bits | 36864 |
| Number of I/O | 97 |
| Number of Gates | 250000 |
| Voltage - Supply | 1.425V ~ 1.575V |
| Mounting Type | Surface Mount |
| Operating Temperature | 0°C ~ 85°C (TJ) |
| Package / Case | 144-LBGA |
| Supplier Device Package | 144-FPBGA (13x13) |
| Purchase URL | https://www.e-xfl.com/product-detail/microchip-technology/m1a3p250-2fg144 |

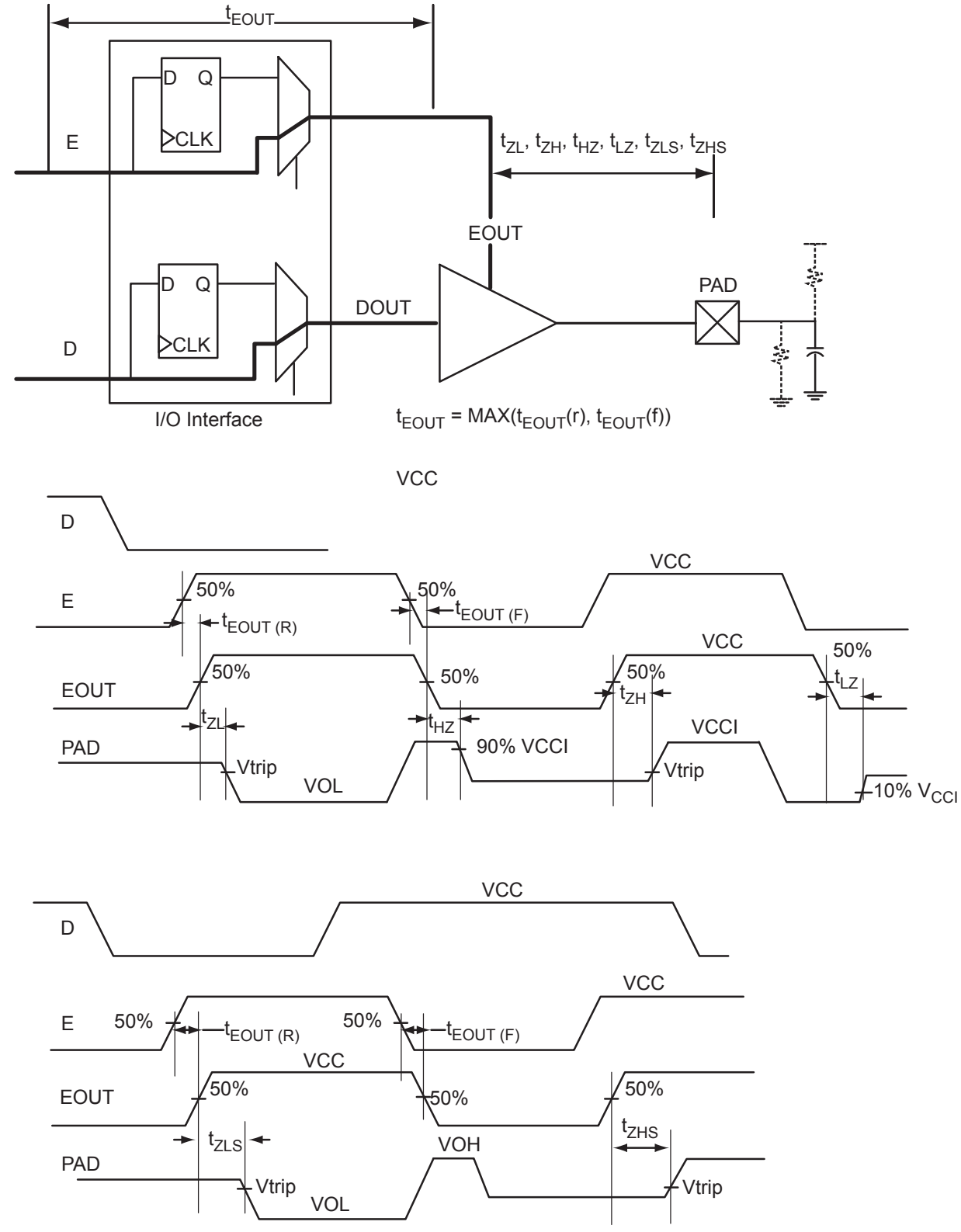


***Figure 2-6 •*** **Tristate Output Buffer Timing Model and Delays (Example)**

**Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –2 Speed Grade, Commercial-Case Conditions: $T_J$ = 70°C, Worst Case VCC = 1.425 V, Worst-Case VCCI (per standard) Advanced I/O Banks**

| I/O Standard | Drive Strength | Equiv. Software Default Drive Strength Option[1] | Slew Rate | Capacitive Load (pF) | External Resistor ( : ) | $t_{DOUT}$ (ns) | $t_{DP}$ (ns) | $t_{DIN}$ (ns) | $t_{PY}$ (ns) | $t_{EOUT}$ (ns) | $t_{ZL}$ (ns) | $t_{ZH}$ (ns) | $t_{LZ}$ (ns) | $t_{HZ}$ (ns) | $t_{ZLS}$ (ns) | $t_{ZHS}$ (ns) | Units |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 3.3 V LVTTL / 3.3 V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 2.64 | 0.03 | 0.76 | 0.32 | 2.69 | 2.11 | 2.40 | 2.68 | 4.36 | 3.78 | ns |
| 3.3 V LVCMOS Wide Range[2] | 100 µA | 12 mA | High | 35 | – | 0.45 | 4.08 | 0.03 | 0.76 | 0.32 | 4.08 | 3.20 | 3.71 | 4.14 | 6.61 | 5.74 | ns |
| 2.5 V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 2.66 | 0.03 | 0.98 | 0.32 | 2.71 | 2.56 | 2.47 | 2.57 | 4.38 | 4.23 | ns |
| 1.8 V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 2.64 | 0.03 | 0.91 | 0.32 | 2.69 | 2.27 | 2.76 | 3.05 | 4.36 | 3.94 | ns |
| 1.5 V LVCMOS | 12 mA | 12 mA | High | 35 | – | 0.45 | 3.05 | 0.03 | 1.07 | 0.32 | 3.10 | 2.67 | 2.95 | 3.14 | 4.77 | 4.34 | ns |
| 3.3 V PCI | Per PCI spec | – | High | 10 | 25 [4] | 0.45 | 2.00 | 0.03 | 0.65 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| 3.3 V PCI-X | Per PCI-X spec | – | High | 10 | 25 [4] | 0.45 | 2.00 | 0.03 | 0.62 | 0.32 | 2.04 | 1.46 | 2.40 | 2.68 | 3.71 | 3.13 | ns |
| LVDS | 24 mA | – | High | – | – | 0.45 | 1.37 | 0.03 | 1.20 | – | – | – | – | – | – | – | ns |
| LVPECL | 24 mA | – | High | – | – | 0.45 | 1.34 | 0.03 | 1.05 | – | – | – | – | – | – | – | ns |

*Notes:*

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-64 for connectivity. This resistor is not required during normal operation.*

Table 2-39 • Minimum and Maximum DC In put and Output Levels
Applicable to Standard I/O Banks

| 3.3 V LVTTL / 3.3 V LVCMOS | VIL | | VIH | | VOL | VOH | IOL | IOH | IOSL | IOSH | IIL [1] | IIH [2] |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| Drive Strength | Min V | Max V | Min V | Max V | Max V | Min V | mA | mA | Max mA [3] | Max mA [3] | µA [4] | µA [4] |
| 2 mA | 0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 2 | 2 | 25 | 27 | 10 | 10 |
| 4 mA | 0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 4 | 4 | 25 | 27 | 10 | 10 |
| 6 mA | 0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 6 | 6 | 51 | 54 | 10 | 10 |
| 8 mA | 0.3 | 0.8 | 2 | 3.6 | 0.4 | 2.4 | 8 | 8 | 51 | 54 | 10 | 10 |

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where 0.3 V < VIN < VIL.
2. $I_{IH}$ is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges
3. Currents are measured at 100°C junction temperature and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

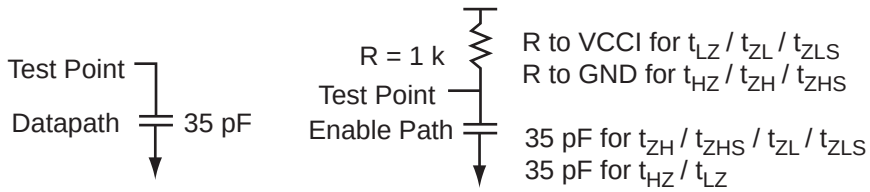


Figure 2-7 • AC Loading

Table 2-40 • AC Waveforms, Measuring Points, and Capacitive Loads

| Input Low (V) | Input High (V) | Measuring Point* (V) | $C_{LOAD}$ (pF) |
|---|---|---|---|
| 0 | 3.3 | 1.4 | 35 |

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.

## Output DDR Module

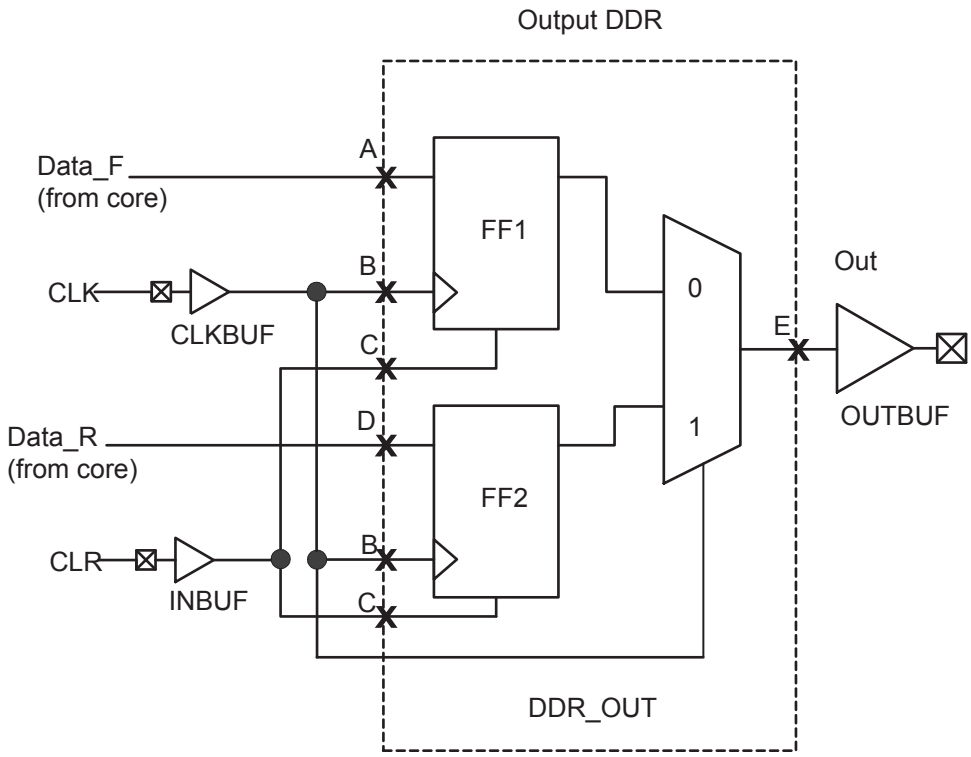


***Figure 2-22 •*** **Output DDR Timing Model**

***Table 2-103 •*** **Parameter Definitions**

| Parameter Name | Parameter Definition | Measuring Nodes (from, to) |
|---|---|---|
| $t_{DDROCLKQ}$ | Clock-to-Out | B, E |
| $t_{DDROCLR2Q}$ | Asynchronous Clear-to-Out | C, E |
| $t_{DDROREMCLR}$ | Clear Removal | C, B |
| $t_{DDRORECCLR}$ | Clear Recovery | C, B |
| $t_{DDROSUD1}$ | Data Setup Data_F | A, B |
| $t_{DDROSUD2}$ | Data Setup Data_R | D, B |
| $t_{DDROHD1}$ | Data Hold Data_F | A, B |
| $t_{DDROHD2}$ | Data Hold Data_R | D, B |

## Timing Characteristics

***Table 2-107* • A3P015 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.66 | 0.81 | 0.75 | 0.92 | 0.88 | 1.08 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.67 | 0.84 | 0.76 | 0.96 | 0.89 | 1.13 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.25 | ns |

***Notes:***

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-108* • A3P030 Global Resource**
**Commercial-Case Conditions: $T_J$ = 70°C, VCC = 1.425 V**

| Parameter | Description | –2 | | –1 | | Std. | | Units |
|---|---|---|---|---|---|---|---|---|
| | | Min.[1] | Max.[2] | Min.[1] | Max.[2] | Min.[1] | Max.[2] | |
| $t_{RCKL}$ | Input Low Delay for Global Clock | 0.67 | 0.81 | 0.76 | 0.92 | 0.89 | 1.09 | ns |
| $t_{RCKH}$ | Input High Delay for Global Clock | 0.68 | 0.85 | 0.77 | 0.97 | 0.91 | 1.14 | ns |
| $t_{RCKMPWH}$ | Minimum Pulse Width High for Global Clock | 0.75 | | 0.85 | | 1.00 | | ns |
| $t_{RCKMPWL}$ | Minimum Pulse Width Low for Global Clock | 0.85 | | 0.96 | | 1.13 | | ns |
| $t_{RCKSW}$ | Maximum Skew for Global Clock | | 0.18 | | 0.21 | | 0.24 | ns |

*Notes:*

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

## Timing Waveforms

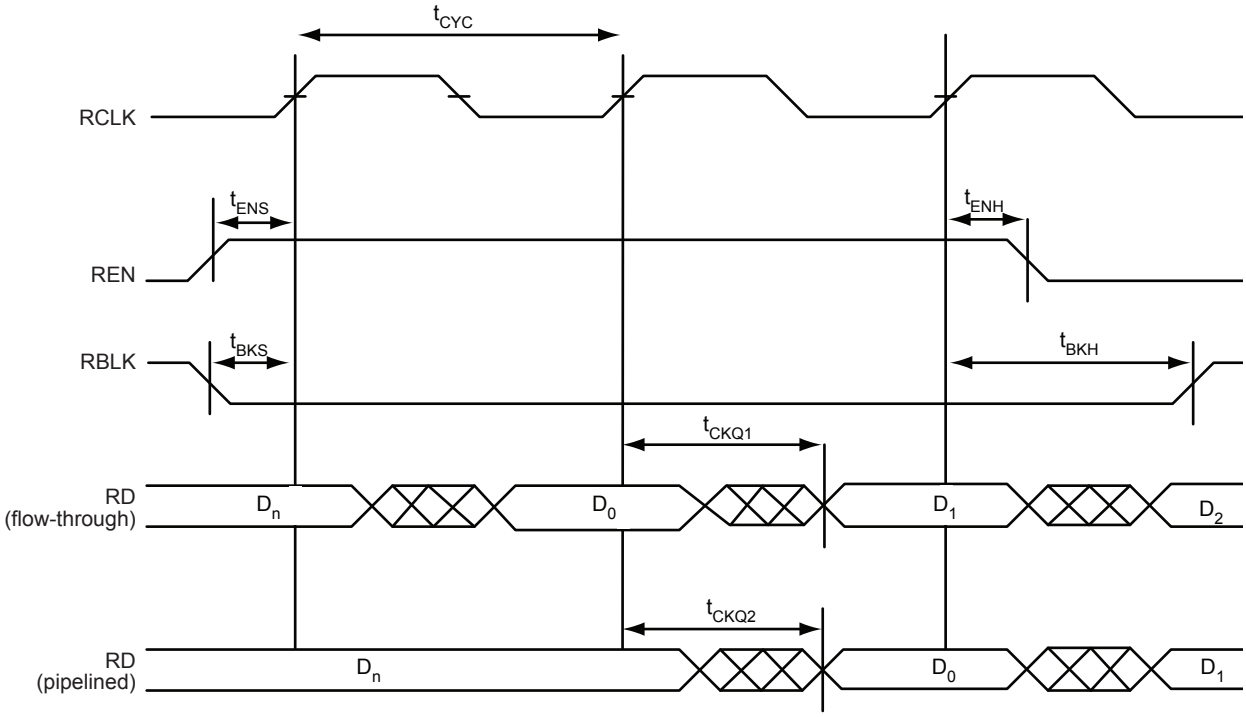


***Figure 2-37 •*** **FIFO Read**

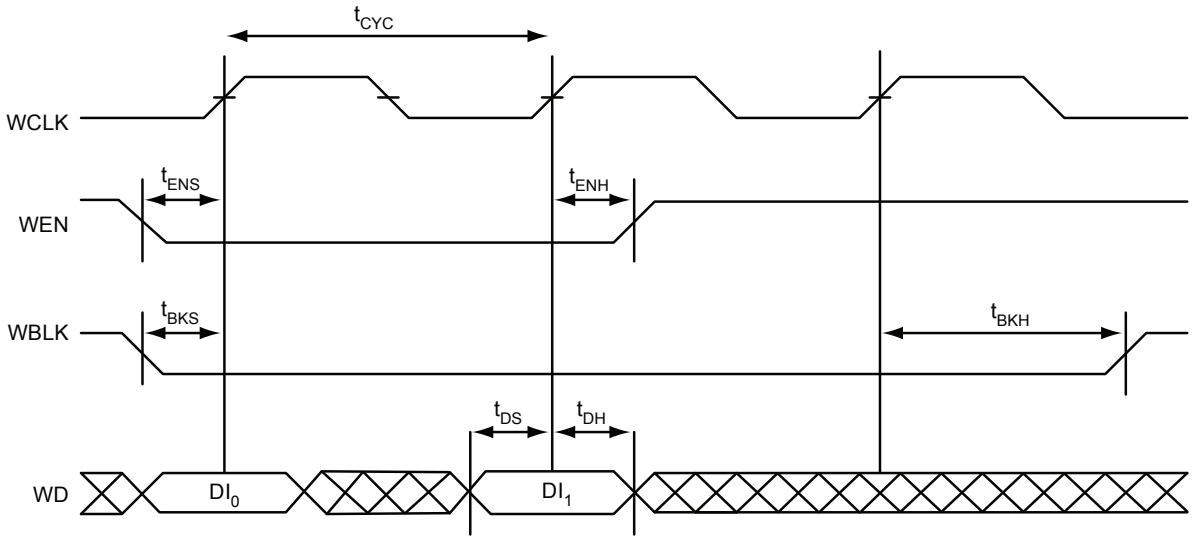


***Figure 2-38 •*** **FIFO Write**

| FG256 | |
|---|---|
| **Pin Number** | **A3P1000 Function** |
| R5 | IO168RSB2 |
| R6 | IO163RSB2 |
| R7 | IO157RSB2 |
| R8 | IO149RSB2 |
| R9 | IO143RSB2 |
| R10 | IO138RSB2 |
| R11 | IO131RSB2 |
| R12 | IO125RSB2 |
| R13 | GDB2/IO115RSB2 |
| R14 | TDI |
| R15 | GNDQ |
| R16 | TDO |
| T1 | GND |
| T2 | IO183RSB2 |
| T3 | GEB2/IO186RSB2 |
| T4 | IO172RSB2 |
| T5 | IO170RSB2 |
| T6 | IO164RSB2 |
| T7 | IO158RSB2 |
| T8 | IO153RSB2 |
| T9 | IO142RSB2 |
| T10 | IO135RSB2 |
| T11 | IO130RSB2 |
| T12 | GDC2/IO116RSB2 |
| T13 | IO120RSB2 |
| T14 | GDA2/IO114RSB2 |
| T15 | TMS |
| T16 | GND |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| K19 | IO88NDB1 |
| K20 | IO94NPB1 |
| K21 | IO98NDB1 |
| K22 | IO98PDB1 |
| L1 | NC |
| L2 | IO200PDB3 |
| L3 | IO210NPB3 |
| L4 | GFB0/IO208NPB3 |
| L5 | GFA0/IO207NDB3 |
| L6 | GFB1/IO208PPB3 |
| L7 | VCOMPLF |
| L8 | GFC0/IO209NPB3 |
| L9 | VCC |
| L10 | GND |
| L11 | GND |
| L12 | GND |
| L13 | GND |
| L14 | VCC |
| L15 | GCC0/IO91NPB1 |
| L16 | GCB1/IO92PPB1 |
| L17 | GCA0/IO93NPB1 |
| L18 | IO96NPB1 |
| L19 | GCB0/IO92NPB1 |
| L20 | IO97PDB1 |
| L21 | IO97NDB1 |
| L22 | IO99NPB1 |
| M1 | NC |
| M2 | IO200NDB3 |
| M3 | IO206NDB3 |
| M4 | GFA2/IO206PDB3 |
| M5 | GFA1/IO207PDB3 |
| M6 | VCCPLF |
| M7 | IO205NDB3 |
| M8 | GFB2/IO205PDB3 |
| M9 | VCC |
| M10 | GND |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| M11 | GND |
| M12 | GND |
| M13 | GND |
| M14 | VCC |
| M15 | GCB2/IO95PPB1 |
| M16 | GCA1/IO93PPB1 |
| M17 | GCC2/IO96PPB1 |
| M18 | IO100PPB1 |
| M19 | GCA2/IO94PPB1 |
| M20 | IO101PPB1 |
| M21 | IO99PPB1 |
| M22 | NC |
| N1 | IO201NDB3 |
| N2 | IO201PDB3 |
| N3 | NC |
| N4 | GFC2/IO204PDB3 |
| N5 | IO204NDB3 |
| N6 | IO203NDB3 |
| N7 | IO203PDB3 |
| N8 | VCCIB3 |
| N9 | VCC |
| N10 | GND |
| N11 | GND |
| N12 | GND |
| N13 | GND |
| N14 | VCC |
| N15 | VCCIB1 |
| N16 | IO95NPB1 |
| N17 | IO100NPB1 |
| N18 | IO102NDB1 |
| N19 | IO102PDB1 |
| N20 | NC |
| N21 | IO101NPB1 |
| N22 | IO103PDB1 |
| P1 | NC |
| P2 | IO199PDB3 |

| FG484 | |
|---|---|
| Pin Number | A3P1000 Function |
| P3 | IO199NDB3 |
| P4 | IO202NDB3 |
| P5 | IO202PDB3 |
| P6 | IO196PPB3 |
| P7 | IO193PPB3 |
| P8 | VCCIB3 |
| P9 | GND |
| P10 | VCC |
| P11 | VCC |
| P12 | VCC |
| P13 | VCC |
| P14 | GND |
| P15 | VCCIB1 |
| P16 | GDB0/IO112NPB1 |
| P17 | IO106NDB1 |
| P18 | IO106PDB1 |
| P19 | IO107PDB1 |
| P20 | NC |
| P21 | IO104PDB1 |
| P22 | IO103NDB1 |
| R1 | NC |
| R2 | IO197PPB3 |
| R3 | VCC |
| R4 | IO197NPB3 |
| R5 | IO196NPB3 |
| R6 | IO193NPB3 |
| R7 | GEC0/IO190NPB3 |
| R8 | VMV3 |
| R9 | VCCIB2 |
| R10 | VCCIB2 |
| R11 | IO147RSB2 |
| R12 | IO136RSB2 |
| R13 | VCCIB2 |
| R14 | VCCIB2 |
| R15 | VMV2 |
| R16 | IO110NDB1 |

| Revision | Changes | Page |
|---|---|---|
| Revision 2 (cont'd) | The "ProASIC3 FPGAs Package Sizes Dimensions" table is new. | III |
| | In the "ProASIC3 Ordering Information", the QN package measurements were updated to include both 0.4 mm and 0.5 mm. | IV |
| | In the General Description section the number of I/Os was updated from 288 to 300. | 1-1 |
| Packaging v1.2 | The "QN68 Bottom View" section is new. | 4-3 |
| Revision 1 (Feb 2008)<br>DC and Switching Characteristics v1.1 | In Table 2-2 Recommended Operating Conditions 1, $T_J$ was listed in the symbol column and was incorrect. It was corrected and changed to $T_A$. | 2-2 |
| | In Table 2-3 Flash Programming Limits Retention, Storage and Operating Temperature, Maximum Operating Junction Temperature was changed from 110°C to 100°C for both commercial and industrial grades. | 2-3 |
| | The "PLL Behavior at Brownout Condition" section is new. | 2-4 |
| | In the "PLL Contribution PPLL" section , the following was deleted:<br>FCLKIN is the input clock frequency. | 2-14 |
| | In Table 2-21 Summary of Maximum and Minimum DC Input Levels, the note was incorrect. It previously said $T_J$ and it was corrected and changed to $T_A$. | 2-21 |
| | In Table 2-115 ProASIC3 CCC/PLL Specification, the SCLK parameter and note 1 are new. | 2-90 |
| | Table 2-125 JTAG 1532 was populated with the parameter data, which was not in the previous version of the document. | 2-108 |
| Packaging v1.1 | In the "VQ100" A3P030 pin table, the function of pin 63 was incorrect and changed from IO39RSB0 to GDB0/IO38RSB0. | 4-19 |
| Revision 0 (Jan 2008) | This document was previously in datasheet v2.2. As a result of moving to the handbook format, Actel has restarted the version numbers. | N/A |
| v2.2<br>(July 2007) | The M7 and M1 device part numbers have been updated in Table 1 ProASIC3 Product Family, "I/Os Per Package", "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix". | i, ii, iii, iii, iv |
| | The words "ambient temperature" were added to the temperature range in the "Automotive ProASIC3 Ordering Information", "Temperature Grade Offerings", and "Speed Grade and Temperature Grade Matrix" sections. | iii, iv |
| | The $T_J$ parameter in Table 3-2 Recommended Operating Conditions was changed to $T_A$, ambient temperature, and table notes 4 6 were added. | 3-2 |
| v2.1<br>(May 2007) | In the "Clock Conditioning Circuit (CCC) and PLL" section, the Wide Input Frequency Range (1.5 MHz to 200 MHz) was changed to (1.5 MHz to 350 MHz). | i |
| | The "Clock Conditioning Circuit (CCC) and PLL" section was updated. | i |
| | In the "I/Os Per Package" section, the A3P030, A3P060, A3P125, ACP250, and A3P600 device I/Os were updated. | ii |
| | Table 3-5 Package Thermal Resistivities was updated with A3P1000 information. The note below the table is also new. | 3-5 |