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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	36864
Number of I/O	68
Number of Gates	250000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	100-TQFP
Supplier Device Package	100-VQFP (14x14)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m1a3p250-vqg100

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time = 300 μs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × (350 MHz / f_{OUT_CCC}) (for PLL only)

Global Clocking

ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high fanout nets.

2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+125	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-4 on page 2-3](#).
2. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on [page 3-1](#) for further information.
3. For flash programming and retention maximum limits, refer to [Table 2-3 on page 2-3](#), and for recommended operating limits, refer to [Table 2-2 on page 2-2](#).

The absolute maximum junction temperature is 100°C. EQ 1 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja} (\text{°C/W})} = \frac{100^{\circ}\text{C} - 70^{\circ}\text{C}}{20.5^{\circ}\text{C/W}} = 1.463 \text{ W}$$

EQ 1

Table 2-5 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft/min	500 ft/min	
Quad Flat No Lead	A3P030	132	0.4	21.4	16.8	15.3	°C/W
	A3P060	132	0.3	21.2	16.6	15.0	°C/W
	A3P125	132	0.2	21.1	16.5	14.9	°C/W
	A3P250	132	0.1	21.0	16.4	14.8	°C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Thin Quad Flat Pack (TQFP)	All devices	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)	All devices	208	8.0	26.1	22.5	20.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

Note: *This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays
 (normalized to $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425 \text{ V}$)

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.88	0.93	0.95	1.00	1.02	1.04
1.500	0.83	0.88	0.90	0.95	0.96	0.98
1.575	0.80	0.84	0.87	0.91	0.93	0.94

Calculating Power Dissipation

Quiescent Supply Current

Table 2-7 • Quiescent Supply Current Characteristics

	A3P015	A3P030	A3P060	A3P125	A3P250	A3P400	A3P600	A3P1000
Typical (25°C)	2 mA	2 mA	2 mA	2 mA	3 mA	3 mA	5 mA	8 mA
Max. (Commercial)	10 mA	10 mA	10 mA	10 mA	20 mA	20 mA	30 mA	50 mA
Max. (Industrial)	15 mA	15 mA	15 mA	15 mA	30 mA	30 mA	45 mA	75 mA

Note: I_{DD} Includes V_{CC} , V_{PUMP} , V_{CCI} , and V_{MV} currents. Values do not include I/O static contribution, which is shown in [Table 2-11](#) and [Table 2-12](#) on page 2-9.

Power per I/O Pin

**Table 2-8 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Advanced I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power $PAC9$ (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.22
3.3 V LVCMOS Wide Range ³	3.3	–	16.22
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. $PAC9$ is the total dynamic power measured on V_{CC} and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

**Table 2-9 • Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings
Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power $PAC9$ (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.23
3.3 V LVCMOS Wide Range ³	3.3	–	16.23

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. $PAC9$ is the total dynamic power measured on V_{CC} and VMV.
3. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • Summary of AC Measuring Points

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
3.3 V LVCMOS Wide Range	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCI (RR)
	0.615 * VCCI (FF)
3.3 V PCI-X	0.285 * VCCI (RR)
	0.615 * VCCI (FF)

Table 2-23 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t_{DP}	Data to Pad delay through the Output Buffer
t_{PY}	Pad to Data delay through the Input Buffer
t_{DOUT}	Data to Output Buffer delay through the I/O interface
t_{EOUT}	Enable to Output Buffer Tristate Control delay through the I/O interface
t_{DIN}	Input Buffer to Data delay through the I/O interface
t_{HZ}	Enable to Pad delay through the Output Buffer—High to Z
t_{ZH}	Enable to Pad delay through the Output Buffer—Z to High
t_{LZ}	Enable to Pad delay through the Output Buffer—Low to Z
t_{ZL}	Enable to Pad delay through the Output Buffer—Z to Low
t_{ZHS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to High
t_{ZLS}	Enable to Pad delay through the Output Buffer with delayed enable—Z to Low

Table 2-58 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA ³	Max. mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	−0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	−0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	−0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges.
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

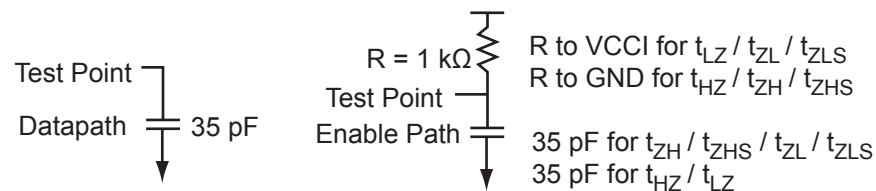


Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	2.5	1.2	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-66 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	8	8	51	45	10	10
12 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	12	12	74	91	10	10
16 mA	−0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI − 0.45	16	16	74	91	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Table 2-67 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL ¹	IIH ²
Drive Strength	Min V	Max V	Min V	Max V	Max V	Min V	mA	mA	Max mA ³	Max mA ³	μA ⁴	μA ⁴
2 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	2	2	11	9	10	10
4 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	4	4	22	17	10	10
6 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	6	6	44	35	10	10
8 mA	−0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI − 0.45	8	8	44	35	10	10

Notes:

1. IIL is the input leakage current per I/O pin over recommended operation conditions where $-0.3\text{ V} < V_{IN} < V_{IL}$.
2. IIH is the input leakage current per I/O pin over recommended operating conditions $V_{IH} < V_{IN} < V_{CCI}$. Input current is larger when operating outside recommended ranges
3. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
4. Currents are measured at 85°C junction temperature.
5. Software default selection highlighted in gray.

Output Enable Register

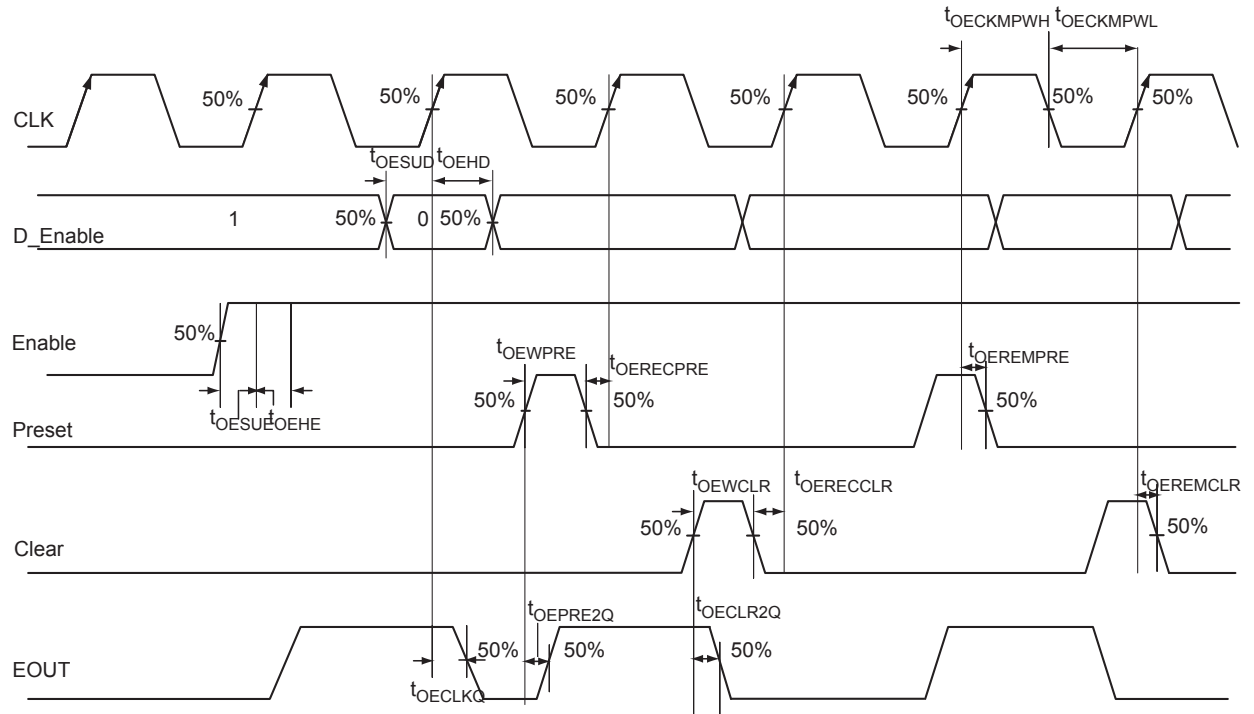


Figure 2-19 • Output Enable Register Timing Diagram

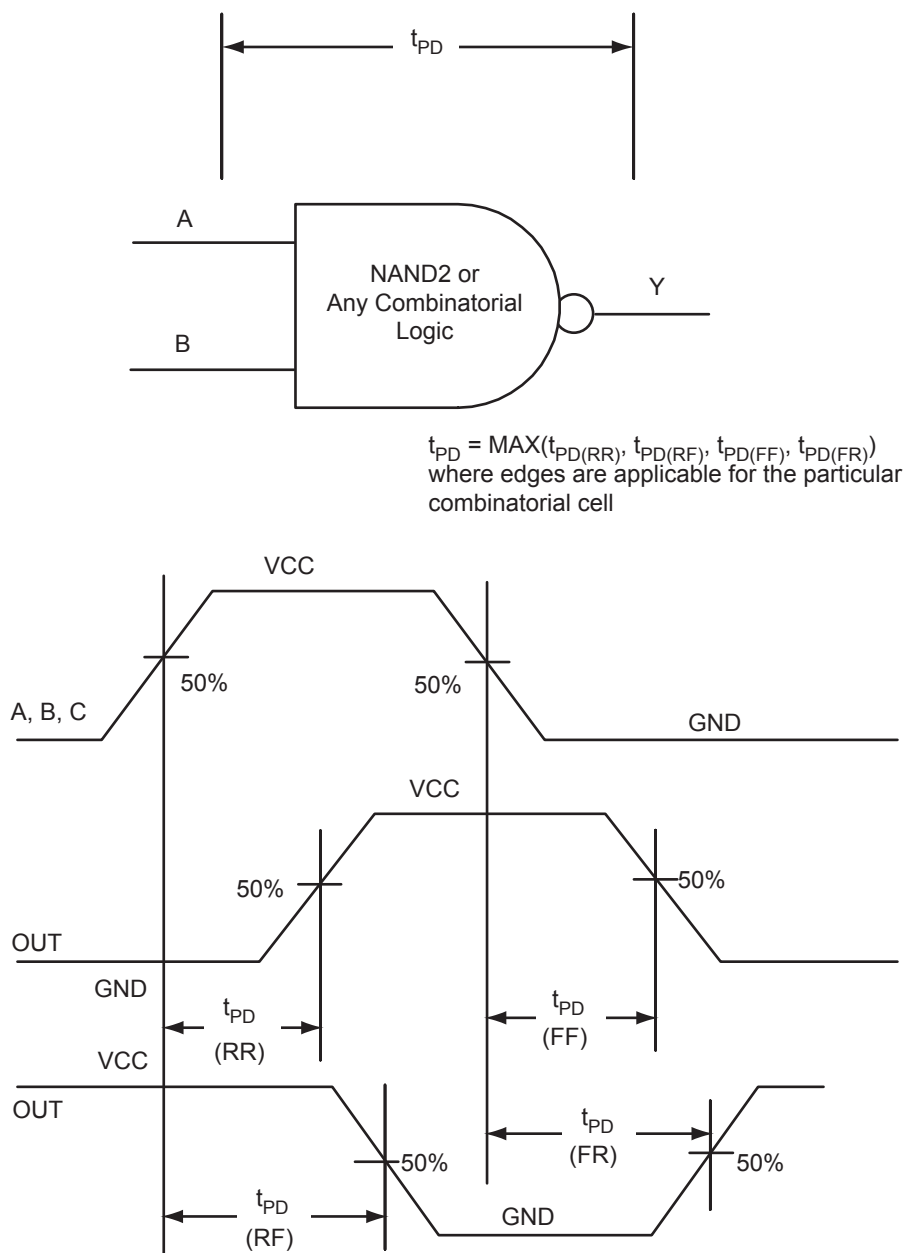


Figure 2-25 • Timing Model and Waveforms

Clock Conditioning Circuits

CCC Electrical Specifications

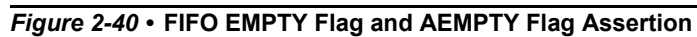
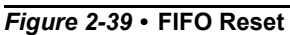
Timing Characteristics

Table 2-115 • ProASIC3 CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Serial Clock (SCLK) for Dynamic PLL ¹			125	MHz
Delay Increments in Programmable Delay Blocks ^{2, 3}		200 ⁴		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
(A3P250 and A3P1000 only) LockControl = 0			300	μs
LockControl = 1			300	μs
(all other dies) LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁵				
(A3P250 and A3P1000 only) LockControl = 0			1.6	ns
LockControl = 1			1.6	ns
(all other dies) LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay ^{1, 3}	0.6		5.56	ns
Delay Range in Block: Programmable Delay ^{2, 3}	0.225		5.56	ns
Delay Range in Block: Fixed Delay ^{2, 3}		2.2		ns

Notes:

1. Maximum value obtained for a –2 speed-grade device in worst-case commercial conditions. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
2. This delay is a function of voltage and temperature. See [Table 2-6 on page 2-6](#) for deratings.
3. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
4. When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to the Libero SoC Online Help for more information.
5. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.
6. The A3P030 device does not contain a PLL.



In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 k Ω will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

User's Guides

ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

<http://www.microsemi.com/soc/documents/PckgMechDrwns.pdf>

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are at <http://www.microsemi.com/products/solutions/package/docs.aspx>.

QN132	
Pin Number	A3P250 Function
C17	IO74RSB2
C18	VCCIB2
C19	TCK
C20	VMV2
C21	VPUMP
C22	VJTAG
C23	VCCIB1
C24	IO53NSB1
C25	IO51NPB1
C26	GCA1/IO50PPB1
C27	GCC0/IO48NDB1
C28	VCCIB1
C29	IO42NDB1
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TQ144	
Pin Number	A3P060 Function
1	GAA2/IO51RSB1
2	IO52RSB1
3	GAB2/IO53RSB1
4	IO95RSB1
5	GAC2/IO94RSB1
6	IO93RSB1
7	IO92RSB1
8	IO91RSB1
9	VCC
10	GND
11	VCCIB1
12	IO90RSB1
13	GFC1/IO89RSB1
14	GFC0/IO88RSB1
15	GFB1/IO87RSB1
16	GFB0/IO86RSB1
17	VCOMPLF
18	GFA0/IO85RSB1
19	VCCPLF
20	GFA1/IO84RSB1
21	GFA2/IO83RSB1
22	GFB2/IO82RSB1
23	GFC2/IO81RSB1
24	IO80RSB1
25	IO79RSB1
26	IO78RSB1
27	GND
28	VCCIB1
29	GEC1/IO77RSB1
30	GEC0/IO76RSB1
31	GEB1/IO75RSB1
32	GEB0/IO74RSB1
33	GEA1/IO73RSB1
34	GEA0/IO72RSB1
35	VMV1
36	GNDQ

TQ144	
Pin Number	A3P060 Function
37	NC
38	GEA2/IO71RSB1
39	GEB2/IO70RSB1
40	GEC2/IO69RSB1
41	IO68RSB1
42	IO67RSB1
43	IO66RSB1
44	IO65RSB1
45	VCC
46	GND
47	VCCIB1
48	NC
49	IO64RSB1
50	NC
51	IO63RSB1
52	NC
53	IO62RSB1
54	NC
55	IO61RSB1
56	NC
57	NC
58	IO60RSB1
59	IO59RSB1
60	IO58RSB1
61	IO57RSB1
62	NC
63	GND
64	NC
65	GDC2/IO56RSB1
66	GDB2/IO55RSB1
67	GDA2/IO54RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1

TQ144	
Pin Number	A3P060 Function
73	VPUMP
74	NC
75	TDO
76	TRST
77	VJTAG
78	GDA0/IO50RSB0
79	GDB0/IO48RSB0
80	GDB1/IO47RSB0
81	VCCIB0
82	GND
83	IO44RSB0
84	GCC2/IO43RSB0
85	GCB2/IO42RSB0
86	GCA2/IO41RSB0
87	GCA0/IO40RSB0
88	GCA1/IO39RSB0
89	GCB0/IO38RSB0
90	GCB1/IO37RSB0
91	GCC0/IO36RSB0
92	GCC1/IO35RSB0
93	IO34RSB0
94	IO33RSB0
95	NC
96	NC
97	NC
98	VCCIB0
99	GND
100	VCC
101	IO30RSB0
102	GBC2/IO29RSB0
103	IO28RSB0
104	GBB2/IO27RSB0
105	IO26RSB0
106	GBA2/IO25RSB0
107	VMV0
108	GNDQ

PQ208	
Pin Number	A3P1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC

PQ208	
Pin Number	A3P1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

FG144	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	A3P125 Function
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	GEB2/IO105RSB1
L4	IO102RSB1
L5	VCCIB1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG144	
Pin Number	A3P400 Function
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO30RSB0
A8	VCC
A9	IO34RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO154UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO23RSB0
B8	IO31RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO154VDB3
C2	GFA2/IO144PPB3
C3	GAC2/IO153UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO25RSB0
C8	IO32RSB0
C9	IO53RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

FG144	
Pin Number	A3P400 Function
D1	IO149NDB3
D2	IO149PDB3
D3	IO153VDB3
D4	GAA2/IO155UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO68PPB1
E1	VCC
E2	GFC0/IO147NDB3
E3	GFC1/IO147PDB3
E4	VCCIB3
E5	IO155VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO67PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO69NDB1
E12	IO70NDB1
F1	GFB0/IO146NPB3
F2	VCOMPLF
F3	GFB1/IO146PPB3
F4	IO144NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO67NDB1
F9	GCB0/IO68NPB1
F10	GND
F11	GCA1/IO69PDB1
F12	GCA2/IO70PDB1

FG144	
Pin Number	A3P400 Function
G1	GFA1/IO145PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO145NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO77UPB1
G9	IO72NDB1
G10	GCC2/IO72PDB1
G11	IO71NDB1
G12	GCB2/IO71PDB1
H1	VCC
H2	GFB2/IO143PDB3
H3	GFC2/IO142PSB3
H4	GEC1/IO137PDB3
H5	VCC
H6	IO75PDB1
H7	IO75NDB1
H8	GDB2/IO81RSB2
H9	GDC0/IO77VPB1
H10	VCCIB1
H11	IO73PSB1
H12	VCC
J1	GEB1/IO136PDB3
J2	IO143NDB3
J3	VCCIB3
J4	GEC0/IO137NDB3
J5	IO125RSB2
J6	IO116RSB2
J7	VCC
J8	TCK
J9	GDA2/IO80RSB2
J10	TDO
J11	GDA1/IO79UDB1
J12	GDB1/IO78UDB1

FG484	
Pin Number	A3P400 Function
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO15RSB0
A7	IO18RSB0
A8	NC
A9	NC
A10	IO23RSB0
A11	IO29RSB0
A12	IO35RSB0
A13	IO36RSB0
A14	NC
A15	NC
A16	IO50RSB0
A17	IO51RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	NC
B7	NC
B8	NC
B9	NC
B10	NC
B11	NC
B12	NC
B13	NC
B14	NC

FG484	
Pin Number	A3P400 Function
B15	NC
B16	NC
B17	NC
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

FG484	
Pin Number	A3P400 Function
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO17RSB0
D10	IO22RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO154UDB3
E5	GAA2/IO155UDB3
E6	IO12RSB0
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO44RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the ProASIC3 datasheet.

Revision	Changes	Page
Revision 18 (March 2016)	Updated 3.3 V DC supply voltage's maximum Commercial and Industrial values from 3.3 V to 3.6 V in Table 2-2 (SAR 72693).	2-2
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833).	NA
Revision 17 (June 2015)	Removed PQFP embedded heat spreader info. from Table 2-5 (SAR 52320).	2-6
	Updated " VCCIBx I/O Supply Voltage " (SAR 43323).	3-1
Revision 16 (December 2014)	Updated " ProASIC3 Ordering Information ". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079). Added Note "Only devices with package size greater than or equal to 5x5 are supported".	1-IV
	Updated Table Note (2) in Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature so that the Table Note is not applicable for Maximum Storage Temperature T _{STG} (SAR 54297).	2-3
	Added values for Drive strength 2 mA in Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew , Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew , Table 2-43 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew , and Table 2-44 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew (SAR 57184).	2-34, 2-35, 2-36, 2-37
	Added Figure 2-1 • High-Temperature Data Retention (HTR) (SAR 45466).	2-3
	Updates made to maintain the style and consistency of the document.	NA
Revision 15 (July 2014)	Added corner pad table note (3) to " QN132 – Bottom View " (SAR 47442).	4-6
	Ambient temperature removed in Table 2-2 , table notes and " ProASIC3 Ordering Information " figure were modified (SAR 48343).	2-2 1-IV
	Other updates were made to maintain the style and consistency of the datasheet.	NA
Revision 14 (April 2014)	Note added for the discontinuance of QN132 package to the following tables and section: " ProASIC3 Devices ", " I/Os Per Package 1 ", " ProASIC3 FPGAs Package Sizes Dimensions " and " QN132 – Bottom View " section (SAR 55118).	I, III, 4-6