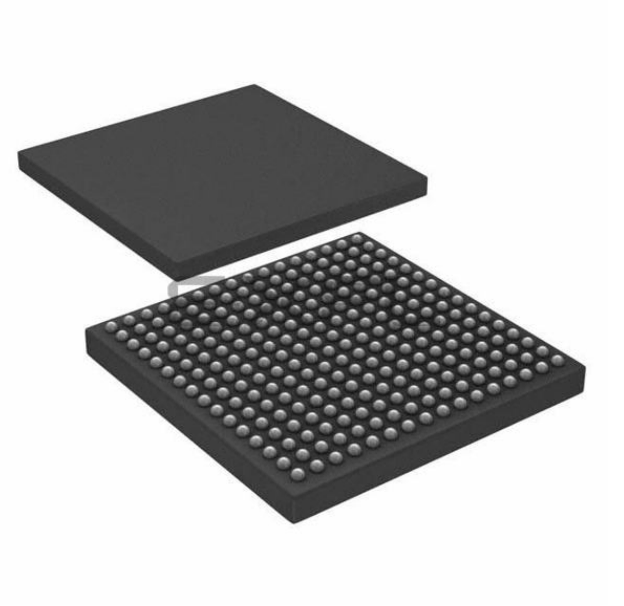

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-1fg256

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1 – ProASIC3 Device Family Overview

General Description

ProASIC3, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC$^{\text{PLUS}}$® family. Nonvolatile flash technology gives ProASIC3 devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P015 and A3P030 devices have no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

ProASIC3 devices support the ARM Cortex-M1 processor. The ARM-enabled devices have Microsemi ordering numbers that begin with M1A3P (Cortex-M1) and do not support AES decryption.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3 devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

ARM-enabled ProASIC3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks.

Table 2-2 • **Recommended Operating Conditions [1]**

Symbol	Parameters [1]		Commercial	Industrial	Units
T_J	Junction temperature		0 to 85[2]	-40 to 100[2]	°C
VCC[3]	1.5 V DC core supply voltage		1.425 to 1.575	1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.4 to 3.6	1.4 to 3.6	V
VPUMP	Programming voltage	Programming Mode	3.15 to 3.45	3.15 to 3.45	V
		Operation [4]	0 to 3.6	0 to 3.6	V
VCCPLL	Analog power supply (PLL)		1.425 to 1.575	1.425 to 1.575	V
VCCI and VMV [5]	1.5 V DC supply voltage		1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	3.0 to 3.6	V
	3.3 V wide range DC supply voltage [6]		2.7 to 3.6	2.7 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O		2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	3.0 to 3.6	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *Software Default Junction Temperature Range in the Libero® System-on-Chip (SoC) software is set to 0°C to +70°C for commercial, and -40°C to +85°C for industrial. To ensure targeted reliability standards are met across the full range of junction temperatures, Microsemi recommends using custom settings for temperature range before running timing and power analysis tools. For more information regarding custom settings, refer to the New Project Dialog Box in the Libero SoC Online Help.*
3. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-18 on page 2-19.*
4. *VPUMP can be left floating during operation (not programming mode).*
5. *VMV and VCCI should be at the same voltage within a given I/O bank. VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
6. *3.3 V wide range is compliant to the JESD8-B specification and supports 3.0 V VCCI operation.*

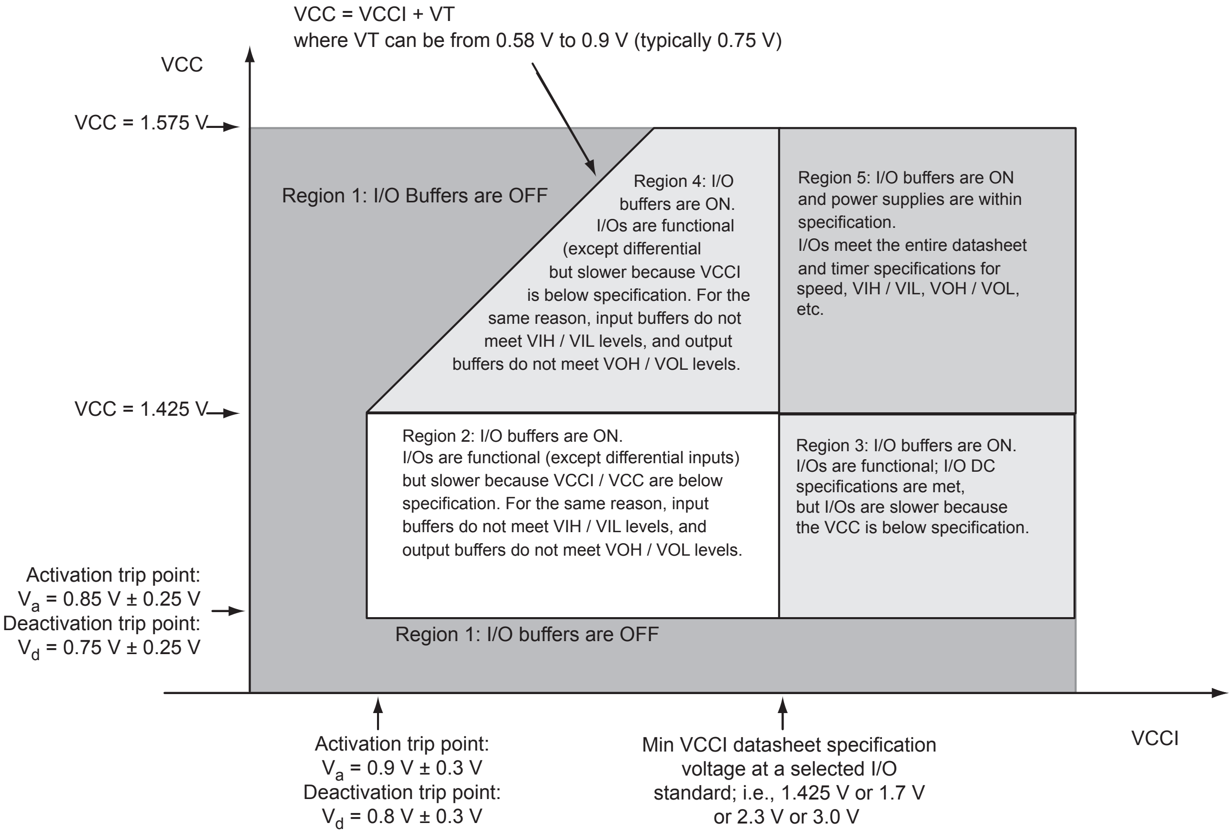

Figure 2-2 • **I/O State as a Function of VCCI and VCC Voltage Levels**

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja}. The thermal characteristics for θ_{ja} are shown for two air flow rates.

Table 2-30 • I/O Output Buffer Maximum Resistances[1]
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range[4]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL-DOWN-MAX)} = (VOLspec) / IOLspec$
3. $R_{(PULL-UP-MAX)} = (VCCImax – VOHspec) / IOHspec$
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK PULL-UP)}$[1] (Ω)		$R_{(WEAK PULL-DOWN)}$[2] (Ω)	
VCCI	Min	Max	Min	Max
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (VCCI_{MAX} – VOH_{spec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-DOWN-MAX)} = (VOL_{spec}) / I_{(WEAK PULL-DOWN-MIN)}$

***Table 2-33* • I/O Short Currents IOSH/IOSL**
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range[2]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

**Table 2-34 • I/O Short Currents IOSH/IOSL
Applicable to Standard I/O Banks**

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range[2]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Table 2-49 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

3.3 V LVCMOS Wide Range	Equiv. Software Default Drive Strength Option[1]	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[2]	IIH[3]
Drive Strength		**Min V**	**Max V**	**Min V**	**Max V**	**Max V**	**Min V**	**µA**	**µA**	**Max mA[4]**	**Max mA[4]**	**µA[5]**	**µA[5]**
100 µA	2 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	4 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	25	27	10	10
100 µA	6 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10
100 µA	8 mA	–0.3	0.8	2	3.6	0.2	VDD – 0.2	100	100	51	54	10	10

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
4. *Currents are measured at 85°C junction temperature.*
5. *All LVMCOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*
6. *Software default selection highlighted in gray.*

Table 2-71 • **1.8 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	–1	0.56	13.21	0.04	1.04	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	–2	0.49	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.22	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	–1	0.56	8.91	0.04	1.04	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	–2	0.49	7.82	0.03	0.91	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
6 mA	Std.	0.66	8.05	0.04	1.22	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	–1	0.56	6.85	0.04	1.04	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	–2	0.49	6.01	0.03	0.91	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
8 mA	Std.	0.66	7.50	0.04	1.22	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	–1	0.56	6.38	0.04	1.04	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	–2	0.49	5.60	0.03	0.91	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
12 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	–1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	–2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-77 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	2	2	16	13	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.575	0.25 * VCCI	0.75 * VCCI	4	4	33	25	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-78 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks**

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max. V**	**Min. V**	**mA**	**mA**	**Max. mA[3]**	**Max. mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.25 * VCCI	0.75 * VCCI	2	2	13	16	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

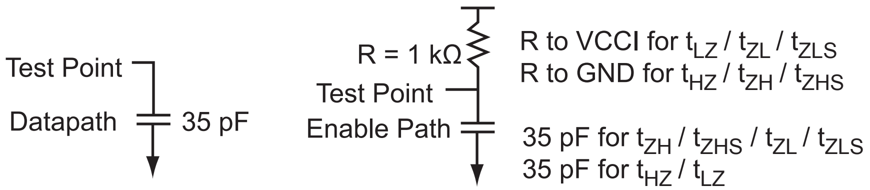

Figure 2-10 • **AC Loading**

Table 2-79 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

Note: **Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Output Enable Register

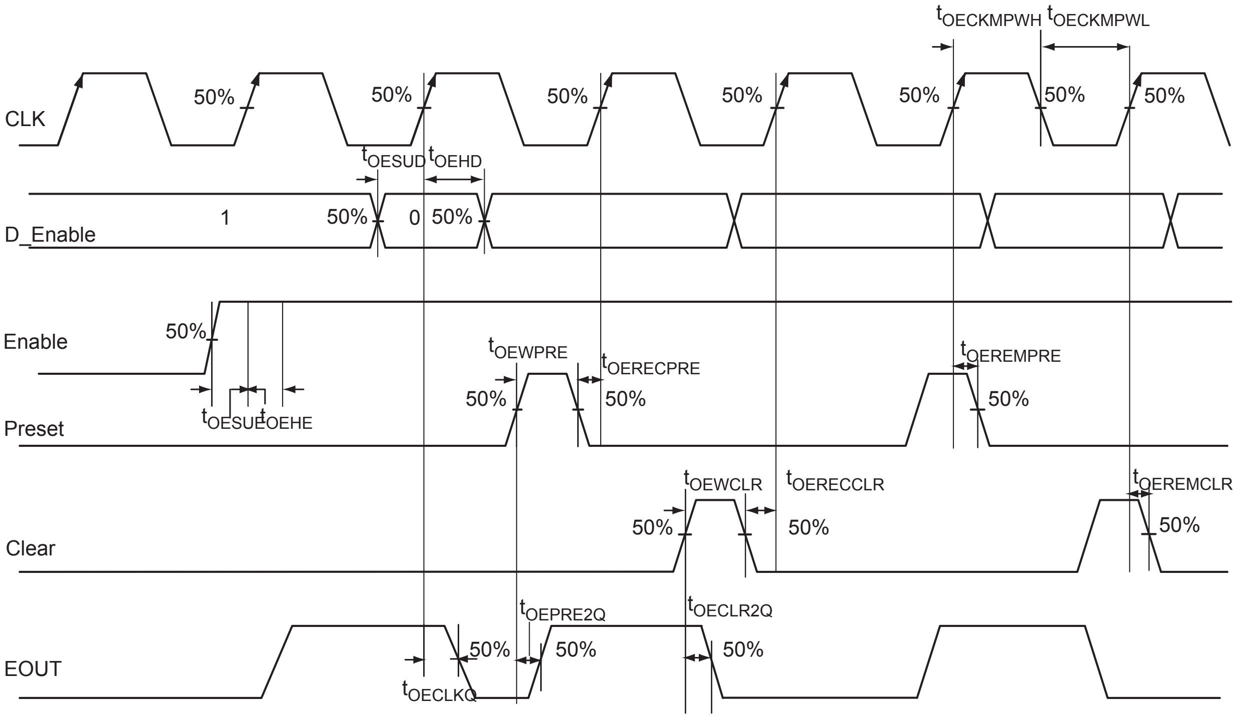

Figure 2-19 • **Output Enable Register Timing Diagram**

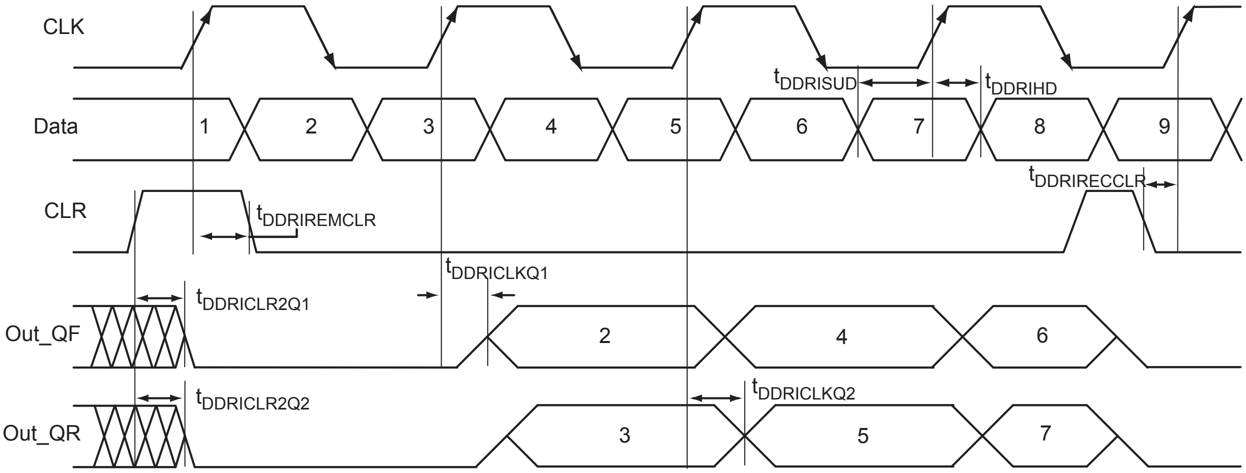

Figure 2-21 **• Input DDR Timing Diagram**

Timing Characteristics

Table 2-102 **• Input DDR Propagation Delays**
Commercial-Case Conditions: T_J = 70°C, Worst Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.27	0.31	0.37	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.39	0.44	0.52	ns
$t_{DDRISUD}$	Data Setup for Input DDR (Fall)	0.25	0.28	0.33	ns
	Data Setup for Input DDR (Rise)	0.25	0.28	0.33	ns
t_{DDRIHD}	Data Hold for Input DDR (Fall)	0.00	0.00	0.00	ns
	Data Hold for Input DDR (Rise)	0.00	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.46	0.53	0.62	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.57	0.65	0.76	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.22	0.25	0.30	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.25	0.30	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.41	0.48	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.37	0.43	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	309	263	MHz

Note: For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.

Output DDR Module

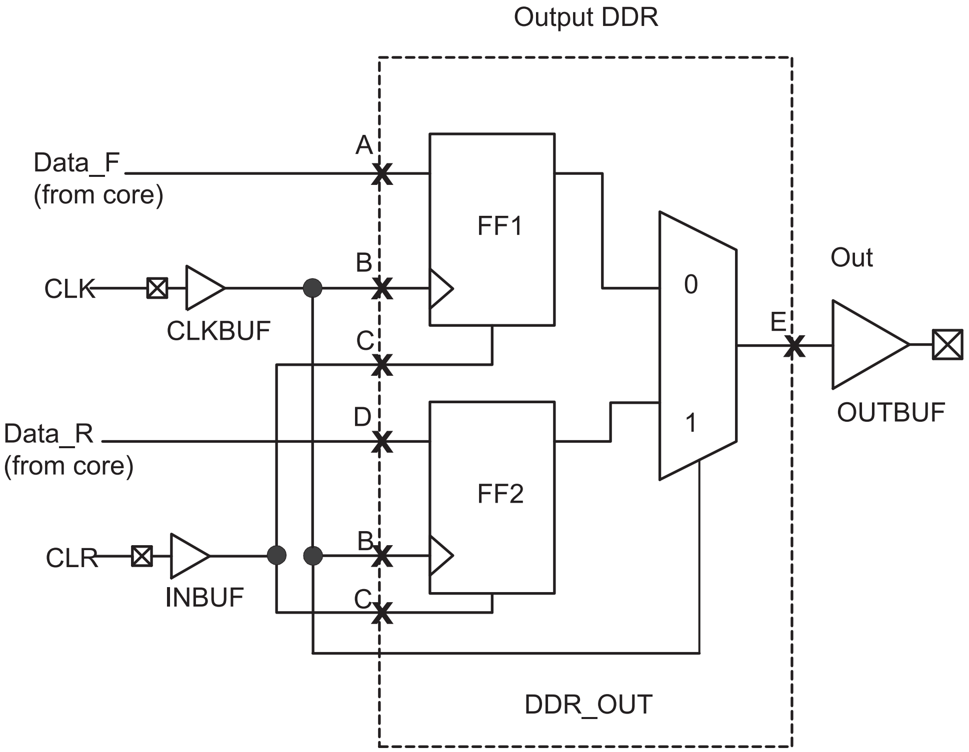

Figure 2-22 • **Output DDR Timing Model**

***Table 2-103* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide*.

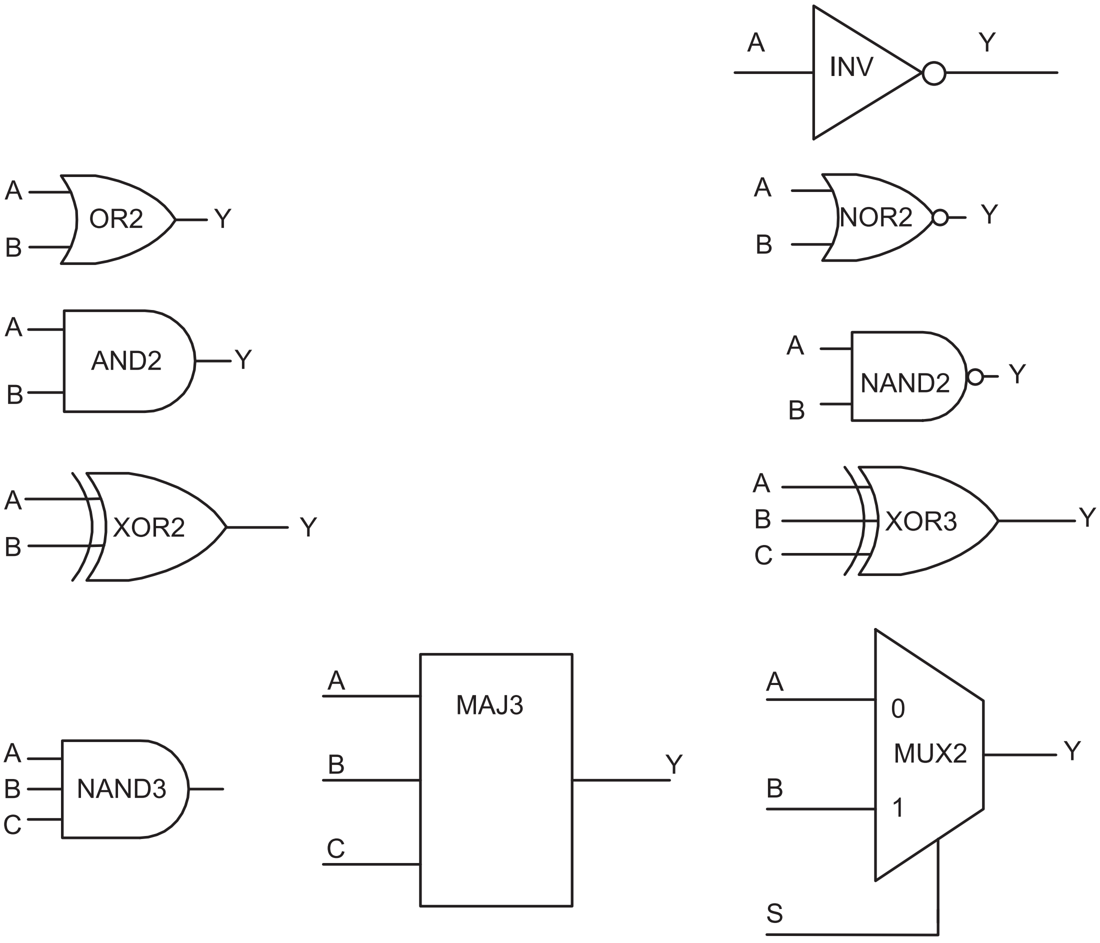

Figure 2-24 • **Sample of Combinatorial Cells**

Timing Characteristics

Table 2-105 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

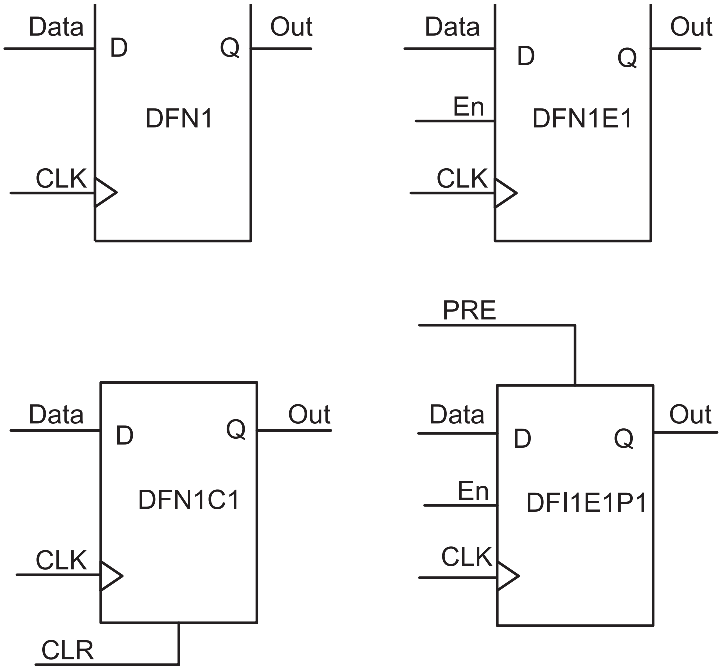

Figure 2-26 • Sample of Sequential Cells

PQ208	
Pin Number	**A3P125 Function**
109	TRST
110	VJTAG
111	GDA0/IO66RSB0
112	GDA1/IO65RSB0
113	GDB0/IO64RSB0
114	GDB1/IO63RSB0
115	GDC0/IO62RSB0
116	GDC1/IO61RSB0
117	NC
118	NC
119	NC
120	NC
121	NC
122	GND
123	VCCIB0
124	NC
125	NC
126	VCC
127	IO60RSB0
128	GCC2/IO59RSB0
129	GCB2/IO58RSB0
130	GND
131	GCA2/IO57RSB0
132	GCA0/IO56RSB0
133	GCA1/IO55RSB0
134	GCB0/IO54RSB0
135	GCB1/IO53RSB0
136	GCC0/IO52RSB0
137	GCC1/IO51RSB0
138	IO50RSB0
139	IO49RSB0
140	VCCIB0
141	GND
142	VCC
143	IO48RSB0
144	IO47RSB0

PQ208	
Pin Number	**A3P125 Function**
145	IO46RSB0
146	NC
147	NC
148	NC
149	GBC2/IO45RSB0
150	IO44RSB0
151	GBB2/IO43RSB0
152	IO42RSB0
153	GBA2/IO41RSB0
154	VMV0
155	GNDQ
156	GND
157	NC
158	GBA1/IO40RSB0
159	GBA0/IO39RSB0
160	GBB1/IO38RSB0
161	GBB0/IO37RSB0
162	GND
163	GBC1/IO36RSB0
164	GBC0/IO35RSB0
165	IO34RSB0
166	IO33RSB0
167	IO32RSB0
168	IO31RSB0
169	IO30RSB0
170	VCCIB0
171	VCC
172	IO29RSB0
173	IO28RSB0
174	IO27RSB0
175	IO26RSB0
176	IO25RSB0
177	IO24RSB0
178	GND
179	IO23RSB0
180	IO22RSB0

PQ208	
Pin Number	**A3P125 Function**
181	IO21RSB0
182	IO20RSB0
183	IO19RSB0
184	IO18RSB0
185	IO17RSB0
186	VCCIB0
187	VCC
188	IO16RSB0
189	IO15RSB0
190	IO14RSB0
191	IO13RSB0
192	IO12RSB0
193	IO11RSB0
194	IO10RSB0
195	GND
196	IO09RSB0
197	IO08RSB0
198	IO07RSB0
199	IO06RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

PQ208	
Pin Number	**A3P1000 Function**
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

PQ208	
Pin Number	**A3P1000 Function**
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

Revision	**Changes**	**Page**
Advance v0.3	The "PLL Macro" section was updated. EXTFB information was removed from this section.	2-15
	The CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} was updated in Table 2-11 • ProASIC3 CCC/PLL Specification	2-29
	EXTFB was removed from Figure 2-27 • CCC/PLL Macro.	2-28
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Hot-Swap Support" section was updated.	2-33
	The "Cold-Sparing Support" section was updated.	2-34
	"Electrostatic Discharge (ESD) Protection" section was updated.	2-35
	The LVPECL specification in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	In the Bank 1 area of Figure 2-72, VMV2 was changed to VMV1 and VCCIB2 was changed to VCC$_I$B1.	2-97
	The VJTAG and I/O pin descriptions were updated in the "Pin Descriptions" section.	2-50
	The "JTAG Pins" section was updated.	2-51
	"128-Bit AES Decryption" section was updated to include M7 device information.	2-53
	Table 3-6 was updated.	3-6
	Table 3-7 was updated.	3-6
	In Table 3-11, PAC4 was updated.	3-93-8
	Table 3-20 was updated.	3-20
	The note in Table 3-32 was updated.	3-27
	All Timing Characteristics tables were updated from LVTTL to Register Delays	3-31 to 3-73
	The Timing Characteristics for RAM4K9, RAM512X18, and FIFO were updated.	3-85 to 3-90
	F_{TCKMAX} was updated in Table 3-110.	3-97
Advance v0.2	Figure 2-11 was updated.	2-9
	The "Clock Resources (VersaNets)" section was updated.	2-9
	The "VersaNet Global Networks and Spine Access" section was updated.	2-9
	The "PLL Macro" section was updated.	2-15
	Figure 2-27 was updated.	2-28
	Figure 2-20 was updated.	2-19
	Table 2-5 was updated.	2-25
	Table 2-6 was updated.	2-25
	The "FIFO Flag Usage Considerations" section was updated.	2-27
	Table 2-13 was updated.	2-30
	Figure 2-24 was updated.	2-31
	The "Cold-Sparing Support" section is new.	2-34

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "ProASIC3 Device Status" table on page IV, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

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The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

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