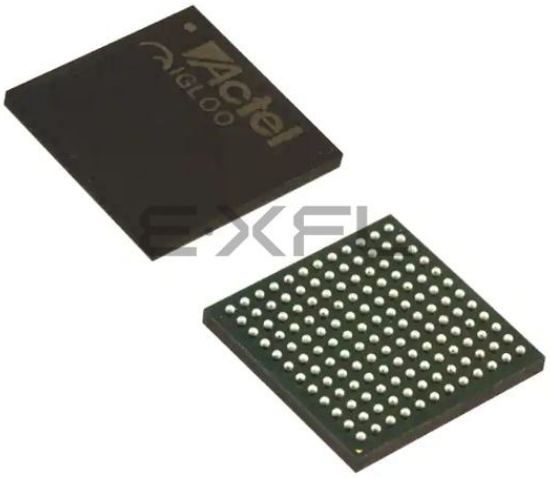

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

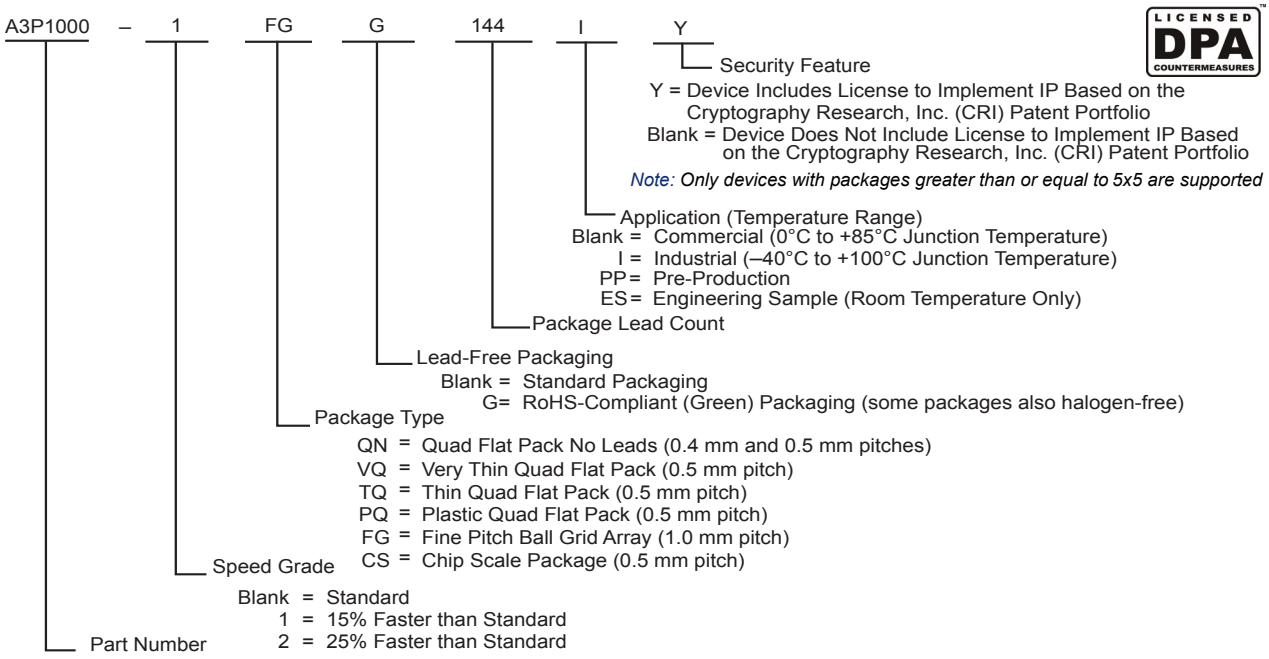
Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	97
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	144-LBGA
Supplier Device Package	144-FPBGA (13x13)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-1fgg144

ProASIC3 Ordering Information



ProASIC3 Devices

A3P015 = 15,000 System Gates (A3P015 is not recommended for new designs.)
A3P030 = 30,000 System Gates
A3P060 = 60,000 System Gates
A3P125 = 125,000 System Gates
A3P250 = 250,000 System Gates
A3P400 = 400,000 System Gates
A3P600 = 600,000 System Gates
A3P1000 = 1,000,000 System Gates

ProASIC3 Devices with Cortex-M1

M1A3P250 = 250,000 System Gates
M1A3P400 = 400,000 System Gates
M1A3P600 = 600,000 System Gates
M1A3P1000 = 1,000,000 System Gates

ProASIC3 Device Status

ProASIC3 Devices	Status	Cortex-M1 Devices	Status
A3P015	Not recommended for new designs.		
A3P030	Production		
A3P060	Production		
A3P125	Production		
A3P250	Production	M1A3P250	Production
A3P400	Production	M1A3P400	Production
A3P600	Production	M1A3P600	Production
A3P1000	Production	M1A3P1000	Production

Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3 device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based ProASIC3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings –2 Speed Grade, Commercial-Case Conditions: T_J = 70°C, Worst Case VCC = 1.425 V, Worst-Case VCCI (per standard) Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[1]	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
3.3 V LVCMOS Wide Range[2]	100 µA	12 mA	High	35	–	0.45	4.08	0.03	0.76	0.32	4.08	3.20	3.71	4.14	6.61	5.74	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	–	High	10	25 [4]	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 [4]	0.45	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	–	High	–	–	0.45	1.37	0.03	1.20	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.45	1.34	0.03	1.05	–	–	–	–	–	–	–	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*
4. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-64 for connectivity. This resistor is not required during normal operation.*

Table 2-29 • I/O Output Buffer Maximum Resistances [1]
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range[4]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *$R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-34 • I/O Short Currents IOSH/IOSL Applicable to Standard I/O Banks

	Drive Strength	IOSL (mA)[1]	IOSH (mA)[1]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
3.3 V LVCMOS Wide Range[2]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

Notes:

1. *T_J = 100°C*
2. *Applicable to 3.3 V LVCMOS Wide Range. I_{OSL}/I_{OSH} dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

The length of time an I/O can withstand IOSH/IOSL events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than six months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-35 • Duration of Short Circuit Event Before Failure

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	0.5 years

Table 2-36 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min)	Input Rise/Fall Time (max)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Table 2-58 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max., V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	3.6	0.7	1.7	2	2	16	18	10	10
4 mA	–0.3	0.7	1.7	3.6	0.7	1.7	4	4	16	18	10	10
6 mA	–0.3	0.7	1.7	3.6	0.7	1.7	6	6	32	37	10	10
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	32	37	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

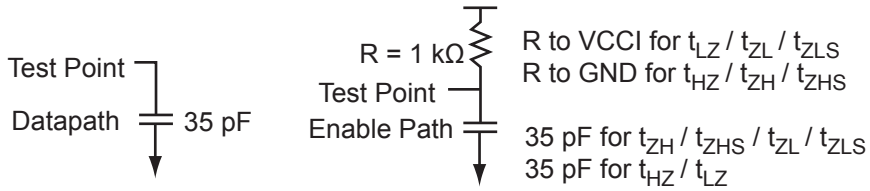


Figure 2-8 • AC Loading

Table 2-59 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.*

Table 2-62 • 2.5 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	–1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	–2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	–1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	–2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-63 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	–2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	–1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	–2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

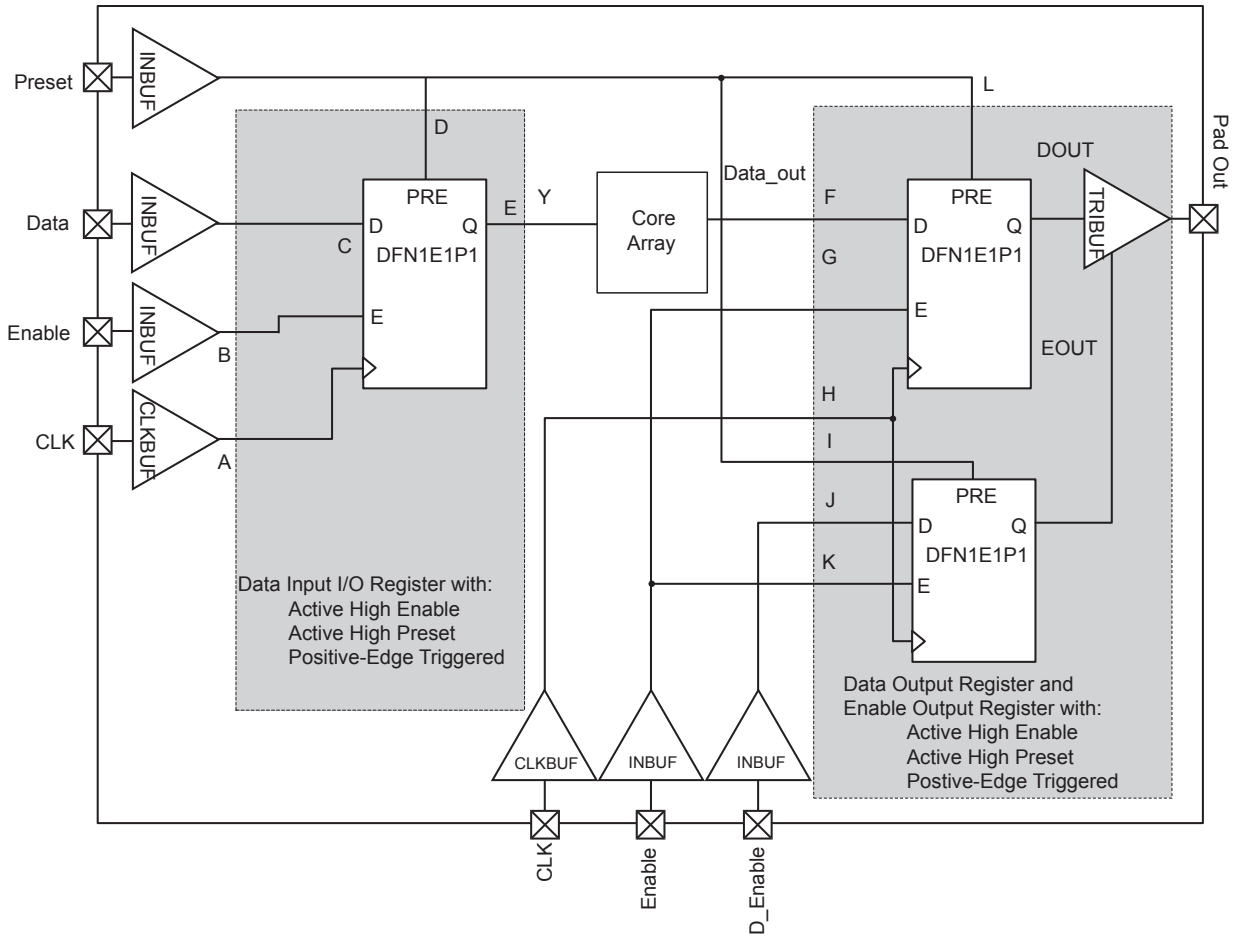


Figure 2-15 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

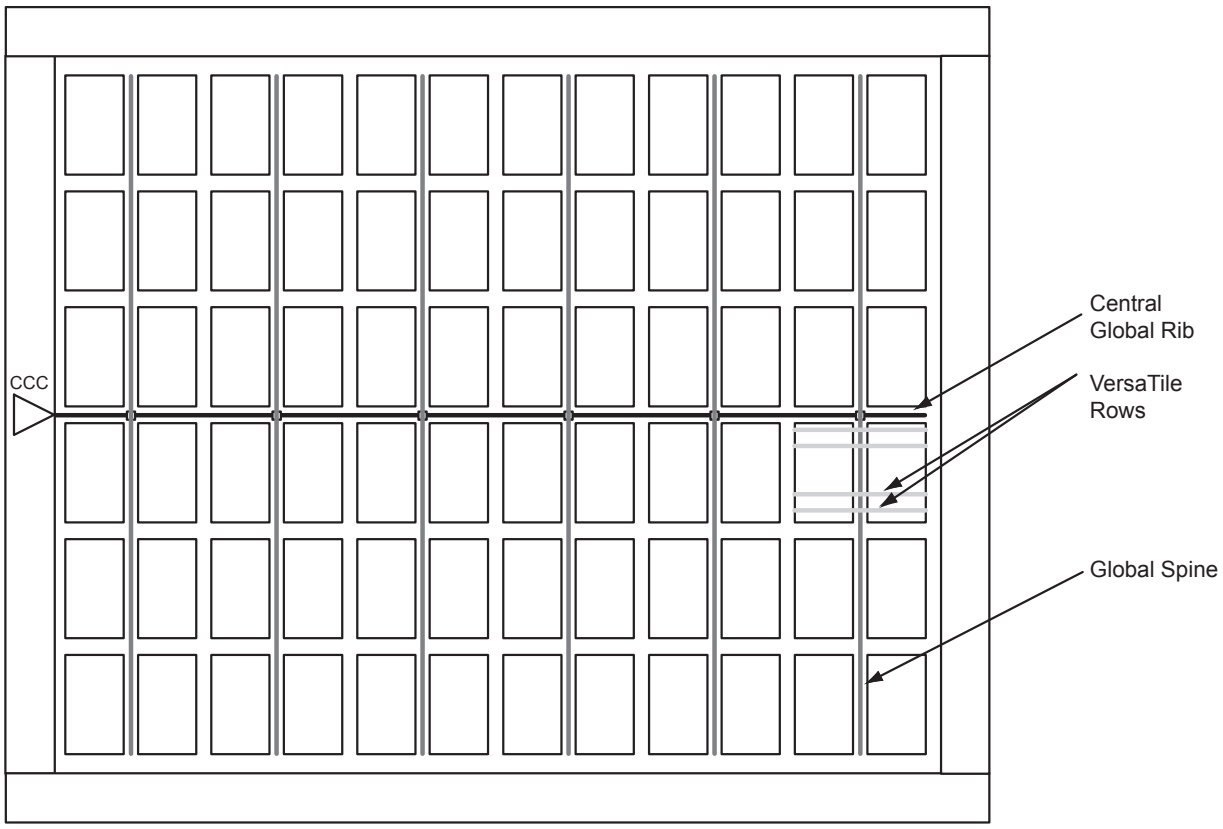


Figure 2-28 • **Example of Global Tree Use in an A3P250 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-90. Table 2-108 to Table 2-114 on page 2-89 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

***Table 2-107* • A3P015 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.66	0.81	0.75	0.92	0.88	1.08	ns
t_{RCKH}	Input High Delay for Global Clock	0.67	0.84	0.76	0.96	0.89	1.13	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.25	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-108* • A3P030 Global Resource**
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.67	0.81	0.76	0.92	0.89	1.09	ns
t_{RCKH}	Input High Delay for Global Clock	0.68	0.85	0.77	0.97	0.91	1.14	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.24	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

***Table 2-119* • FIFO (for A3P250 only, aspect-ratio-dependent)**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.26	3.71	4.36	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

QN48	
Pin Number	**A3P030 Function**
1	IO82RSB1
2	GEC0/IO73RSB1
3	GEA0/IO72RSB1
4	GEB0/IO71RSB1
5	GND
6	VCCIB1
7	IO68RSB1
8	IO67RSB1
9	IO66RSB1
10	IO65RSB1
11	IO64RSB1
12	IO62RSB1
13	IO61RSB1
14	IO60RSB1
15	IO57RSB1
16	IO55RSB1
17	IO53RSB1
18	VCC
19	VCCIB1
20	IO46RSB1
21	IO42RSB1
22	TCK
23	TDI
24	TMS
25	VPUMP
26	TDO
27	TRST
28	VJTAG
29	IO38RSB0
30	GDB0/IO34RSB0
31	GDA0/IO33RSB0
32	GDC0/IO32RSB0
33	VCCIB0
34	GND
35	VCC
36	IO25RSB0

QN48	
Pin Number	**A3P030 Function**
37	IO24RSB0
38	IO22RSB0
39	IO20RSB0
40	IO18RSB0
41	IO16RSB0
42	IO14RSB0
43	IO10RSB0
44	IO08RSB0
45	IO06RSB0
46	IO04RSB0
47	IO02RSB0
48	IO00RSB0

VQ100	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

VQ100	
Pin Number	A3P125 Function
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

VQ100	
Pin Number	A3P125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

FG256	
Pin Number	A3P400 Function
G13	GCC1/IO67PPB1
G14	IO64NPB1
G15	IO73PDB1
G16	IO73NDB1
H1	GFB0/IO146NPB3
H2	GFA0/IO145NDB3
H3	GFB1/IO146PPB3
H4	VCOMPLF
H5	GFC0/IO147NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO67NPB1
H13	GCB1/IO68PPB1
H14	GCA0/IO69NPB1
H15	NC
H16	GCB0/IO68NPB1
J1	GFA2/IO144PPB3
J2	GFA1/IO145PDB3
J3	VCCPLF
J4	IO143NDB3
J5	GFB2/IO143PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO71PPB1
J13	GCA1/IO69PPB1
J14	GCC2/IO72PPB1
J15	NC
J16	GCA2/IO70PDB1

FG256	
Pin Number	A3P400 Function
K1	GFC2/IO142PDB3
K2	IO144NPB3
K3	IO141PPB3
K4	IO120RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO71NPB1
K14	IO74RSB1
K15	IO72NPB1
K16	IO70NDB1
L1	IO142NDB3
L2	IO141NPB3
L3	IO125RSB2
L4	IO139RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO78VPB1
L14	IO76VDB1
L15	IO76UDB1
L16	IO75PDB1
M1	IO140PDB3
M2	IO130RSB2
M3	IO138NPB3
M4	GEC0/IO137NPB3

FG256	
Pin Number	A3P400 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO108RSB2
M9	IO101RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO83RSB2
M14	GDB1/IO78UPB1
M15	GDC1/IO77UDB1
M16	IO75NDB1
N1	IO140NDB3
N2	IO138PPB3
N3	GEC1/IO137PPB3
N4	IO131RSB2
N5	GNDQ
N6	GEA2/IO134RSB2
N7	IO117RSB2
N8	IO111RSB2
N9	IO99RSB2
N10	IO94RSB2
N11	IO87RSB2
N12	GNDQ
N13	IO93RSB2
N14	VJTAG
N15	GDC0/IO77VDB1
N16	GDA1/IO79UDB1
P1	GEB1/IO136PDB3
P2	GEB0/IO136NDB3
P3	VMV2
P4	IO129RSB2
P5	IO128RSB2
P6	IO122RSB2
P7	IO115RSB2
P8	IO110RSB2

FG256	
Pin Number	**A3P400 Function**
P9	IO98RSB2
P10	IO95RSB2
P11	IO88RSB2
P12	IO84RSB2
P13	TCK
P14	VPUMP
P15	TRST
P16	GDA0/IO79VDB1
R1	GEA1/IO135PDB3
R2	GEA0/IO135NDB3
R3	IO127RSB2
R4	GEC2/IO132RSB2
R5	IO123RSB2
R6	IO118RSB2
R7	IO112RSB2
R8	IO106RSB2
R9	IO100RSB2
R10	IO96RSB2
R11	IO89RSB2
R12	IO85RSB2
R13	GDB2/IO81RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO126RSB2
T3	GEB2/IO133RSB2
T4	IO124RSB2
T5	IO116RSB2
T6	IO113RSB2
T7	IO107RSB2
T8	IO105RSB2
T9	IO102RSB2
T10	IO97RSB2
T11	IO92RSB2
T12	GDC2/IO82RSB2

FG256	
Pin Number	**A3P400 Function**
T13	IO86RSB2
T14	GDA2/IO80RSB2
T15	TMS
T16	GND

FG256	
Pin Number	A3P600 Function
G13	GCC1/IO69PPB1
G14	IO65NPB1
G15	IO75PDB1
G16	IO75NDB1
H1	GFB0/IO163NPB3
H2	GFA0/IO162NDB3
H3	GFB1/IO163PPB3
H4	VCOMPLF
H5	GFC0/IO164NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO69NPB1
H13	GCB1/IO70PPB1
H14	GCA0/IO71NPB1
H15	IO67NPB1
H16	GCB0/IO70NPB1
J1	GFA2/IO161PPB3
J2	GFA1/IO162PDB3
J3	VCCPLF
J4	IO160NDB3
J5	GFB2/IO160PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO73PPB1
J13	GCA1/IO71PPB1
J14	GCC2/IO74PPB1
J15	IO80PPB1
J16	GCA2/IO72PDB1

FG256	
Pin Number	A3P600 Function
K1	GFC2/IO159PDB3
K2	IO161NPB3
K3	IO156PPB3
K4	IO129RSB2
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO73NPB1
K14	IO80NPB1
K15	IO74NPB1
K16	IO72NDB1
L1	IO159NDB3
L2	IO156NPB3
L3	IO151PPB3
L4	IO158PSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO87NPB1
L14	IO85NDB1
L15	IO85PDB1
L16	IO84PDB1
M1	IO150PDB3
M2	IO151NPB3
M3	IO147NPB3
M4	GEC0/IO146NPB3

FG256	
Pin Number	A3P600 Function
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	IO117RSB2
M9	IO110RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	IO94RSB2
M14	GDB1/IO87PPB1
M15	GDC1/IO86PDB1
M16	IO84NDB1
N1	IO150NDB3
N2	IO147PPB3
N3	GEC1/IO146PPB3
N4	IO140RSB2
N5	GNDQ
N6	GEA2/IO143RSB2
N7	IO126RSB2
N8	IO120RSB2
N9	IO108RSB2
N10	IO103RSB2
N11	IO99RSB2
N12	GNDQ
N13	IO92RSB2
N14	VJTAG
N15	GDC0/IO86NDB1
N16	GDA1/IO88PDB1
P1	GEB1/IO145PDB3
P2	GEB0/IO145NDB3
P3	VMV2
P4	IO138RSB2
P5	IO136RSB2
P6	IO131RSB2
P7	IO124RSB2
P8	IO119RSB2

FG256	
Pin Number	**A3P1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0

FG256	
Pin Number	**A3P1000 Function**
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1

FG256	
Pin Number	**A3P1000 Function**
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG256	
Pin Number	**A3P1000 Function**
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

FG484	
Pin Number	A3P1000 Function
K19	IO88NDB1
K20	IO94NPB1
K21	IO98NDB1
K22	IO98PDB1
L1	NC
L2	IO200PDB3
L3	IO210NPB3
L4	GFB0/IO208NPB3
L5	GFA0/IO207NDB3
L6	GFB1/IO208PPB3
L7	VCOMPLF
L8	GFC0/IO209NPB3
L9	VCC
L10	GND
L11	GND
L12	GND
L13	GND
L14	VCC
L15	GCC0/IO91NPB1
L16	GCB1/IO92PPB1
L17	GCA0/IO93NPB1
L18	IO96NPB1
L19	GCB0/IO92NPB1
L20	IO97PDB1
L21	IO97NDB1
L22	IO99NPB1
M1	NC
M2	IO200NDB3
M3	IO206NDB3
M4	GFA2/IO206PDB3
M5	GFA1/IO207PDB3
M6	VCCPLF
M7	IO205NDB3
M8	GFB2/IO205PDB3
M9	VCC
M10	GND

FG484	
Pin Number	A3P1000 Function
M11	GND
M12	GND
M13	GND
M14	VCC
M15	GCB2/IO95PPB1
M16	GCA1/IO93PPB1
M17	GCC2/IO96PPB1
M18	IO100PPB1
M19	GCA2/IO94PPB1
M20	IO101PPB1
M21	IO99PPB1
M22	NC
N1	IO201NDB3
N2	IO201PDB3
N3	NC
N4	GFC2/IO204PDB3
N5	IO204NDB3
N6	IO203NDB3
N7	IO203PDB3
N8	VCCIB3
N9	VCC
N10	GND
N11	GND
N12	GND
N13	GND
N14	VCC
N15	VCCIB1
N16	IO95NPB1
N17	IO100NPB1
N18	IO102NDB1
N19	IO102PDB1
N20	NC
N21	IO101NPB1
N22	IO103PDB1
P1	NC
P2	IO199PDB3

FG484	
Pin Number	A3P1000 Function
P3	IO199NDB3
P4	IO202NDB3
P5	IO202PDB3
P6	IO196PPB3
P7	IO193PPB3
P8	VCCIB3
P9	GND
P10	VCC
P11	VCC
P12	VCC
P13	VCC
P14	GND
P15	VCCIB1
P16	GDB0/IO112NPB1
P17	IO106NDB1
P18	IO106PDB1
P19	IO107PDB1
P20	NC
P21	IO104PDB1
P22	IO103NDB1
R1	NC
R2	IO197PPB3
R3	VCC
R4	IO197NPB3
R5	IO196NPB3
R6	IO193NPB3
R7	GEC0/IO190NPB3
R8	VMV3
R9	VCCIB2
R10	VCCIB2
R11	IO147RSB2
R12	IO136RSB2
R13	VCCIB2
R14	VCCIB2
R15	VMV2
R16	IO110NDB1