



Welcome to [E-XFL.COM](#)

### **Understanding Embedded - FPGAs (Field Programmable Gate Array)**

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

### **Applications of Embedded - FPGAs**

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

#### **Details**

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	<a href="https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-1fgg484">https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-1fgg484</a>

$F_{CLK}$  is the global clock signal frequency.

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$P_{AC1}$ ,  $P_{AC2}$ ,  $P_{AC3}$ , and  $P_{AC4}$  are device-dependent.

### **Sequential Cells Contribution— $P_{S-CELL}$**

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

$F_{CLK}$  is the global clock signal frequency.

### **Combinatorial Cells Contribution— $P_{C-CELL}$**

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

$F_{CLK}$  is the global clock signal frequency.

### **Routing Net Contribution— $P_{NET}$**

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

$N_{S-CELL}$  is the number of VersaTiles used as sequential modules in the design.

$N_{C-CELL}$  is the number of VersaTiles used as combinatorial modules in the design.

$\alpha_1$  is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-16 on page 2-14](#).

$F_{CLK}$  is the global clock signal frequency.

### **I/O Input Buffer Contribution— $P_{INPUTS}$**

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

$N_{INPUTS}$  is the number of I/O input buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-14](#).

$F_{CLK}$  is the global clock signal frequency.

### **I/O Output Buffer Contribution— $P_{OUTPUTS}$**

$$P_{OUTPUTS} = N_{OUTPUTS} * \alpha_2 / 2 * \beta_1 * P_{AC10} * F_{CLK}$$

$N_{OUTPUTS}$  is the number of I/O output buffers used in the design.

$\alpha_2$  is the I/O buffer toggle rate—guidelines are provided in [Table 2-16 on page 2-14](#).

$\beta_1$  is the I/O buffer enable rate—guidelines are provided in [Table 2-17 on page 2-14](#).

$F_{CLK}$  is the global clock signal frequency.

**Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings**

–2 Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst Case VCC = 1.425 V,  
 Worst-Case VCCI (per standard)  
 Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor ( $\Omega$ )	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DN}$ (ns)	$t_{PY}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	$t_{ZLs}$ (ns)	$t_{ZHs}$ (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu\text{A}$	12 mA	High	35	–	0.45	4.08	0.03	0.76	0.32	4.08	3.20	3.71	4.14	6.61	5.74	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	–	High	10	25 <sup>4</sup>	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 <sup>4</sup>	0.45	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	–	High	–	–	0.45	1.37	0.03	1.20	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.45	1.34	0.03	1.05	–	–	–	–	–	–	–	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-64 for connectivity. This resistor is not required during normal operation.

**Table 2-26 • Summary of I/O Timing Characteristics—Software Default Settings**

–2 Speed Grade, Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst Case VCC = 1.425 V,  
 Worst-Case VCCI (per standard)  
 Standard I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Slew Rate	Capacitive Load (pF)	External Resistor	$t_{DOUT}$ (ns)	$t_{DP}$ (ns)	$t_{DIN}$ (ns)	$t_{PY}$ (ns)	$t_{EOUT}$ (ns)	$t_{ZL}$ (ns)	$t_{ZH}$ (ns)	$t_{LZ}$ (ns)	$t_{HZ}$ (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
3.3 V LVCMOS Wide Range <sup>2</sup>	100 $\mu$ A	8 mA	High	35	–	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns
2.5 V LVCMOS	8 mA	8 mA	High	35	–	0.45	3.56	0.03	0.96	0.32	3.40	3.56	1.78	1.91	ns
1.8 V LVCMOS	4 mA	4 mA	High	35	–	0.45	4.74	0.03	0.90	0.32	4.02	4.74	1.80	1.85	ns
1.5 V LVCMOS	2 mA	2 mA	High	35	–	0.45	5.71	0.03	1.06	0.32	4.71	5.71	1.83	1.83	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

**Table 2-29 • I/O Output Buffer Maximum Resistances<sup>1</sup>**  
**Applicable to Standard Plus I/O Banks**

Standard	Drive Strength	R <sub>PULL-DOWN</sub> (Ω) <sup>2</sup>	R <sub>PULL-UP</sub> (Ω) <sup>3</sup>
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
3.3 V LVCMOS Wide Range <sup>4</sup>	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

**Notes:**

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at <http://www.microsemi.com/soc/download/ibis/default.aspx>.
2.  $R_{(PULL-DOWN-MAX)} = (VOLspec) / IOspec$
3.  $R_{(PULL-UP-MAX)} = (VCCImax - VOHspec) / IOHspec$
4. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.

**Table 2-54 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case  $V_{CC} = 1.425 \text{ V}$ , Worst-Case  $V_{CCI} = 3.0 \text{ V}$   
 Applicable to Standard I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option <sup>1</sup>	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	Units
100 $\mu\text{A}$	2 mA	Std.	0.60	10.93	0.04	1.52	0.43	10.93	9.46	3.20	3.32	ns
		-1	0.51	9.29	0.04	1.29	0.36	9.29	8.04	2.72	2.82	ns
		-2	0.45	8.16	0.03	1.13	0.32	8.16	7.06	2.39	2.48	ns
100 $\mu\text{A}$	4 mA	Std.	0.60	10.93	0.04	1.52	0.43	10.93	9.46	3.20	3.32	ns
		-1	0.51	9.29	0.04	1.29	0.36	9.29	8.04	2.72	2.82	ns
		-2	0.45	8.16	0.03	1.13	0.32	8.16	7.06	2.39	2.48	ns
100 $\mu\text{A}$	6 mA	Std.	0.60	6.82	0.04	1.52	0.43	6.82	5.70	3.70	4.16	ns
		-1	0.51	5.80	0.04	1.29	0.36	5.80	4.85	3.15	3.54	ns
		-2	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns
100 $\mu\text{A}$	8 mA	Std.	0.60	6.82	0.04	1.52	0.43	6.82	5.70	3.70	4.16	ns
		-1	0.51	5.80	0.04	1.29	0.36	5.80	4.85	3.15	3.54	ns
		-2	0.45	5.09	0.03	1.13	0.32	5.09	4.25	2.77	3.11	ns

**Notes:**

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is  $\pm 100 \mu\text{A}$ . Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. Software default selection highlighted in gray.
3. For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## Timing Characteristics

**Table 2-70 • 1.8 V LVC MOS High Slew**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	-1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	-2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	-1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	-2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	-1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	-2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	-1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	-2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	-1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	-2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

**Notes:**

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-71 • 1.8 V LVC MOS Low Slew**

 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V  
 Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	$t_{DOUT}$	$t_{DP}$	$t_{DIN}$	$t_{PY}$	$t_{EOUT}$	$t_{ZL}$	$t_{ZH}$	$t_{LZ}$	$t_{HZ}$	$t_{ZLS}$	$t_{ZHS}$	Units
2 mA	Std.	0.66	15.53	0.04	1.22	0.43	14.11	15.53	2.78	1.60	16.35	17.77	ns
	-1	0.56	13.21	0.04	1.04	0.36	12.01	13.21	2.36	1.36	13.91	15.11	ns
	-2	0.49	11.60	0.03	0.91	0.32	10.54	11.60	2.07	1.19	12.21	13.27	ns
4 mA	Std.	0.66	10.48	0.04	1.22	0.43	10.41	10.48	3.23	2.73	12.65	12.71	ns
	-1	0.56	8.91	0.04	1.04	0.36	8.86	8.91	2.75	2.33	10.76	10.81	ns
	-2	0.49	7.82	0.03	0.91	0.32	7.77	7.82	2.41	2.04	9.44	9.49	ns
6 mA	Std.	0.66	8.05	0.04	1.22	0.43	8.20	7.84	3.54	3.27	10.43	10.08	ns
	-1	0.56	6.85	0.04	1.04	0.36	6.97	6.67	3.01	2.78	8.88	8.57	ns
	-2	0.49	6.01	0.03	0.91	0.32	6.12	5.86	2.64	2.44	7.79	7.53	ns
8 mA	Std.	0.66	7.50	0.04	1.22	0.43	7.64	7.30	3.61	3.41	9.88	9.53	ns
	-1	0.56	6.38	0.04	1.04	0.36	6.50	6.21	3.07	2.90	8.40	8.11	ns
	-2	0.49	5.60	0.03	0.91	0.32	5.71	5.45	2.69	2.55	7.38	7.12	ns
12 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	-1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	-2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns
16 mA	Std.	0.66	7.29	0.04	1.22	0.43	7.23	7.29	3.71	3.95	9.47	9.53	ns
	-1	0.56	6.20	0.04	1.04	0.36	6.15	6.20	3.15	3.36	8.06	8.11	ns
	-2	0.49	5.45	0.03	0.91	0.32	5.40	5.45	2.77	2.95	7.07	7.12	ns

*Note:* For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels**

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL <sup>1</sup>	Output Lower Current	0.65	0.91	1.16	mA
IOH <sup>1</sup>	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIL <sup>2,3</sup>	Input High Leakage Current			10	µA
IIL <sup>2,4</sup>	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

**Notes:**

1. IOL/IOH defined by VODIFF/(Resistor Network)
2. Currents are measured at 85°C junction temperature.
3. IIL is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.
4. IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN < VIL.

**Table 2-91 • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: \*Measuring point =  $V_{trip}$ . See [Table 2-22 on page 2-22](#) for a complete table of trip points.

**Timing Characteristics**
**Table 2-92 • LVDS**

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t <sub>DOUT</sub>	t <sub>DP</sub>	t <sub>DIN</sub>	t <sub>PY</sub>	Units
Std.	0.66	1.83	0.04	1.60	ns
-1	0.56	1.56	0.04	1.36	ns
-2	0.49	1.37	0.03	1.20	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

## Output DDR Module

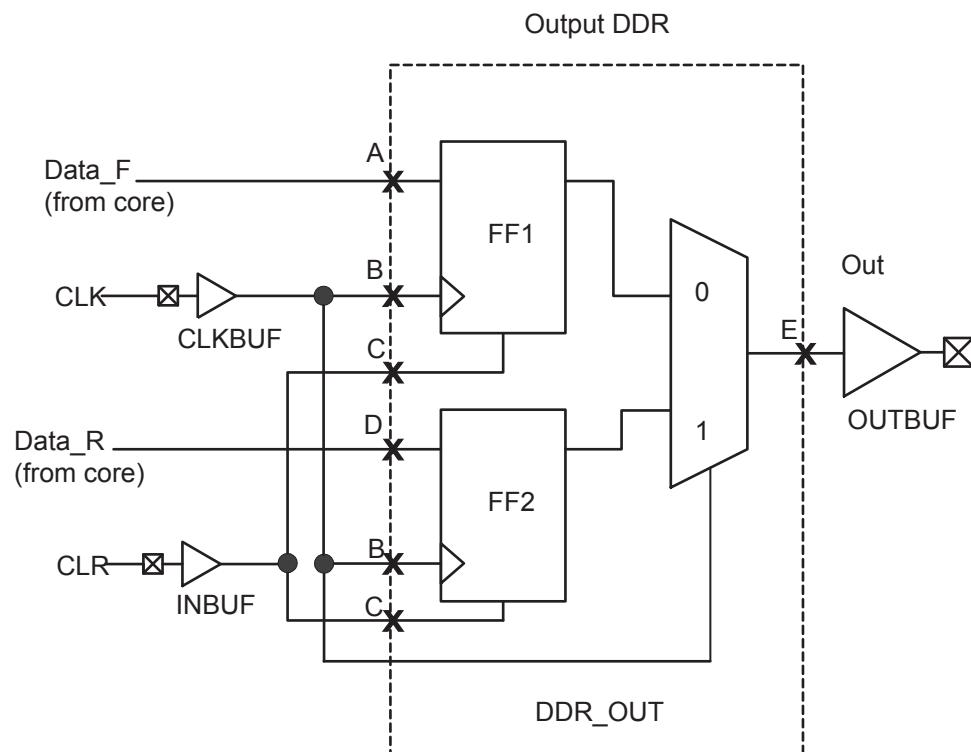


Figure 2-22 • Output DDR Timing Model

Table 2-103 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

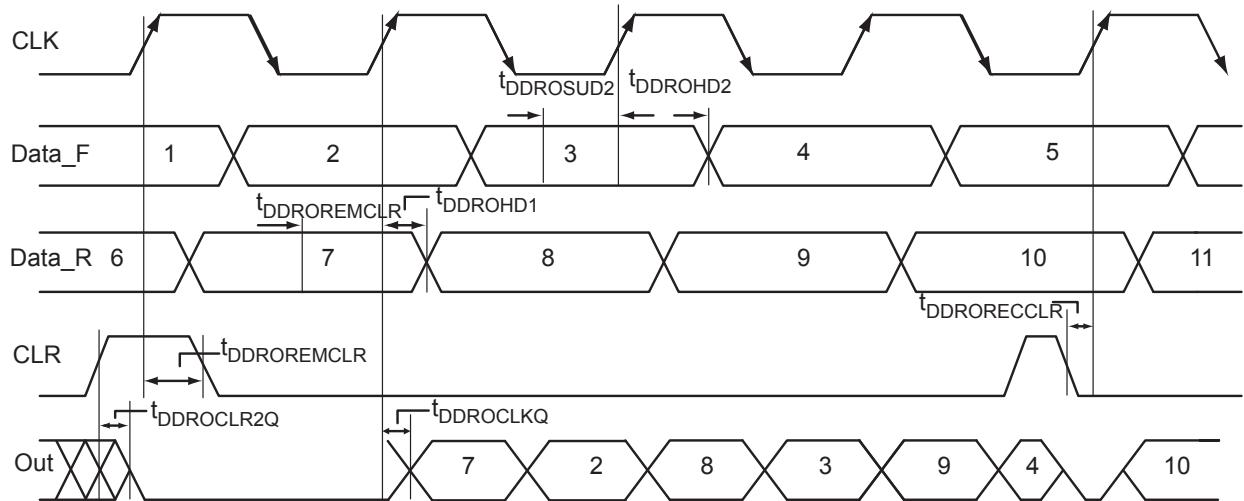


Figure 2-23 • Output DDR Timing Diagram

### Timing Characteristics

Table 2-104 • Output DDR Propagation Delays

Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ , Worst-Case VCC = 1.425 V

Parameter	Description	-2	-1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.70	0.80	0.94	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.38	0.43	0.51	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.80	0.91	1.07	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	0.00	ns
$t_{DDRORECCCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.22	0.25	0.30	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.25	0.30	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.41	0.48	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.37	0.43	ns
$F_{DDOMAX}$	Maximum Frequency for the Output DDR	350	309	263	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

## VersaTile Characteristics

### VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the [Fusion, IGLOO®/e, and ProASIC3/E Macro Library Guide](#).

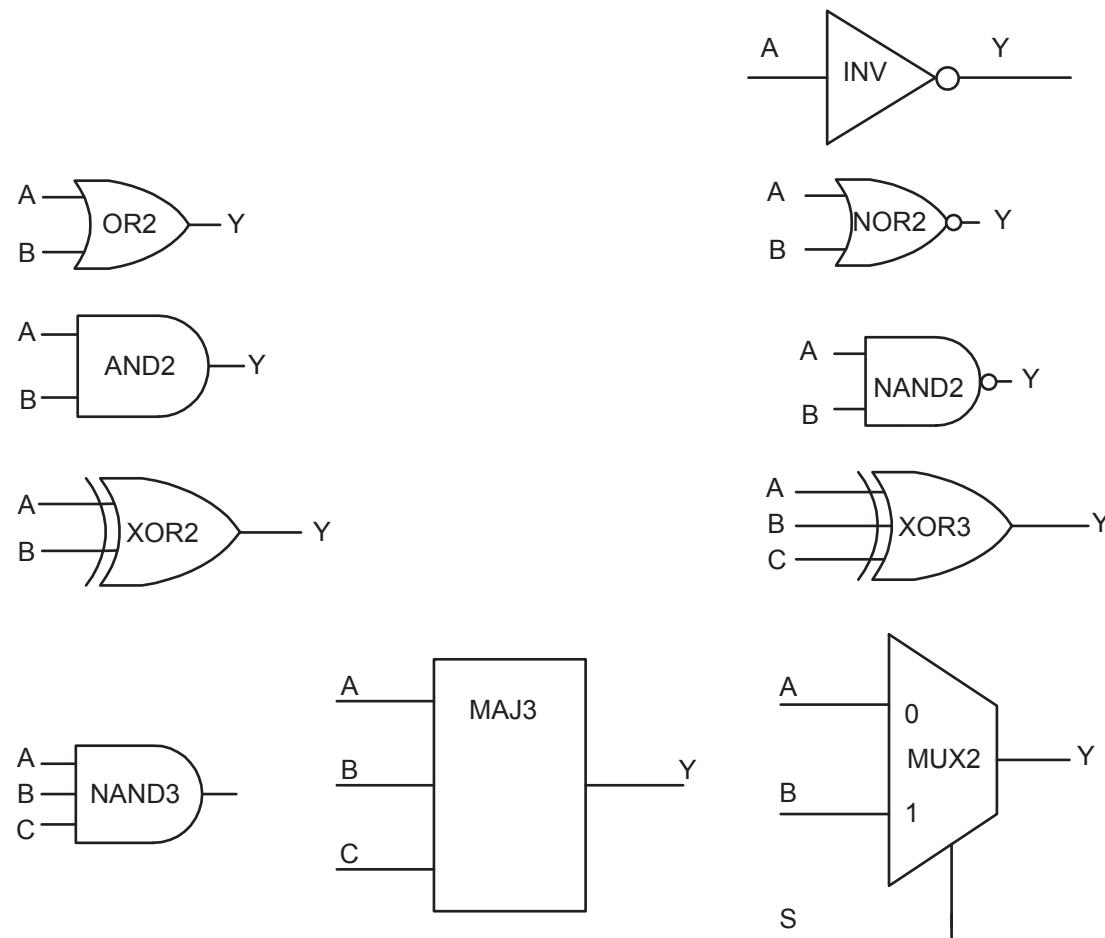


Figure 2-24 • Sample of Combinatorial Cells

**Table 2-113 • A3P600 Global Resource**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $VCC = 1.425 \text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
$t_{RCKH}$	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

**Notes:**

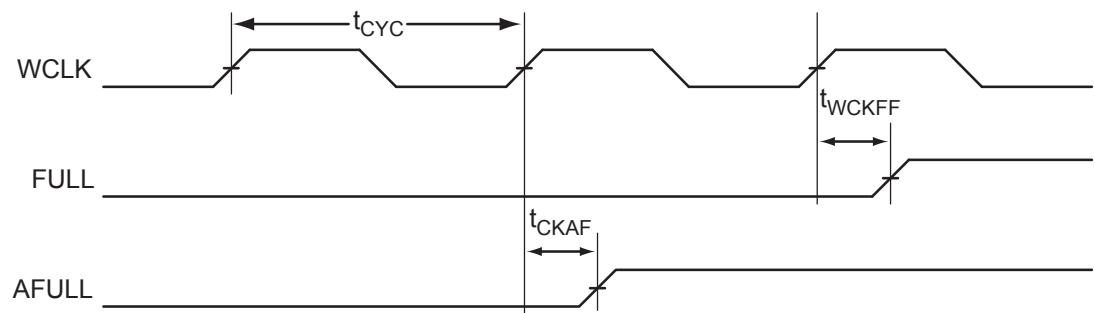
1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

**Table 2-114 • A3P1000 Global Resource**  
 Commercial-Case Conditions:  $T_J = 70^\circ\text{C}$ ,  $VCC = 1.425 \text{ V}$

Parameter	Description	-2		-1		Std.		Units
		Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	Min. <sup>1</sup>	Max. <sup>2</sup>	
$t_{RCKL}$	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
$t_{RCKH}$	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
$t_{RCKSW}$	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

**Notes:**

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.



WA/RA  
(Address Counter) NO MATCH NO MATCH Dist = AFF\_TH MATCH (FULL)

Figure 2-41 • FIFO FULL Flag and AFULL Flag Assertion

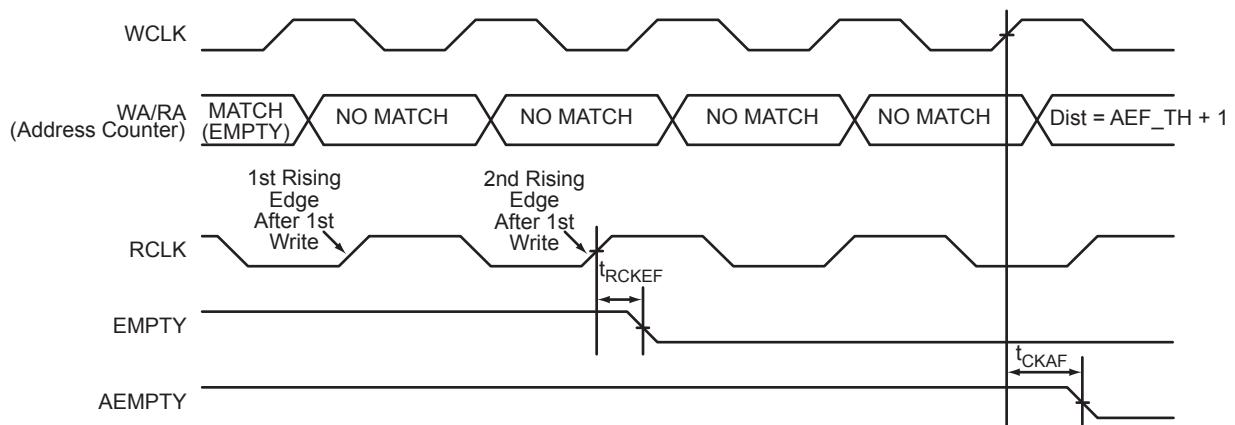


Figure 2-42 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

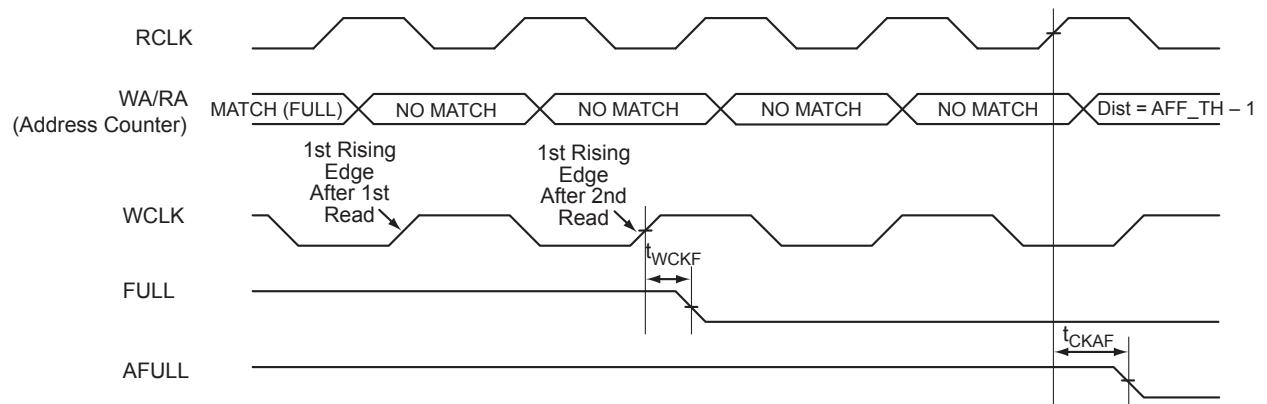
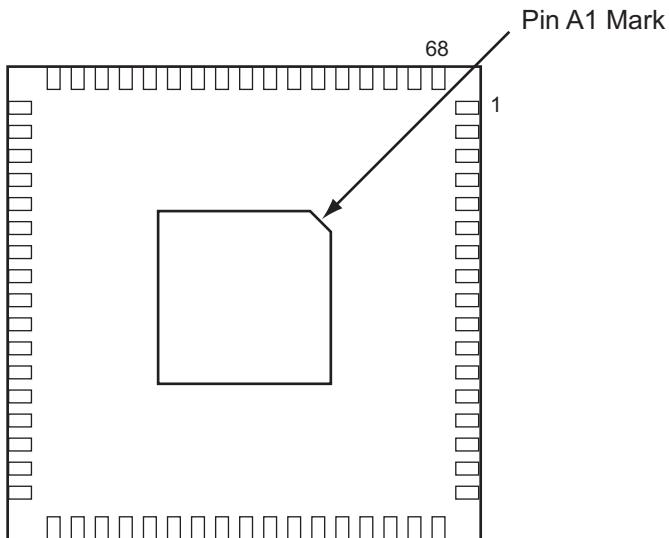


Figure 2-43 • FIFO FULL Flag and AFULL Flag Deassertion

## QN68 – Bottom View

---



**Note:** *The die attach paddle center of the package is tied to ground (GND).*

---

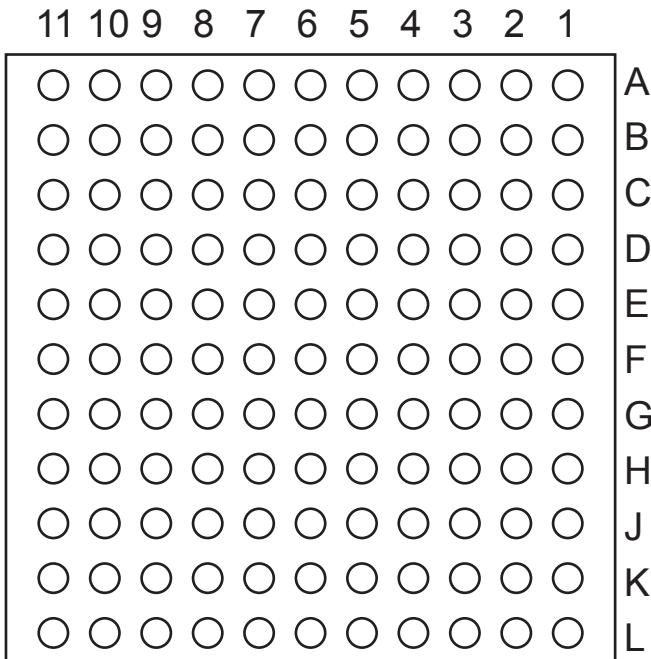
### Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

<b>QN132</b>	
<b>Pin Number</b>	<b>A3P030 Function</b>
C17	IO51RSB1
C18	NC
C19	TCK
C20	NC
C21	VPUMP
C22	VJTAG
C23	NC
C24	NC
C25	NC
C26	GDB0/IO38RSB0
C27	NC
C28	VCCIB0
C29	IO32RSB0
C30	IO29RSB0
C31	IO28RSB0
C32	IO25RSB0
C33	NC
C34	NC
C35	VCCIB0
C36	IO17RSB0
C37	IO14RSB0
C38	IO11RSB0
C39	IO07RSB0
C40	IO04RSB0
D1	GND
D2	GND
D3	GND
D4	GND

## CS121 – Bottom View

---



**Note:** *The die attach paddle center of the package is tied to ground (GND).*

---

### Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

<b>PQ208</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO115UDB3
9	IO115VDB3
10	IO114UDB3
11	IO114VDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	VCC
17	GND
18	VCCIB3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	VCOMPLF
26	GFA0/IO108NPB3
27	VCCPLF
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC

<b>PQ208</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
37	IO104PDB3
38	IO104NDB3
39	IO103PSB3
40	VCCIB3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	VCCIB2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	VCC
72	VCCIB2

<b>PQ208</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	VCC
89	VCCIB2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO16RSB0
A6	GND
A7	IO30RSB0
A8	VCC
A9	IO34RSB0
A10	GBA0/IO58RSB0
A11	GBA1/IO59RSB0
A12	GNDQ
B1	GAB2/IO154UDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO14RSB0
B6	IO19RSB0
B7	IO23RSB0
B8	IO31RSB0
B9	GBB0/IO56RSB0
B10	GBB1/IO57RSB0
B11	GND
B12	VMV1
C1	IO154VDB3
C2	GFA2/IO144PPB3
C3	GAC2/IO153UDB3
C4	VCC
C5	IO12RSB0
C6	IO17RSB0
C7	IO25RSB0
C8	IO32RSB0
C9	IO53RSB0
C10	GBA2/IO60PDB1
C11	IO60NDB1
C12	GBC2/IO62PPB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
D1	IO149NDB3
D2	IO149PDB3
D3	IO153VDB3
D4	GAA2/IO155UPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO54RSB0
D8	GBC1/IO55RSB0
D9	GBB2/IO61PDB1
D10	IO61NDB1
D11	IO62NPB1
D12	GCB1/IO68PPB1
E1	VCC
E2	GFC0/IO147NDB3
E3	GFC1/IO147PDB3
E4	VCCIB3
E5	IO155VPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO67PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO69NDB1
E12	IO70NDB1
F1	GFB0/IO146NPB3
F2	VCOMPLF
F3	GFB1/IO146PPB3
F4	IO144NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO67NDB1
F9	GCB0/IO68NPB1
F10	GND
F11	GCA1/IO69PDB1
F12	GCA2/IO70PDB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P400 Function</b>
G1	GFA1/IO145PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO145NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO77UPB1
G9	IO72NDB1
G10	GCC2/IO72PDB1
G11	IO71NDB1
G12	GCB2/IO71PDB1
H1	VCC
H2	GFB2/IO143PDB3
H3	GFC2/IO142PSB3
H4	GEC1/IO137PDB3
H5	VCC
H6	IO75PDB1
H7	IO75NDB1
H8	GDB2/IO81RSB2
H9	GDC0/IO77VPB1
H10	VCCIB1
H11	IO73PSB1
H12	VCC
J1	GEB1/IO136PDB3
J2	IO143NDB3
J3	VCCIB3
J4	GEC0/IO137NDB3
J5	IO125RSB2
J6	IO116RSB2
J7	VCC
J8	TCK
J9	GDA2/IO80RSB2
J10	TDO
J11	GDA1/IO79UDB1
J12	GDB1/IO78UDB1

<b>FG144</b>	
<b>Pin Number</b>	<b>A3P1000 Function</b>
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	VCCIB2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	VJTAG
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	VCCIB2
M11	VPUMP
M12	GNDQ

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

<b>FG256</b>	
<b>Pin Number</b>	<b>A3P250 Function</b>
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2