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Understanding [Embedded - FPGAs \(Field Programmable Gate Array\)](#)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details

Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-2fgg256

Your valuable IP is protected with industry-standard security, making remote ISP possible. A ProASIC3 device provides the best available security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Instant On

Flash-based ProASIC3 devices support Level 0 of the Instant On classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The Instant On feature of flash-based ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and clock generation PLLs that are used for these purposes in a system. In addition, glitches and brownouts in system power will not corrupt the ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based ProASIC3 devices exhibit power characteristics similar to an ASIC, making them an ideal choice for power-sensitive applications. ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

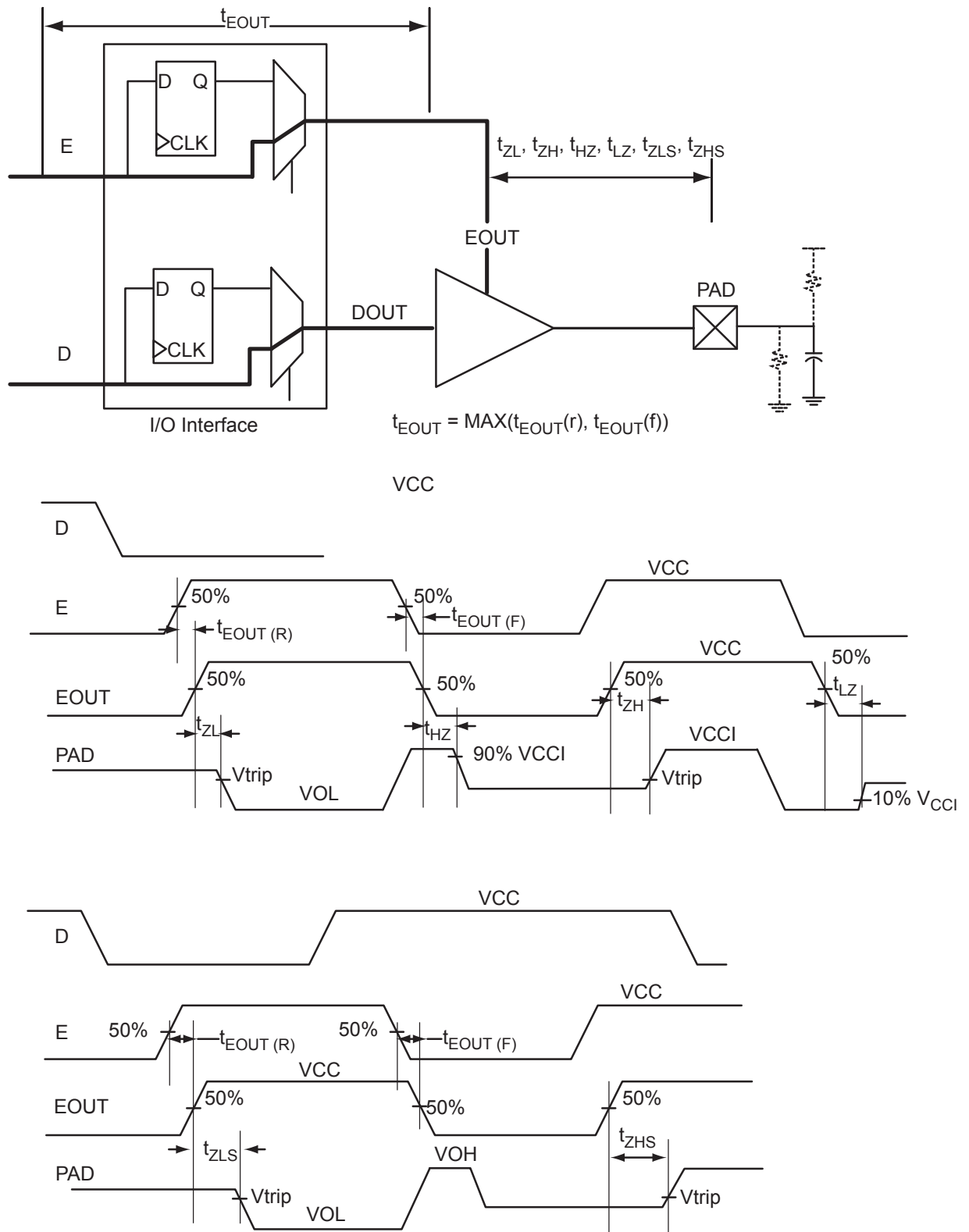


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (Example)

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings
 –2 Speed Grade, Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$,
 Worst-Case V_{CCI} (per standard)
 Advanced I/O Banks

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option ¹	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
3.3 V LVCMOS Wide Range ²	100 μA	12 mA	High	35	–	0.45	4.08	0.03	0.76	0.32	4.08	3.20	3.71	4.14	6.61	5.74	ns
2.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
1.8 V LVCMOS	12 mA	12 mA	High	35	–	0.45	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
1.5 V LVCMOS	12 mA	12 mA	High	35	–	0.45	3.05	0.03	1.07	0.32	3.10	2.67	2.95	3.14	4.77	4.34	ns
3.3 V PCI	Per PCI spec	–	High	10	25 ⁴	0.45	2.00	0.03	0.65	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
3.3 V PCI-X	Per PCI-X spec	–	High	10	25 ⁴	0.45	2.00	0.03	0.62	0.32	2.04	1.46	2.40	2.68	3.71	3.13	ns
LVDS	24 mA	–	High	–	–	0.45	1.37	0.03	1.20	–	–	–	–	–	–	–	ns
LVPECL	24 mA	–	High	–	–	0.45	1.34	0.03	1.05	–	–	–	–	–	–	–	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.
4. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-64](#) for connectivity. This resistor is not required during normal operation.

Table 2-33 • I/O Short Currents IOSH/IOSL
Applicable to Standard Plus I/O Banks

	Drive Strength	IOSL (mA) ¹	IOSH (mA) ¹
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
3.3 V LVCMOS Wide Range ²	100 μ A	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

Notes:

1. $T_J = 100^{\circ}\text{C}$
2. Applicable to 3.3 V LVCMOS Wide Range. IOSL/IOSH dependent on the I/O buffer drive strength selected for wide range applications. All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.

Timing Characteristics

Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
4 mA	Std.	0.66	7.66	0.04	1.02	0.43	7.80	6.59	2.65	2.61	10.03	8.82	ns
	–1	0.56	6.51	0.04	0.86	0.36	6.63	5.60	2.25	2.22	8.54	7.51	ns
	–2	0.49	5.72	0.03	0.76	0.32	5.82	4.92	1.98	1.95	7.49	6.59	ns
6 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
8 mA	Std.	0.66	4.91	0.04	1.02	0.43	5.00	4.07	2.99	3.20	7.23	6.31	ns
	–1	0.56	4.17	0.04	0.86	0.36	4.25	3.46	2.54	2.73	6.15	5.36	ns
	–2	0.49	3.66	0.03	0.76	0.32	3.73	3.04	2.23	2.39	5.40	4.71	ns
12 mA	Std.	0.66	3.53	0.04	1.02	0.43	3.60	2.82	3.21	3.58	5.83	5.06	ns
	–1	0.56	3.00	0.04	0.86	0.36	3.06	2.40	2.73	3.05	4.96	4.30	ns
	–2	0.49	2.64	0.03	0.76	0.32	2.69	2.11	2.40	2.68	4.36	3.78	ns
16 mA	Std.	0.66	3.33	0.04	1.02	0.43	3.39	2.56	3.26	3.68	5.63	4.80	ns
	–1	0.56	2.83	0.04	0.86	0.36	2.89	2.18	2.77	3.13	4.79	4.08	ns
	–2	0.49	2.49	0.03	0.76	0.32	2.53	1.91	2.44	2.75	4.20	3.58	ns
24 mA	Std.	0.66	3.08	0.04	1.02	0.43	3.13	2.12	3.32	4.06	5.37	4.35	ns
	–1	0.56	2.62	0.04	0.86	0.36	2.66	1.80	2.83	3.45	4.57	3.70	ns
	–2	0.49	2.30	0.03	0.76	0.32	2.34	1.58	2.48	3.03	4.01	3.25	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-51 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option ¹	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 μA	2 mA	Std.	0.60	15.86	0.04	1.54	0.43	15.86	13.51	4.09	3.80	19.25	16.90	ns
		–1	0.51	13.49	0.04	1.31	0.36	13.49	11.49	3.48	3.23	16.38	14.38	ns
		–2	0.45	11.84	0.03	1.15	0.32	11.84	10.09	3.05	2.84	14.38	12.62	ns
100 μA	4 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	6 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 μA	8 mA	Std.	0.60	8.63	0.04	1.54	0.43	8.63	7.39	4.96	5.28	12.02	10.79	ns
		–1	0.51	7.34	0.04	1.31	0.36	7.34	6.29	4.22	4.49	10.23	9.18	ns
		–2	0.45	6.44	0.03	1.15	0.32	6.44	5.52	3.70	3.94	8.98	8.06	ns
100 μA	16 mA	Std.	0.60	8.05	0.04	1.54	0.43	8.05	6.93	5.03	5.43	11.44	10.32	ns
		–1	0.51	6.85	0.04	1.31	0.36	6.85	5.90	4.28	4.62	9.74	8.78	ns
		–2	0.45	6.01	0.03	1.15	0.32	6.01	5.18	3.76	4.06	8.55	7.71	ns
100 μA	24 mA	Std.	0.60	7.50	0.04	1.54	0.43	7.50	6.90	5.13	6.00	10.89	10.29	ns
		–1	0.51	6.38	0.04	1.31	0.36	6.38	5.87	4.36	5.11	9.27	8.76	ns
		–2	0.45	5.60	0.03	1.15	0.32	5.60	5.15	3.83	4.48	8.13	7.69	ns

Notes:

1. The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is $\pm 100\text{ }\mu\text{A}$. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-61 • 2.5 V LVCMOS Low Slew
Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	11.40	0.04	1.31	0.43	11.22	11.40	2.68	2.20	13.45	13.63	ns
	–1	0.51	9.69	0.04	1.11	0.36	9.54	9.69	2.28	1.88	11.44	11.60	ns
	–2	0.45	8.51	0.03	0.98	0.32	8.38	8.51	2.00	1.65	10.05	10.18	ns
6 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
8 mA	Std.	0.60	7.96	0.04	1.31	0.43	8.11	7.81	3.05	2.89	10.34	10.05	ns
	–1	0.51	6.77	0.04	1.11	0.36	6.90	6.65	2.59	2.46	8.80	8.55	ns
	–2	0.45	5.94	0.03	0.98	0.32	6.05	5.84	2.28	2.16	7.72	7.50	ns
12 mA	Std.	0.60	6.18	0.04	1.31	0.43	6.29	5.92	3.30	3.32	8.53	8.15	ns
	–1	0.51	5.26	0.04	1.11	0.36	5.35	5.03	2.81	2.83	7.26	6.94	ns
	–2	0.45	4.61	0.03	0.98	0.32	4.70	4.42	2.47	2.48	6.37	6.09	ns
16 mA	Std.	0.60	5.76	0.04	1.31	0.43	5.87	5.53	3.36	3.44	8.11	7.76	ns
	–1	0.51	4.90	0.04	1.11	0.36	4.99	4.70	2.86	2.92	6.90	6.60	ns
	–2	0.45	4.30	0.03	0.98	0.32	4.38	4.13	2.51	2.57	6.05	5.80	ns
24 mA	Std.	0.60	5.51	0.04	1.31	0.43	5.50	5.51	3.43	3.87	7.74	7.74	ns
	–1	0.51	4.68	0.04	1.11	0.36	4.68	4.68	2.92	3.29	6.58	6.59	ns
	–2	0.45	4.11	0.03	0.98	0.32	4.11	4.11	2.56	2.89	5.78	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Output DDR Module

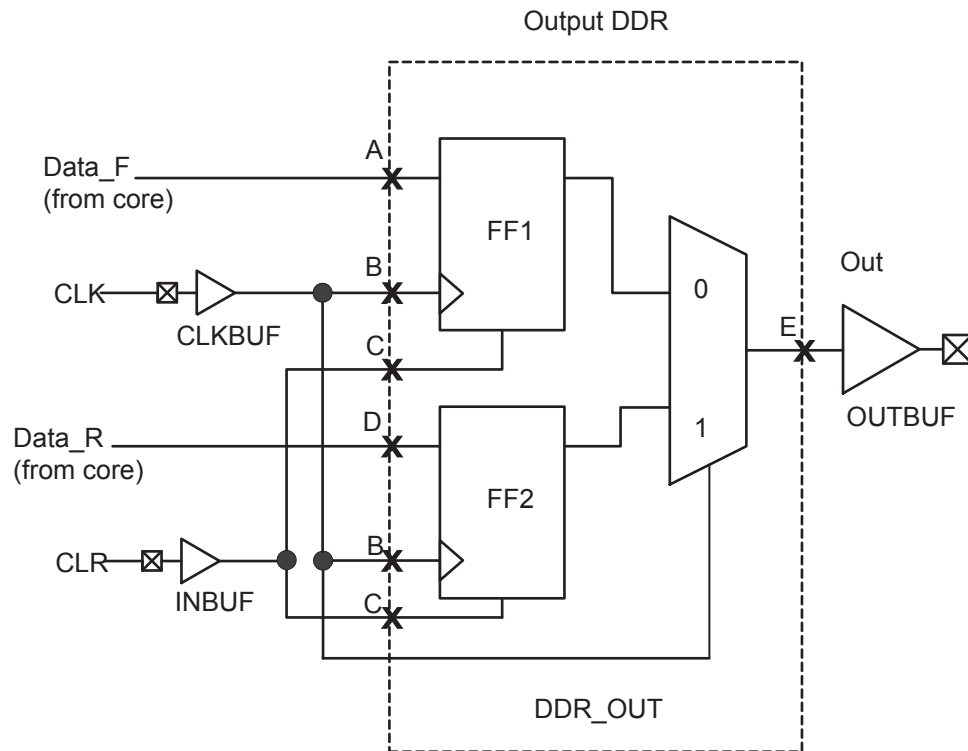


Figure 2-22 • Output DDR Timing Model

Table 2-103 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDROCLKQ}	Clock-to-Out	B, E
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out	C, E
$t_{\text{DDROREMCLR}}$	Clear Removal	C, B
$t_{\text{DDRORECCLR}}$	Clear Recovery	C, B
t_{DDROSUD1}	Data Setup Data_F	A, B
t_{DDROSUD2}	Data Setup Data_R	D, B
t_{DDROHD1}	Data Hold Data_F	A, B
t_{DDROHD2}	Data Hold Data_R	D, B

Timing Characteristics

Table 2-107 • A3P015 Global Resource
 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.66	0.81	0.75	0.92	0.88	1.08	ns
t_{RCKH}	Input High Delay for Global Clock	0.67	0.84	0.76	0.96	0.89	1.13	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.25	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage-supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Table 2-108 • A3P030 Global Resource
 Commercial-Case Conditions: $T_J = 70^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–2		–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input Low Delay for Global Clock	0.67	0.81	0.76	0.92	0.89	1.09	ns
t_{RCKH}	Input High Delay for Global Clock	0.68	0.85	0.77	0.97	0.91	1.14	ns
t_{RCKMPWH}	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
t_{RCKMPWL}	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.18		0.21		0.24	ns

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-6 on page 2-6](#) for derating values.

Timing Waveforms

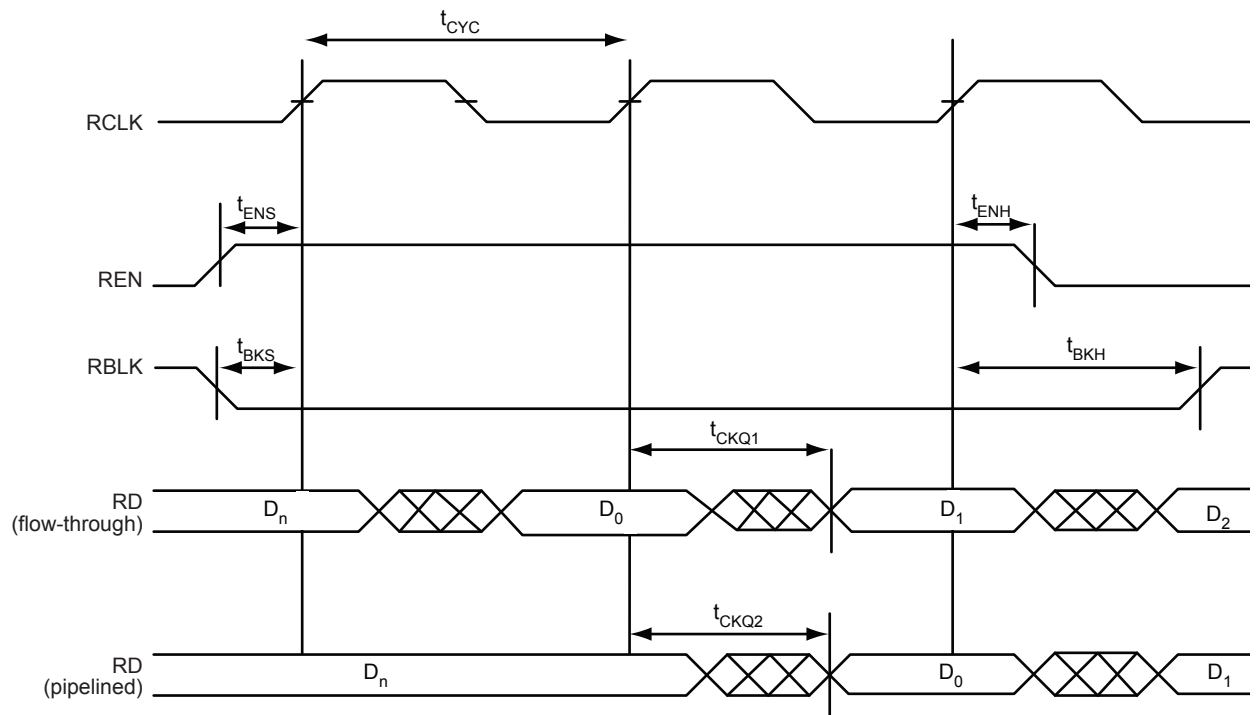


Figure 2-37 • FIFO Read

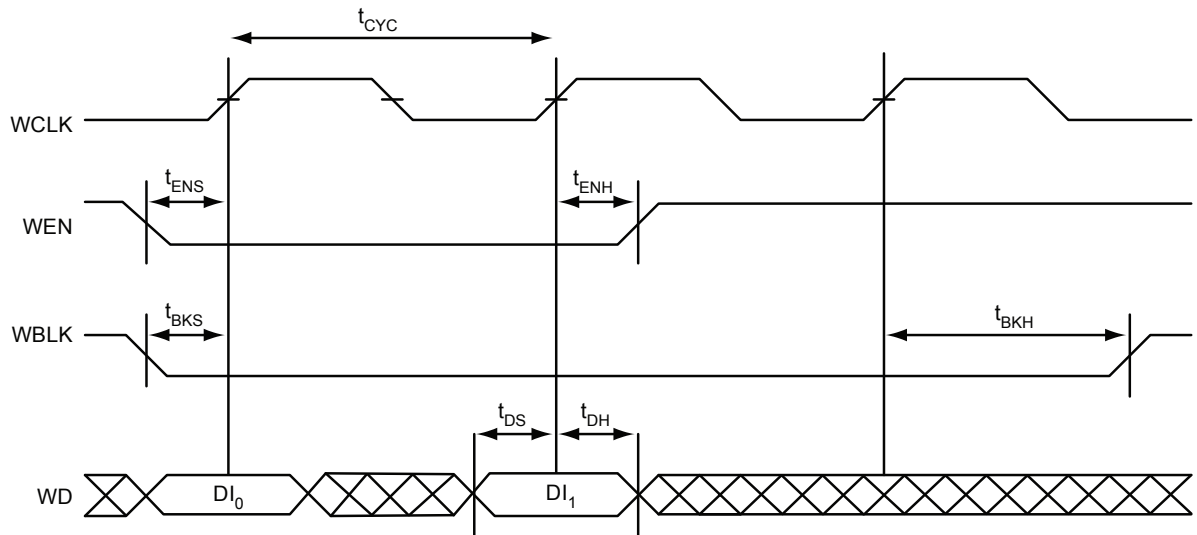


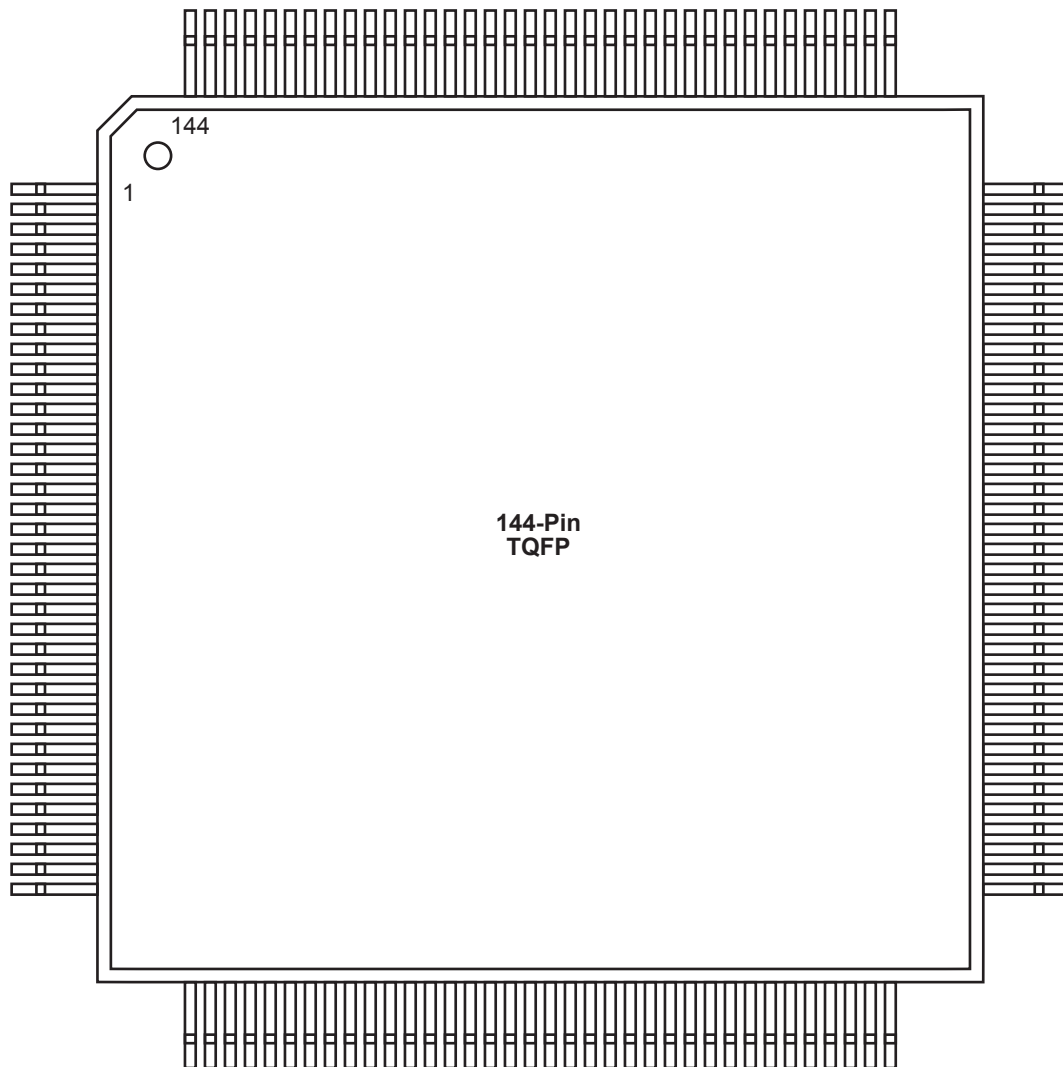
Figure 2-38 • FIFO Write

Table 2-121 • A3P250 FIFO 1k×4**Worst Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, $V_{CC} = 1.425\text{ V}$**

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	4.05	4.61	5.42	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.36	2.68	3.15	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.89	1.02	1.20	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
t_{REMRSTB}	RESET Removal	0.29	0.33	0.38	ns
t_{RECRSTB}	RESET Recovery	1.50	1.71	2.01	ns
t_{MPWRSTB}	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

QN132	
Pin Number	A3P060 Function
C17	IO57RSB1
C18	NC
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO42RSB0
C27	GCC0/IO39RSB0
C28	VCCIB0
C29	IO29RSB0
C30	GNDQ
C31	GBA1/IO27RSB0
C32	GBB0/IO24RSB0
C33	VCC
C34	IO19RSB0
C35	IO16RSB0
C36	IO13RSB0
C37	GAC1/IO10RSB0
C38	NC
C39	GAA0/IO05RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TQ144 – Top View



Note

For more information on package drawings, see [PD3068: Package Mechanical Drawings](#).

PQ208	
Pin Number	A3P400 Function
1	GND
2	GAA2/IO155UDB3
3	IO155VDB3
4	GAB2/IO154UDB3
5	IO154VDB3
6	GAC2/IO153UDB3
7	IO153VDB3
8	IO152UDB3
9	IO152VDB3
10	IO151UDB3
11	IO151VDB3
12	IO150PDB3
13	IO150NDB3
14	IO149PDB3
15	IO149NDB3
16	VCC
17	GND
18	VCCIB3
19	IO148PDB3
20	IO148NDB3
21	GFC1/IO147PDB3
22	GFC0/IO147NDB3
23	GFB1/IO146PDB3
24	GFB0/IO146NDB3
25	VCOMPLF
26	GFA0/IO145NPB3
27	VCCPLF
28	GFA1/IO145PPB3
29	GND
30	GFA2/IO144PDB3
31	IO144NDB3
32	GFB2/IO143PDB3
33	IO143NDB3
34	GFC2/IO142PDB3
35	IO142NDB3
36	NC

PQ208	
Pin Number	A3P400 Function
37	IO141PSB3
38	IO140PDB3
39	IO140NDB3
40	VCCIB3
41	GND
42	IO138PDB3
43	IO138NDB3
44	GEC1/IO137PDB3
45	GEC0/IO137NDB3
46	GEB1/IO136PDB3
47	GEB0/IO136NDB3
48	GEA1/IO135PDB3
49	GEA0/IO135NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	NC
55	GEA2/IO134RSB2
56	GEB2/IO133RSB2
57	GEC2/IO132RSB2
58	IO131RSB2
59	IO130RSB2
60	IO129RSB2
61	IO128RSB2
62	VCCIB2
63	IO125RSB2
64	IO123RSB2
65	GND
66	IO121RSB2
67	IO119RSB2
68	IO117RSB2
69	IO115RSB2
70	IO113RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P400 Function
73	IO112RSB2
74	IO111RSB2
75	IO110RSB2
76	IO109RSB2
77	IO108RSB2
78	IO107RSB2
79	IO106RSB2
80	IO104RSB2
81	GND
82	IO102RSB2
83	IO101RSB2
84	IO100RSB2
85	IO99RSB2
86	IO98RSB2
87	IO97RSB2
88	VCC
89	VCCIB2
90	IO94RSB2
91	IO92RSB2
92	IO90RSB2
93	IO88RSB2
94	IO86RSB2
95	IO84RSB2
96	GDC2/IO82RSB2
97	GND
98	GDB2/IO81RSB2
99	GDA2/IO80RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

PQ208	
Pin Number	A3P1000 Function
1	GND
2	GAA2/IO225PDB3
3	IO225NDB3
4	GAB2/IO224PDB3
5	IO224NDB3
6	GAC2/IO223PDB3
7	IO223NDB3
8	IO222PDB3
9	IO222NDB3
10	IO220PDB3
11	IO220NDB3
12	IO218PDB3
13	IO218NDB3
14	IO216PDB3
15	IO216NDB3
16	VCC
17	GND
18	VCCIB3
19	IO212PDB3
20	IO212NDB3
21	GFC1/IO209PDB3
22	GFC0/IO209NDB3
23	GFB1/IO208PDB3
24	GFB0/IO208NDB3
25	VCOMPLF
26	GFA0/IO207NPB3
27	VCCPLF
28	GFA1/IO207PPB3
29	GND
30	GFA2/IO206PDB3
31	IO206NDB3
32	GFB2/IO205PDB3
33	IO205NDB3
34	GFC2/IO204PDB3
35	IO204NDB3
36	VCC

PQ208	
Pin Number	A3P1000 Function
37	IO199PDB3
38	IO199NDB3
39	IO197PSB3
40	VCCIB3
41	GND
42	IO191PDB3
43	IO191NDB3
44	GEC1/IO190PDB3
45	GEC0/IO190NDB3
46	GEB1/IO189PDB3
47	GEB0/IO189NDB3
48	GEA1/IO188PDB3
49	GEA0/IO188NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	GEA2/IO187RSB2
55	GEB2/IO186RSB2
56	GEC2/IO185RSB2
57	IO184RSB2
58	IO183RSB2
59	IO182RSB2
60	IO181RSB2
61	IO180RSB2
62	VCCIB2
63	IO178RSB2
64	IO176RSB2
65	GND
66	IO174RSB2
67	IO172RSB2
68	IO170RSB2
69	IO168RSB2
70	IO166RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P1000 Function
73	IO162RSB2
74	IO160RSB2
75	IO158RSB2
76	IO156RSB2
77	IO154RSB2
78	IO152RSB2
79	IO150RSB2
80	IO148RSB2
81	GND
82	IO143RSB2
83	IO141RSB2
84	IO139RSB2
85	IO137RSB2
86	IO135RSB2
87	IO133RSB2
88	VCC
89	VCCIB2
90	IO128RSB2
91	IO126RSB2
92	IO124RSB2
93	IO122RSB2
94	IO120RSB2
95	IO118RSB2
96	GDC2/IO116RSB2
97	GND
98	GDB2/IO115RSB2
99	GDA2/IO114RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	GNDQ
108	TDO

PQ208	
Pin Number	A3P1000 Function
109	TRST
110	VJTAG
111	GDA0/IO113NDB1
112	GDA1/IO113PDB1
113	GDB0/IO112NDB1
114	GDB1/IO112PDB1
115	GDC0/IO111NDB1
116	GDC1/IO111PDB1
117	IO109NDB1
118	IO109PDB1
119	IO106NDB1
120	IO106PDB1
121	IO104PSB1
122	GND
123	VCCIB1
124	IO99NDB1
125	IO99PDB1
126	NC
127	IO96NDB1
128	GCC2/IO96PDB1
129	GCB2/IO95PSB1
130	GND
131	GCA2/IO94PSB1
132	GCA1/IO93PDB1
133	GCA0/IO93NDB1
134	GCB0/IO92NDB1
135	GCB1/IO92PDB1
136	GCC0/IO91NDB1
137	GCC1/IO91PDB1
138	IO88NDB1
139	IO88PDB1
140	VCCIB1
141	GND
142	VCC
143	IO86PSB1
144	IO84NDB1

PQ208	
Pin Number	A3P1000 Function
145	IO84PDB1
146	IO82NDB1
147	IO82PDB1
148	IO80NDB1
149	GBC2/IO80PDB1
150	IO79NDB1
151	GBB2/IO79PDB1
152	IO78NDB1
153	GBA2/IO78PDB1
154	VMV1
155	GNDQ
156	GND
157	VMV0
158	GBA1/IO77RSB0
159	GBA0/IO76RSB0
160	GBB1/IO75RSB0
161	GBB0/IO74RSB0
162	GND
163	GBC1/IO73RSB0
164	GBC0/IO72RSB0
165	IO70RSB0
166	IO67RSB0
167	IO63RSB0
168	IO60RSB0
169	IO57RSB0
170	VCCIB0
171	VCC
172	IO54RSB0
173	IO51RSB0
174	IO48RSB0
175	IO45RSB0
176	IO42RSB0
177	IO40RSB0
178	GND
179	IO38RSB0
180	IO35RSB0

PQ208	
Pin Number	A3P1000 Function
181	IO33RSB0
182	IO31RSB0
183	IO29RSB0
184	IO27RSB0
185	IO25RSB0
186	VCCIB0
187	VCC
188	IO22RSB0
189	IO20RSB0
190	IO18RSB0
191	IO16RSB0
192	IO15RSB0
193	IO14RSB0
194	IO13RSB0
195	GND
196	IO12RSB0
197	IO11RSB0
198	IO10RSB0
199	IO09RSB0
200	VCCIB0
201	GAC1/IO05RSB0
202	GAC0/IO04RSB0
203	GAB1/IO03RSB0
204	GAB0/IO02RSB0
205	GAA1/IO01RSB0
206	GAA0/IO00RSB0
207	GNDQ
208	VMV0

FG484	
Pin Number	A3P1000 Function
A1	GND
A2	GND
A3	VCCIB0
A4	IO07RSB0
A5	IO09RSB0
A6	IO13RSB0
A7	IO18RSB0
A8	IO20RSB0
A9	IO26RSB0
A10	IO32RSB0
A11	IO40RSB0
A12	IO41RSB0
A13	IO53RSB0
A14	IO59RSB0
A15	IO64RSB0
A16	IO65RSB0
A17	IO67RSB0
A18	IO69RSB0
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	IO06RSB0
B5	IO08RSB0
B6	IO12RSB0
B7	IO15RSB0
B8	IO19RSB0
B9	IO24RSB0
B10	IO31RSB0
B11	IO39RSB0
B12	IO48RSB0
B13	IO54RSB0
B14	IO58RSB0

FG484	
Pin Number	A3P1000 Function
B15	IO63RSB0
B16	IO66RSB0
B17	IO68RSB0
B18	IO70RSB0
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	IO220PDB3
C3	NC
C4	NC
C5	GND
C6	IO10RSB0
C7	IO14RSB0
C8	VCC
C9	VCC
C10	IO30RSB0
C11	IO37RSB0
C12	IO43RSB0
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	IO219PDB3
D2	IO220NDB3
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0

FG484	
Pin Number	A3P1000 Function
D7	GAB0/IO02RSB0
D8	IO16RSB0
D9	IO22RSB0
D10	IO28RSB0
D11	IO35RSB0
D12	IO45RSB0
D13	IO50RSB0
D14	IO55RSB0
D15	IO61RSB0
D16	GBB1/IO75RSB0
D17	GBA0/IO76RSB0
D18	GBA1/IO77RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	IO219NDB3
E2	NC
E3	GND
E4	GAB2/IO224PDB3
E5	GAA2/IO225PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO17RSB0
E9	IO21RSB0
E10	IO27RSB0
E11	IO34RSB0
E12	IO44RSB0
E13	IO51RSB0
E14	IO57RSB0
E15	GBC1/IO73RSB0
E16	GBB0/IO74RSB0
E17	IO71RSB0
E18	GAA2/IO78PDB1
E19	IO81PDB1
E20	GND

5 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each version of the ProASIC3 datasheet.

Revision	Changes	Page
Revision 18 (March 2016)	Updated 3.3 V DC supply voltage's maximum Commercial and Industrial values from 3.3 V to 3.6 V in Table 2-2 (SAR 72693).	2-2
	Added reference of Package Mechanical Drawings document in all package pin assignment notes (76833).	NA
Revision 17 (June 2015)	Removed PQFP embedded heat spreader info. from Table 2-5 (SAR 52320).	2-6
	Updated " VCCIBx I/O Supply Voltage " (SAR 43323).	3-1
Revision 16 (December 2014)	Updated " ProASIC3 Ordering Information ". Interchanged the positions of Y- Security Feature and I- Application (Temperature Range) (SAR 61079). Added Note "Only devices with package size greater than or equal to 5x5 are supported".	1-IV
	Updated Table Note (2) in Table 2-3 • Flash Programming Limits – Retention, Storage and Operating Temperature so that the Table Note is not applicable for Maximum Storage Temperature T _{STG} (SAR 54297).	2-3
	Added values for Drive strength 2 mA in Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew , Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew , Table 2-43 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew , and Table 2-44 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew (SAR 57184).	2-34, 2-35, 2-36, 2-37
	Added Figure 2-1 • High-Temperature Data Retention (HTR) (SAR 45466).	2-3
	Updates made to maintain the style and consistency of the document.	NA
Revision 15 (July 2014)	Added corner pad table note (3) to " QN132 – Bottom View " (SAR 47442).	4-6
	Ambient temperature removed in Table 2-2 , table notes and " ProASIC3 Ordering Information " figure were modified (SAR 48343).	2-2 1-IV
	Other updates were made to maintain the style and consistency of the datasheet.	NA
Revision 14 (April 2014)	Note added for the discontinuance of QN132 package to the following tables and section: " ProASIC3 Devices ", " I/Os Per Package 1 ", " ProASIC3 FPGAs Package Sizes Dimensions " and " QN132 – Bottom View " section (SAR 55118).	I, III, 4-6

Revision	Changes	Page
Advance v0.2, (continued)	Table 2-43 was updated.	2-64
	Table 2-18 was updated.	2-45
	Pin descriptions in the "JTAG Pins" section were updated.	2-51
	The "User I/O Naming Convention" section was updated.	2-48
	Table 3-7 was updated.	3-6
	The "Methodology" section was updated.	3-10
	Table 3-40 and Table 3-39 were updated.	3-33,3-32
	The A3P250 "100-Pin VQFP*" pin table was updated.	4-14
	The A3P250 "208-Pin PQFP*" pin table was updated.	4-23
	The A3P1000 "208-Pin PQFP*" pin table was updated.	4-29
	The A3P250 "144-Pin FBGA*" pin table was updated.	4-36
	The A3P1000 "144-Pin FBGA*" pin table was updated.	4-32
	The A3P250 "256-Pin FBGA*" pin table was updated.	4-45
	The A3P1000 "256-Pin FBGA*" pin table was updated.	4-54
	The A3P1000 "484-Pin FBGA*" pin table was updated.	4-68