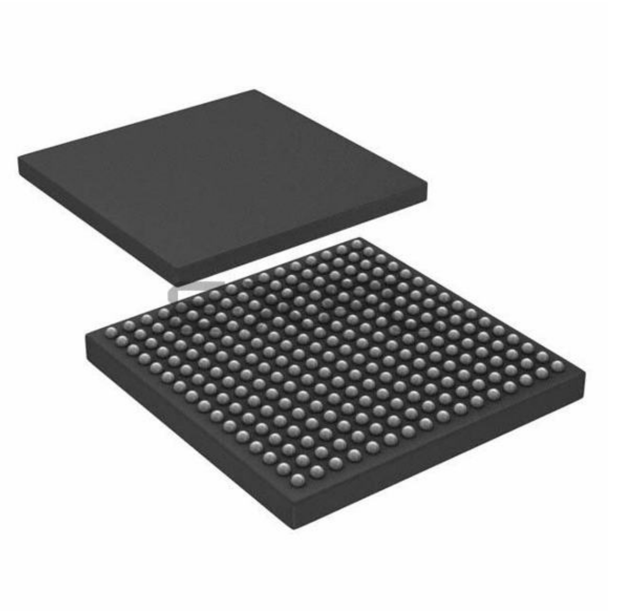
Microchip Technology - M7A3P1000-2FGG256I Datasheet



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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	177
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	-40°C ~ 100°C (TJ)
Package / Case	256-LBGA
Supplier Device Package	256-FPBGA (17x17)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-2fgg256i

User Nonvolatile FlashROM

ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Internet protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, set-top boxes)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard ProASIC3 IEEE 1532 JTAG programming interface. The core can be individually programmed (erased and written), and on-chip AES decryption can be used selectively to securely load data over public networks (except in the A3P015 and A3P030 devices), as in security keys stored in the FlashROM for a user design.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The ProASIC3 development software solutions, Libero® System-on-Chip (SoC) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Libero SoC and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM and FIFO

ProASIC3 devices (except the A3P015 and A3P030 devices) have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro (except in A3P015 and A3P030 devices).

In addition, every SRAM block has an embedded FIFO control unit. The control unit allows the SRAM block to be configured as a synchronous FIFO without using additional core VersaTiles. The FIFO width and depth are programmable. The FIFO also features programmable Almost Empty (AEMPTY) and Almost Full (AFULL) flags in addition to the normal Empty and Full flags. The embedded FIFO control unit contains the counters necessary for generation of the read and write address pointers. The embedded SRAM/FIFO blocks can be cascaded to create larger configurations.

PLL and CCC

ProASIC3 devices provide designers with very flexible clock conditioning capabilities. Each member of the ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL. The A3P015 and A3P030 devices do not have a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

2 – ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-2 on page 2-2 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPUMP	Programming voltage	–0.3 to 3.75	V
VCCPLL	Analog power supply (PLL)	–0.3 to 1.65	V
VCCI	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCI + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T_{STG} [2]	Storage temperature	–65 to +150	°C
T_J [2]	Junction temperature	+125	°C

Notes:

1. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-4 on page 2-3.*
2. *VMV pins must be connected to the corresponding VCCI pins. See the "VMVx I/O Supply Voltage (quiet)" section on page 3-1 for further information.*
3. *For flash programming and retention maximum limits, refer to Table 2-3 on page 2-3, and for recommended operating limits, refer to Table 2-2 on page 2-2.*

The absolute maximum junction temperature is 100°C. EQ 1 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. } (°\text{C}) - \text{Max. ambient temp. } (°\text{C})}{\theta_{ja}(°\text{C/W})} = \frac{100°\text{C} - 70°\text{C}}{20.5°\text{C/W}} = 1.463\ \text{W}$$

EQ 1

Table 2-5 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft/min	500 ft/min	
Quad Flat No Lead	A3P030	132	0.4	21.4	16.8	15.3	°C/W
	A3P060	132	0.3	21.2	16.6	15.0	°C/W
	A3P125	132	0.2	21.1	16.5	14.9	°C/W
	A3P250	132	0.1	21.0	16.4	14.8	°C/W
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Thin Quad Flat Pack (TQFP)	All devices	144	11.0	33.5	28.0	25.7	°C/W
Plastic Quad Flat Pack (PQFP)	All devices	208	8.0	26.1	22.5	20.8	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

Note: *This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

Temperature and Voltage Derating Factors

Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 70°C, VCC = 1.425 V)

Array Voltage VCC (V)	Junction Temperature (°C)					
	–40°C	0°C	25°C	70°C	85°C	100°C
1.425	0.88	0.93	0.95	1.00	1.02	1.04
1.500	0.83	0.88	0.90	0.95	0.96	0.98
1.575	0.80	0.84	0.87	0.91	0.93	0.94

Table 2-51 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Advanced I/O Banks

Drive Strength	Equiv. Software Default Drive Strength Option[1]	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
100 µA	2 mA	Std.	0.60	15.86	0.04	1.54	0.43	15.86	13.51	4.09	3.80	19.25	16.90	ns
		–1	0.51	13.49	0.04	1.31	0.36	13.49	11.49	3.48	3.23	16.38	14.38	ns
		–2	0.45	11.84	0.03	1.15	0.32	11.84	10.09	3.05	2.84	14.38	12.62	ns
100 µA	4 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 µA	6 mA	Std.	0.60	11.25	0.04	1.54	0.43	11.25	9.54	4.61	4.70	14.64	12.93	ns
		–1	0.51	9.57	0.04	1.31	0.36	9.57	8.11	3.92	4.00	12.46	11.00	ns
		–2	0.45	8.40	0.03	1.15	0.32	8.40	7.12	3.44	3.51	10.93	9.66	ns
100 µA	8 mA	Std.	0.60	8.63	0.04	1.54	0.43	8.63	7.39	4.96	5.28	12.02	10.79	ns
		–1	0.51	7.34	0.04	1.31	0.36	7.34	6.29	4.22	4.49	10.23	9.18	ns
		–2	0.45	6.44	0.03	1.15	0.32	6.44	5.52	3.70	3.94	8.98	8.06	ns
100 µA	16 mA	Std.	0.60	8.05	0.04	1.54	0.43	8.05	6.93	5.03	5.43	11.44	10.32	ns
		–1	0.51	6.85	0.04	1.31	0.36	6.85	5.90	4.28	4.62	9.74	8.78	ns
		–2	0.45	6.01	0.03	1.15	0.32	6.01	5.18	3.76	4.06	8.55	7.71	ns
100 µA	24 mA	Std.	0.60	7.50	0.04	1.54	0.43	7.50	6.90	5.13	6.00	10.89	10.29	ns
		–1	0.51	6.38	0.04	1.31	0.36	6.38	5.87	4.36	5.11	9.27	8.76	ns
		–2	0.45	5.60	0.03	1.15	0.32	5.60	5.15	3.83	4.48	8.13	7.69	ns

Notes:

1. *The minimum drive strength for any LVCMOS 3.3 V software configuration when run in wide range is ±100 µA. Drive strength displayed in the software is supported for normal range only. For a detailed I/V curve, refer to the IBIS models.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Timing Characteristics

Table 2-60 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.60	8.66	0.04	1.31	0.43	7.83	8.66	2.68	2.30	10.07	10.90	ns
	–1	0.51	7.37	0.04	1.11	0.36	6.66	7.37	2.28	1.96	8.56	9.27	ns
	–2	0.45	6.47	0.03	0.98	0.32	5.85	6.47	2.00	1.72	7.52	8.14	ns
6 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
8 mA	Std.	0.60	5.17	0.04	1.31	0.43	5.04	5.17	3.05	3.00	7.27	7.40	ns
	–1	0.51	4.39	0.04	1.11	0.36	4.28	4.39	2.59	2.55	6.19	6.30	ns
	–2	0.45	3.86	0.03	0.98	0.32	3.76	3.86	2.28	2.24	5.43	5.53	ns
12 mA	Std.	0.60	3.56	0.04	1.31	0.43	3.63	3.43	3.30	3.44	5.86	5.67	ns
	–1	0.51	3.03	0.04	1.11	0.36	3.08	2.92	2.81	2.92	4.99	4.82	ns
	–2	0.45	2.66	0.03	0.98	0.32	2.71	2.56	2.47	2.57	4.38	4.23	ns
16 mA	Std.	0.60	3.35	0.04	1.31	0.43	3.41	3.06	3.36	3.55	5.65	5.30	ns
	–1	0.51	2.85	0.04	1.11	0.36	2.90	2.60	2.86	3.02	4.81	4.51	ns
	–2	0.45	2.50	0.03	0.98	0.32	2.55	2.29	2.51	2.65	4.22	3.96	ns
24 mA	Std.	0.60	3.09	0.04	1.31	0.43	3.15	2.44	3.44	4.00	5.38	4.68	ns
	–1	0.51	2.63	0.04	1.11	0.36	2.68	2.08	2.92	3.40	4.58	3.98	ns
	–2	0.45	2.31	0.03	0.98	0.32	2.35	1.82	2.57	2.98	4.02	3.49	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-62 • **2.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	8.28	0.04	1.30	0.43	7.41	8.28	2.25	2.07	9.64	10.51	ns
	–1	0.56	7.04	0.04	1.10	0.36	6.30	7.04	1.92	1.76	8.20	8.94	ns
	–2	0.49	6.18	0.03	0.97	0.32	5.53	6.18	1.68	1.55	7.20	7.85	ns
6 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
8 mA	Std.	0.66	4.85	0.04	1.30	0.43	4.65	4.85	2.59	2.71	6.88	7.09	ns
	–1	0.56	4.13	0.04	1.10	0.36	3.95	4.13	2.20	2.31	5.85	6.03	ns
	–2	0.49	3.62	0.03	0.97	0.32	3.47	3.62	1.93	2.02	5.14	5.29	ns
12 mA	Std.	0.66	3.21	0.04	1.30	0.43	3.27	3.14	2.82	3.11	5.50	5.38	ns
	–1	0.56	2.73	0.04	1.10	0.36	2.78	2.67	2.40	2.65	4.68	4.57	ns
	–2	0.49	2.39	0.03	0.97	0.32	2.44	2.35	2.11	2.32	4.11	4.02	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-63 • **2.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.66	10.84	0.04	1.30	0.43	10.64	10.84	2.26	1.99	12.87	13.08	ns
	–1	0.56	9.22	0.04	1.10	0.36	9.05	9.22	1.92	1.69	10.95	11.12	ns
	–2	0.49	8.10	0.03	0.97	0.32	7.94	8.10	1.68	1.49	9.61	9.77	ns
6 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
8 mA	Std.	0.66	7.37	0.04	1.30	0.43	7.50	7.36	2.59	2.61	9.74	9.60	ns
	–1	0.56	6.27	0.04	1.10	0.36	6.38	6.26	2.20	2.22	8.29	8.16	ns
	–2	0.49	5.50	0.03	0.97	0.32	5.60	5.50	1.93	1.95	7.27	7.17	ns
12 mA	Std.	0.66	5.63	0.04	1.30	0.43	5.73	5.51	2.83	3.01	7.97	7.74	ns
	–1	0.56	4.79	0.04	1.10	0.36	4.88	4.68	2.41	2.56	6.78	6.59	ns
	–2	0.49	4.20	0.03	0.97	0.32	4.28	4.11	2.11	2.25	5.95	5.78	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Timing Characteristics

Table 2-70 • **1.8 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.7 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	11.86	0.04	1.22	0.43	9.14	11.86	2.77	1.66	11.37	14.10	ns
	–1	0.56	10.09	0.04	1.04	0.36	7.77	10.09	2.36	1.41	9.67	11.99	ns
	–2	0.49	8.86	0.03	0.91	0.32	6.82	8.86	2.07	1.24	8.49	10.53	ns
4 mA	Std.	0.66	6.91	0.04	1.22	0.43	5.86	6.91	3.22	2.84	8.10	9.15	ns
	–1	0.56	5.88	0.04	1.04	0.36	4.99	5.88	2.74	2.41	6.89	7.78	ns
	–2	0.49	5.16	0.03	0.91	0.32	4.38	5.16	2.41	2.12	6.05	6.83	ns
6 mA	Std.	0.66	4.45	0.04	1.22	0.43	4.18	4.45	3.53	3.38	6.42	6.68	ns
	–1	0.56	3.78	0.04	1.04	0.36	3.56	3.78	3.00	2.88	5.46	5.69	ns
	–2	0.49	3.32	0.03	0.91	0.32	3.12	3.32	2.64	2.53	4.79	4.99	ns
8 mA	Std.	0.66	3.92	0.04	1.22	0.43	3.93	3.92	3.60	3.52	6.16	6.16	ns
	–1	0.56	3.34	0.04	1.04	0.36	3.34	3.34	3.06	3.00	5.24	5.24	ns
	–2	0.49	2.93	0.03	0.91	0.32	2.93	2.93	2.69	2.63	4.60	4.60	ns
12 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns
16 mA	Std.	0.66	3.53	0.04	1.22	0.43	3.60	3.04	3.70	4.08	5.84	5.28	ns
	–1	0.56	3.01	0.04	1.04	0.36	3.06	2.59	3.15	3.47	4.96	4.49	ns
	–2	0.49	2.64	0.03	0.91	0.32	2.69	2.27	2.76	3.05	4.36	3.94	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-81 • **1.5 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	12.78	0.04	1.44	0.43	12.81	12.78	3.40	2.64	15.05	15.02	ns
	–1	0.56	10.87	0.04	1.22	0.36	10.90	10.87	2.89	2.25	12.80	12.78	ns
	–2	0.49	9.55	0.03	1.07	0.32	9.57	9.55	2.54	1.97	11.24	11.22	ns
4 mA	Std.	0.66	10.01	0.04	1.44	0.43	10.19	9.55	3.75	3.27	12.43	11.78	ns
	–1	0.56	8.51	0.04	1.22	0.36	8.67	8.12	3.19	2.78	10.57	10.02	ns
	–2	0.49	7.47	0.03	1.07	0.32	7.61	7.13	2.80	2.44	9.28	8.80	ns
6 mA	Std.	0.66	9.33	0.04	1.44	0.43	9.51	8.89	3.83	3.43	11.74	11.13	ns
	–1	0.56	7.94	0.04	1.22	0.36	8.09	7.56	3.26	2.92	9.99	9.47	ns
	–2	0.49	6.97	0.03	1.07	0.32	7.10	6.64	2.86	2.56	8.77	8.31	ns
8 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns
12 mA	Std.	0.66	8.91	0.04	1.44	0.43	9.07	8.89	3.95	4.05	11.31	11.13	ns
	–1	0.56	7.58	0.04	1.22	0.36	7.72	7.57	3.36	3.44	9.62	9.47	ns
	–2	0.49	6.65	0.03	1.07	0.32	6.78	6.64	2.95	3.02	8.45	8.31	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-82 • **1.5 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 1.4 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.83	0.04	1.42	0.43	6.42	7.83	2.71	2.55	8.65	10.07	ns
	–1	0.56	6.66	0.04	1.21	0.36	5.46	6.66	2.31	2.17	7.36	8.56	ns
	–2	0.49	5.85	0.03	1.06	0.32	4.79	5.85	2.02	1.90	6.46	7.52	ns
4 mA	Std.	0.66	4.84	0.04	1.42	0.43	4.49	4.84	3.03	3.13	6.72	7.08	ns
	–1	0.56	4.12	0.04	1.21	0.36	3.82	4.12	2.58	2.66	5.72	6.02	ns
	–2	0.49	3.61	0.03	1.06	0.32	3.35	3.61	2.26	2.34	5.02	5.28	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

***Table 2-86* • Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	**Min. V**	**Max. V**	**Min. V**	**Max. V**	**Max,. V**	**Min. V**	**mA**	**mA**	**Max. mA[1]**	**Max. mA[1]**	**μA[2]**	**μA[2]**
Per PCI specification	Per PCI curves										10	10

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 85°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Microsemi loadings for enable path characterization are described in Figure 2-11.

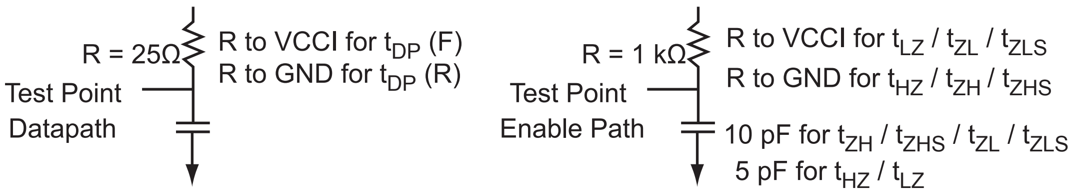

***Figure 2-11* • AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; Microsemi loading for tristate is described in Table 2-87.

***Table 2-87* • AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCI for $t_{DP(R)}$ 0.615 * VCCI for $t_{DP(F)}$	10

Note: *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.

DDR Module Specifications

Input DDR Module

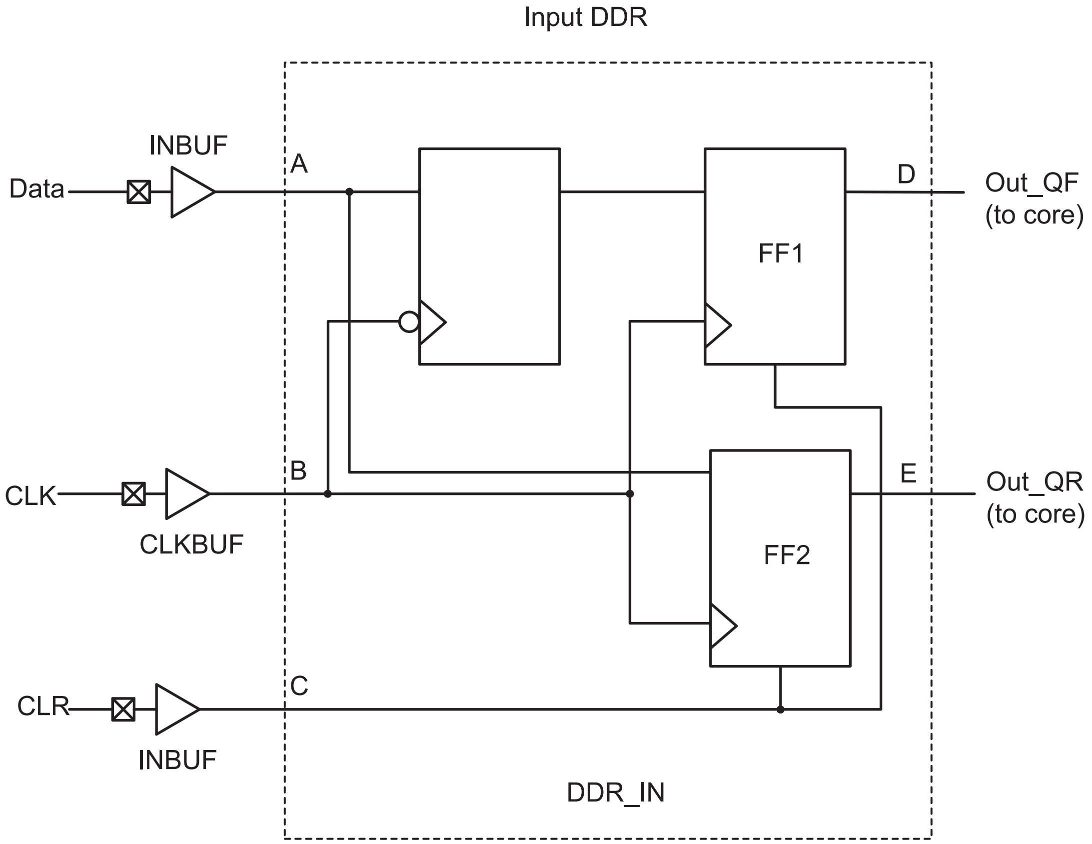

Figure 2-20 • **Input DDR Timing Model**

Table 2-101 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

Timing Characteristics

Table 2-105 • Combinatorial Cell Propagation Delays
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–2	–1	Std.	Units
INV	Y = !A	t_{PD}	0.40	0.46	0.54	ns
AND2	Y = A · B	t_{PD}	0.47	0.54	0.63	ns
NAND2	Y = !(A · B)	t_{PD}	0.47	0.54	0.63	ns
OR2	Y = A + B	t_{PD}	0.49	0.55	0.65	ns
NOR2	Y = !(A + B)	t_{PD}	0.49	0.55	0.65	ns
XOR2	Y = A ⊕ B	t_{PD}	0.74	0.84	0.99	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.70	0.79	0.93	ns
XOR3	Y = A ⊕ B ⊕ C	t_{PD}	0.87	1.00	1.17	ns
MUX2	Y = A !S + B S	t_{PD}	0.51	0.58	0.68	ns
AND3	Y = A · B · C	t_{PD}	0.56	0.64	0.75	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *Fusion, IGLOO/e, and ProASIC3/E Macro Library Guide*.

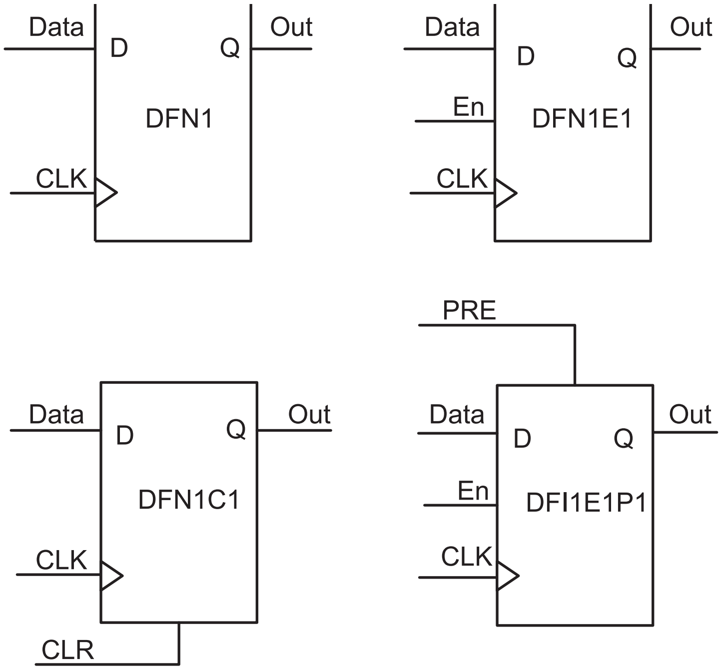

Figure 2-26 • Sample of Sequential Cells

Timing Waveforms

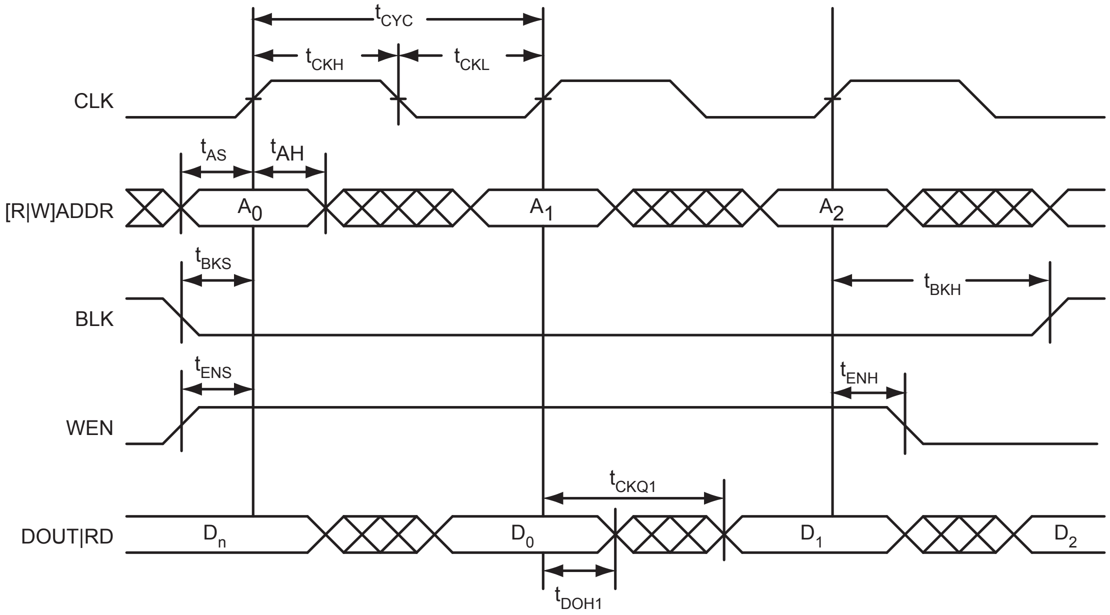

***Figure 2-31* • RAM Read for Pass-Through Output. Applicable to Both RAM4K9 and RAM512x18.**

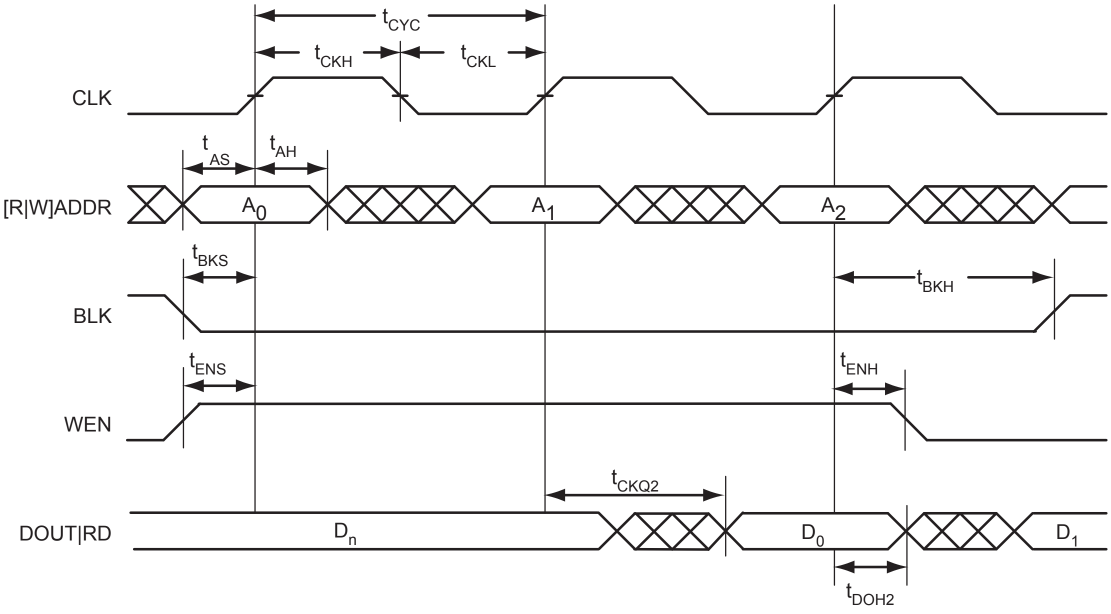

***Figure 2-32* • RAM Read for Pipelined Output. Applicable to Both RAM4K9 and RAM512x18.**

***Table 2-117* • RAM512X18**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{AS}	Address setup time	0.25	0.28	0.33	ns
t_{AH}	Address hold time	0.00	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.13	0.15	0.17	ns
t_{ENH}	REN, WEN hold time	0.10	0.11	0.13	ns
t_{DS}	Input data (WD) setup time	0.18	0.21	0.25	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained)	2.16	2.46	2.89	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.90	1.02	1.20	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—Applicable to Opening Edge	0.50	0.43	0.38	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—Applicable to Opening Edge	0.59	0.50	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to data out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.21	0.24	0.29	ns
t_{CYC}	Clock cycle time	3.23	3.68	4.32	ns
F_{MAX}	Maximum frequency	310	272	231	MHz

Notes:

1. *For more information, refer to the application note Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-120 **• A3P250 FIFO 512×8**
Worst Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	3.75	4.27	5.02	ns
t_{ENH}	REN, WEN Hold Time	0.00	0.00	0.00	ns
t_{BKS}	BLK Setup Time	0.19	0.22	0.26	ns
t_{BKH}	BLK Hold Time	0.00	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.18	0.21	0.25	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.17	2.47	2.90	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.94	1.07	1.26	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.72	1.96	2.30	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.63	1.86	2.18	ns
t_{CKAF}	Clock High to Almost Empty/Full Flag Valid	6.19	7.05	8.29	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.69	1.93	2.27	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.13	6.98	8.20	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.92	1.05	1.23	ns
	RESET Low to Data Out Low on RD (pipelined)	0.92	1.05	1.23	ns
$t_{REMRSTB}$	RESET Removal	0.29	0.33	0.38	ns
$t_{RECRSTB}$	RESET Recovery	1.50	1.71	2.01	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.21	0.24	0.29	ns
t_{CYC}	Clock Cycle Time	3.23	3.68	4.32	ns
F_{MAX}	Maximum Frequency for FIFO	310	272	231	MHz

QN68	
Pin Number	**A3P015 Function**
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132	
Pin Number	**A3P125 Function**
C17	IO83RSB1
C18	VCCIB1
C19	TCK
C20	VMV1
C21	VPUMP
C22	VJTAG
C23	VCCIB0
C24	NC
C25	NC
C26	GCA1/IO55RSB0
C27	GCC0/IO52RSB0
C28	VCCIB0
C29	IO42RSB0
C30	GNDQ
C31	GBA1/IO40RSB0
C32	GBB0/IO37RSB0
C33	VCC
C34	IO24RSB0
C35	IO19RSB0
C36	IO16RSB0
C37	IO10RSB0
C38	VCCIB0
C39	GAB1/IO03RSB0
C40	VMV0
D1	GND
D2	GND
D3	GND
D4	GND

TQ144	
Pin Number	**A3P125 Function**
1	GAA2/IO67RSB1
2	IO68RSB1
3	GAB2/IO69RSB1
4	IO132RSB1
5	GAC2/IO131RSB1
6	IO130RSB1
7	IO129RSB1
8	IO128RSB1
9	VCC
10	GND
11	VCCIB1
12	IO127RSB1
13	GFC1/IO126RSB1
14	GFC0/IO125RSB1
15	GFB1/IO124RSB1
16	GFB0/IO123RSB1
17	VCOMPLF
18	GFA0/IO122RSB1
19	VCCPLF
20	GFA1/IO121RSB1
21	GFA2/IO120RSB1
22	GFB2/IO119RSB1
23	GFC2/IO118RSB1
24	IO117RSB1
25	IO116RSB1
26	IO115RSB1
27	GND
28	VCCIB1
29	GEC1/IO112RSB1
30	GEC0/IO111RSB1
31	GEB1/IO110RSB1
32	GEB0/IO109RSB1
33	GEA1/IO108RSB1
34	GEA0/IO107RSB1
35	VMV1
36	GNDQ
37	NC
38	GEA2/IO106RSB1
39	GEB2/IO105RSB1
40	GEC2/IO104RSB1
41	IO103RSB1
42	IO102RSB1
43	IO101RSB1
44	IO100RSB1
45	VCC
46	GND
47	VCCIB1
48	IO99RSB1
49	IO97RSB1
50	IO95RSB1
51	IO93RSB1
52	IO92RSB1
53	IO90RSB1
54	IO88RSB1
55	IO86RSB1
56	IO84RSB1
57	IO83RSB1
58	IO82RSB1
59	IO81RSB1
60	IO80RSB1
61	IO79RSB1
62	VCC
63	GND
64	VCCIB1
65	GDC2/IO72RSB1
66	GDB2/IO71RSB1
67	GDA2/IO70RSB1
68	GNDQ
69	TCK
70	TDI
71	TMS
72	VMV1
73	VPUMP
74	NC
75	TDO
76	TRST
77	VJTAG
78	GDA0/IO66RSB0
79	GDB0/IO64RSB0
80	GDB1/IO63RSB0
81	VCCIB0
82	GND
83	IO60RSB0
84	GCC2/IO59RSB0
85	GCB2/IO58RSB0
86	GCA2/IO57RSB0
87	GCA0/IO56RSB0
88	GCA1/IO55RSB0
89	GCB0/IO54RSB0
90	GCB1/IO53RSB0
91	GCC0/IO52RSB0
92	GCC1/IO51RSB0
93	IO50RSB0
94	IO49RSB0
95	NC
96	NC
97	NC
98	VCCIB0
99	GND
100	VCC
101	IO47RSB0
102	GBC2/IO45RSB0
103	IO44RSB0
104	GBB2/IO43RSB0
105	IO42RSB0
106	GBA2/IO41RSB0
107	VMV0
108	GNDQ

FG256	
Pin Number	**A3P250 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO07RSB0
A6	IO10RSB0
A7	IO11RSB0
A8	IO15RSB0
A9	IO20RSB0
A10	IO25RSB0
A11	IO29RSB0
A12	IO33RSB0
A13	GBB1/IO38RSB0
A14	GBA0/IO39RSB0
A15	GBA1/IO40RSB0
A16	GND
B1	GAB2/IO117UDB3
B2	GAA2/IO118UDB3
B3	NC
B4	GAB1/IO03RSB0
B5	IO06RSB0
B6	IO09RSB0
B7	IO12RSB0
B8	IO16RSB0
B9	IO21RSB0
B10	IO26RSB0
B11	IO30RSB0
B12	GBC1/IO36RSB0
B13	GBB0/IO37RSB0
B14	NC
B15	GBA2/IO41PDB1
B16	IO41NDB1
C1	IO117VDB3
C2	IO118VDB3
C3	NC
C4	NC
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO13RSB0
C8	IO17RSB0
C9	IO22RSB0
C10	IO27RSB0
C11	IO31RSB0
C12	GBC0/IO35RSB0
C13	IO34RSB0
C14	NC
C15	IO42NPB1
C16	IO44PDB1
D1	IO114VDB3
D2	IO114UDB3
D3	GAC2/IO116UDB3
D4	NC
D5	GNDQ
D6	IO08RSB0
D7	IO14RSB0
D8	IO18RSB0
D9	IO23RSB0
D10	IO28RSB0
D11	IO32RSB0
D12	GNDQ
D13	NC
D14	GBB2/IO42PPB1
D15	NC
D16	IO44NDB1
E1	IO113PDB3
E2	NC
E3	IO116VDB3
E4	IO115UDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO19RSB0
E9	IO24RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO43PDB1
E14	IO46RSB1
E15	NC
E16	IO45PDB1
F1	IO113NDB3
F2	IO112PPB3
F3	NC
F4	IO115VDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO43NDB1
F14	NC
F15	IO47PPB1
F16	IO45NDB1
G1	IO111NDB3
G2	IO111PDB3
G3	IO112NPB3
G4	GFC1/IO110PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

Revision	Changes	Page
Revision 5 (Aug 2008) DC and Switching Characteristics v1.3	TJ, Maximum Junction Temperature, was changed to 100° from 110º in the "Thermal Characteristics" section and EQ 1. The calculated result of Maximum Power Allowed has thus changed to 1.463 W from 1.951 W.	2-6
	Values for the A3P015 device were added to Table 2-7 • Quiescent Supply Current Characteristics.	2-7
	Values for the A3P015 device were added to Table 2-14 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices. P_{AC14} was removed. Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices is new.	2-11, 2-12
	The "PLL Contribution—PPLL" section was updated to change the P_{PLL} formula from $P_{AC13} + P_{AC14} * F_{CLKOUT}$ to $P_{DC4} + P_{AC13} * F_{CLKOUT}$.	2-14
	Both fall and rise values were included for $t_{DDRISUD}$ and t_{DDRIHD} in Table 2-102 • Input DDR Propagation Delays.	2-78
	Table 2-107 • A3P015 Global Resource is new.	2-86
	The typical value for Delay Increments in Programmable Delay Blocks was changed from 160 to 200 in Table 2-115 • ProASIC3 CCC/PLL Specification.	2-90
Revision 4 (Jun 2008) DC and Switching Characteristics v1.2	Table note references were added to Table 2-2 • Recommended Operating Conditions 1, and the order of the table notes was changed.	2-2
	The title for Table 2-4 • Overshoot and Undershoot Limits 1 was modified to remove "as measured on quiet I/Os." Table note 1 was revised to remove "estimated SSO density over cycles." Table note 2 was revised to remove "refers only to overshoot/undershoot limits for simultaneous switching I/Os."	2-3
	The "Power per I/O Pin" section was updated to include 3 additional tables pertaining to input buffer power and output buffer power.	2-7
	Table 2-29 • I/O Output Buffer Maximum Resistances 1 was revised to include values for 3.3 V PCI/PCI-X.	2-27
	Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels was updated.	2-66
Revision 3 (Jun 2008) Packaging v1.3	Pin numbers were added to the "QN68 – Bottom View" package diagram. Note 2 was added below the diagram.	4-3
	The "QN132 – Bottom View" package diagram was updated to include D1 to D4. In addition, note 1 was changed from top view to bottom view, and note 2 is new.	4-6
Revision 2 (Feb 2008) Product Brief v1.0	This document was divided into two sections and given a version number, starting at v1.0. The first section of the document includes features, benefits, ordering information, and temperature and speed grade offerings. The second section is a device family overview.	N/A
	This document was updated to include A3P015 device information. QN68 is a new package that was added because it is offered in the A3P015. The following sections were updated: "Features and Benefits" "ProASIC3 Ordering Information" "Temperature Grade Offerings" "ProASIC3 Flash Family FPGAs" "A3P015 and A3P030" note Introduction and Overview (NA)	N/A

Revision	Changes	Page
v2.0 (continued)	Table 3-20 • Summary of I/O Timing Characteristics—Software Default Settings (Advanced) and Table 3-21 • Summary of I/O Timing Characteristics—Software Default Settings (Standard Plus) were updated.	3-20 to 3-20
	Table 3-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices was updated.	3-9
	Table 3-24 • I/O Output Buffer Maximum Resistances1 (Advanced) and Table 3-25 • I/O Output Buffer Maximum Resistances1 (Standard Plus) were updated.	3-22 to 3-22
	Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions was updated.	3-18
	Table 3-28 • I/O Short Currents IOSH/IOSL (Advanced) and Table 3-29 • I/O Short Currents IOSH/IOSL (Standard Plus) were updated.	3-24 to 3-26
	The note in Table 3-32 • I/O Input Rise Time, Fall Time, and Related I/O Reliability was updated.	3-27
	Figure 3-33 • Write Access After Write onto Same Address, Figure 3-34 • Read Access After Write onto Same Address, and Figure 3-35 • Write Access After Read onto Same Address are new.	3-82 to 3-84
	Figure 3-43 • Timing Diagram was updated.	3-96
	Ambient was deleted from the "Speed Grade and Temperature Grade Matrix".	iv
	Notes were added to the package diagrams identifying if they were top or bottom view.	N/A
	The A3P030 "132-Pin QFN" table is new.	4-2
	The A3P060 "132-Pin QFN" table is new.	4-4
	The A3P125 "132-Pin QFN" table is new.	4-6
	The A3P250 "132-Pin QFN" table is new.	4-8
	The A3P030 "100-Pin VQFP" table is new.	4-11
Advance v0.7 (January 2007)	In the "I/Os Per Package" table, the I/O numbers were added for A3P060, A3P125, and A3P250. The A3P030-VQ100 I/O was changed from 79 to 77.	ii
Advance v0.6 (April 2006)	The term flow-through was changed to pass-through.	N/A
	Table 1 was updated to include the QN132.	ii
	The "I/Os Per Package" table was updated with the QN132. The footnotes were also updated. The A3P400-FG144 I/O count was updated.	ii
	"Automotive ProASIC3 Ordering Information" was updated with the QN132.	iii
	"Temperature Grade Offerings" was updated with the QN132.	iii
	B-LVDS and M-LDVS are new I/O standards added to the datasheet.	N/A
	The term flow-through was changed to pass-through.	N/A
	Figure 2-7 • Efficient Long-Line Resources was updated.	2-7
	The footnotes in Figure 2-15 • Clock Input Sources Including CLKBUF, CLKBUF_LVDS/LVPECL, and CLKINT were updated.	2-16
	The Delay Increments in the Programmable Delay Blocks specification in Figure 2-24 • ProASIC3E CCC Options.	2-24
	The "SRAM and FIFO" section was updated.	2-21