Microchip Technology - M7A3P1000-2PQ208 Datasheet

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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications,

Details	
Product Status	Obsolete
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	154
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	208-BFQFP
Supplier Device Package	208-PQFP (28x28)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-2pq208

1 – ProASIC3 Device Family Overview

General Description

ProASIC3, the third-generation family of Microsemi flash FPGAs, offers performance, density, and features beyond those of the ProASIC$^{PLUS®}$ family. Nonvolatile flash technology gives ProASIC3 devices the advantage of being a secure, low power, single-chip solution that is Instant On. ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). The A3P015 and A3P030 devices have no PLL or RAM support. ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of true dual-port SRAM and up to 300 user I/Os.

ProASIC3 devices support the ARM Cortex-M1 processor. The ARM-enabled devices have Microsemi ordering numbers that begin with M1A3P (Cortex-M1) and do not support AES decryption.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based ProASIC3 devices allow all functionality to be Instant On; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system reprogramming to support future design iterations and field upgrades with confidence that valuable intellectual property (IP) cannot be compromised or copied. Secure ISP can be performed using the industry-standard AES algorithm. The ProASIC3 family device architecture mitigates the need for ASIC migration at higher user volumes. This makes the ProASIC3 family a cost-effective ASIC replacement solution, especially for applications in the consumer, networking/ communications, computing, and avionics markets.

Security

The nonvolatile, flash-based ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to provide the highest level of protection in the FPGA industry for intellectual property and configuration data. In addition, all FlashROM data in ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES standard was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. ProASIC3 devices with AES-based security provide a high level of protection for remote field updates over public networks such as the Internet, and are designed to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves.

ARM-enabled ProASIC3 devices do not support user-controlled AES security mechanisms. Since the ARM core must be protected at all times, AES encryption is always on for the core logic, so bitstreams are always encrypted. There is no user access to encryption for the FlashROM programming data.

Security, built into the FPGA fabric, is an inherent component of the ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. The ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks.

Table 2-9 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard Plus I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-10 • **Summary of I/O Input Buffer Power (Per Pin) – Default I/O Software Settings Applicable to Standard I/O Banks**

	VMV (V)	Static Power PDC2 (mW) [1]	Dynamic Power PAC9 (µW/MHz) [2]
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.24
3.3 V LVCMOS Wide Range[3]	3.3	–	17.24
2.5 V LVCMOS	2.5	–	5.19
1.8 V LVCMOS	1.8	–	2.18
1.5 V LVCMOS (JESD8-11)	1.5	–	1.52

Notes:

1. *PDC2 is the static power (where applicable) measured on VMV.*
2. *PAC9 is the total dynamic power measured on VCC and VMV.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-11 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings[1] Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	468.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *PDC3 is the static power (where applicable) measured on VCCI.*
3. *PAC10 is the total dynamic power measured on VCC and VCCI.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Table 2-12 • Summary of I/O Output Buffer Power (Per Pin) – Default I/O Software Settings[1] Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	VCCI (V)	Static Power PDC3 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	452.67
3.3 V LVCMOS Wide Range[4]	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. *Dynamic power consumption is given for standard load and software default drive strength and output slew.*
2. *P_{DC3} is the static power (where applicable) measured on VMV.*
3. *P_{AC10} is the total dynamic power measured on VCC and VMV.*
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD8-B specification.*

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-18 • **Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings Applicable to Advanced I/O Banks**

I/O Standard	Drive Strength	Equiv. Software Default Drive Strength Option[2]	Slew Rate	VIL		VIH		VOL	VOH	IOL[1] mA	IOH[1] mA
				Min V	Max V	Min V	Max V	Max V	Min V		
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
3.3 V LVCMOS Wide Range[3]	100 µA	12 mA	High	–0.3	0.8	2	3.6	0.2	VCCI – 0.2	0.1	0.1
2.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.7	1.7	2.7	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12
1.5 V LVCMOS	12 mA	12 mA	High	–0.3	0.35 * VCCI	0.65 * VCCI	1.6	0.25 * VCCI	0.75 * VCCI	12	12
3.3 V PCI	Per PCI specifications										
3.3 V PCI-X	Per PCI-X specifications										

Notes:

1. *Currents are measured at 85°C junction temperature.*
2. *3.3 V LVCMOS wide range is applicable to 100 µA drive strength only. The configuration will NOT operate at the equivalent software default drive strength. These values are for Normal Ranges ONLY.*
3. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-43 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	–1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	–2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
4 mA	Std.	0.66	7.20	0.04	1.00	0.43	7.34	6.29	2.27	2.34	9.57	8.52	ns
	–1	0.56	6.13	0.04	0.85	0.36	6.24	5.35	1.93	1.99	8.14	7.25	ns
	–2	0.49	5.38	0.03	0.75	0.32	5.48	4.69	1.70	1.75	7.15	6.36	ns
6 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	–1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	–2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
8 mA	Std.	0.66	4.50	0.04	1.00	0.43	4.58	3.82	2.58	2.88	6.82	6.05	ns
	–1	0.56	3.83	0.04	0.85	0.36	3.90	3.25	2.19	2.45	5.80	5.15	ns
	–2	0.49	3.36	0.03	0.75	0.32	3.42	2.85	1.92	2.15	5.09	4.52	ns
12 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	–1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	–2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns
16 mA	Std.	0.66	3.16	0.04	1.00	0.43	3.22	2.58	2.79	3.22	5.45	4.82	ns
	–1	0.56	2.69	0.04	0.85	0.36	2.74	2.20	2.37	2.74	4.64	4.10	ns
	–2	0.49	2.36	0.03	0.75	0.32	2.40	1.93	2.08	2.41	4.07	3.60	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-44 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
4 mA	Std.	0.66	9.68	0.04	1.00	0.43	9.86	8.42	2.28	2.21	12.09	10.66	ns
	–1	0.56	8.23	0.04	0.85	0.36	8.39	7.17	1.94	1.88	10.29	9.07	ns
	–2	0.49	7.23	0.03	0.75	0.32	7.36	6.29	1.70	1.65	9.03	7.96	ns
6 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
8 mA	Std.	0.66	6.70	0.04	1.00	0.43	6.82	5.89	2.58	2.74	9.06	8.12	ns
	–1	0.56	5.70	0.04	0.85	0.36	5.80	5.01	2.20	2.33	7.71	6.91	ns
	–2	0.49	5.00	0.03	0.75	0.32	5.10	4.40	1.93	2.05	6.76	6.06	ns
12 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns
16 mA	Std.	0.66	5.05	0.04	1.00	0.43	5.14	4.51	2.79	3.08	7.38	6.75	ns
	–1	0.56	4.29	0.04	0.85	0.36	4.37	3.84	2.38	2.62	6.28	5.74	ns
	–2	0.49	3.77	0.03	0.75	0.32	3.84	3.37	2.09	2.30	5.51	5.04	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-45 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
4 mA	Std.	0.66	7.07	0.04	1.00	0.43	7.20	6.23	2.07	2.15	ns
	–1	0.56	6.01	0.04	0.85	0.36	6.12	5.30	1.76	1.83	ns
	–2	0.49	5.28	0.03	0.75	0.32	5.37	4.65	1.55	1.60	ns
6 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns
	–2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns
8 mA	Std.	0.66	4.41	0.04	1.00	0.43	4.49	3.75	2.39	2.69	ns
	–1	0.56	3.75	0.04	0.85	0.36	3.82	3.19	2.04	2.29	ns

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-56 • Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL1	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	10	10
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-57 • Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	10	10
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	10	10
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	10	10
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	10	10
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-66 • **Minimum and Maximum DC Input and Output Levels Applicable to Advanced I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min V**	**Max V**	**Min V**	**Max V**	**Max V**	**Min V**	**mA**	**mA**	**Max mA[3]**	**Max mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	8	8	51	45	10	10
12 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	12	12	74	91	10	10
16 mA	–0.3	0.35 * VCCI	0.65 * VCCI	1.9	0.45	VCCI – 0.45	16	16	74	91	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-67 • **Minimum and Maximum DC Input and Output Levels Applicable to Standard Plus I/O I/O Banks**

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	**Min V**	**Max V**	**Min V**	**Max V**	**Max V**	**Min V**	**mA**	**mA**	**Max mA[3]**	**Max mA[3]**	**µA[4]**	**µA[4]**
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	11	9	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	22	17	10	10
6 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	6	6	44	35	10	10
8 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	8	8	44	35	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <V CCI. Input current is larger when operating outside recommended ranges*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

Table 2-68 • Minimum and Maximum DC Input and Output Levels Applicable to Standard I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL[1]	IIH[2]
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[3]	Max. mA[3]	µA[4]	µA[4]
2 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	2	2	9	11	10	10
4 mA	–0.3	0.35 * VCCI	0.65 * VCCI	3.6	0.45	VCCI – 0.45	4	4	17	22	10	10

Notes:

1. *IIL is the input leakage current per I/O pin over recommended operation conditions where –0.3 V < VIN < VIL.*
2. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN < VCCI. Input current is larger when operating outside recommended ranges.*
3. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
4. *Currents are measured at 85°C junction temperature.*
5. *Software default selection highlighted in gray.*

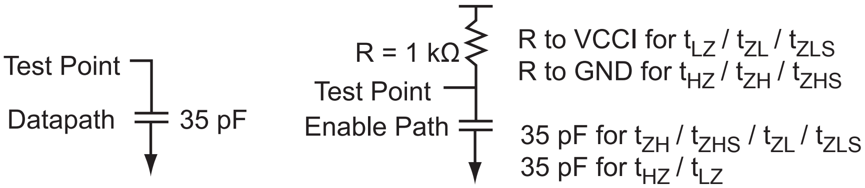

Figure 2-9 • AC Loading

Table 2-69 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.8	0.9	35

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-22 for a complete table of trip points.*

Table 2-90 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCI	Supply Voltage	2.375	2.5	2.625	V
VOL	Output Low Voltage	0.9	1.075	1.25	V
VOH	Output High Voltage	1.25	1.425	1.6	V
IOL [1]	Output Lower Current	0.65	0.91	1.16	mA
IOH [1]	Output High Current	0.65	0.91	1.16	mA
VI	Input Voltage	0		2.925	V
IIH [2,3]	Input High Leakage Current			10	µA
IIL [2,4]	Input Low Leakage Current			10	µA
VODIFF	Differential Output Voltage	250	350	450	mV
VOCM	Output Common Mode Voltage	1.125	1.25	1.375	V
VICM	Input Common Mode Voltage	0.05	1.25	2.35	V
VIDIFF	Input Differential Voltage	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(Resistor Network)*
2. *Currents are measured at 85°C junction temperature.*
3. *IIH is the input leakage current per I/O pin over recommended operating conditions VIH < VIN <VCCI. Input current is larger when operating outside recommended ranges.*
4. *IIL is the input leakage current per I/O pin over recommended operation conditions where -0.3 V < VIN <VIL.*

Table 2-91 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.075	1.325	Cross point

Note: *Measuring point = $V_{trip.}$ See Table 2-22 on page 2-22 for a complete table of trip points.

Timing Characteristics

Table 2-92 • LVDS
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 2.3 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.83	0.04	1.60	ns
–1	0.56	1.56	0.04	1.36	ns
–2	0.49	1.37	0.03	1.20	ns

Note: *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

DDR Module Specifications

Input DDR Module

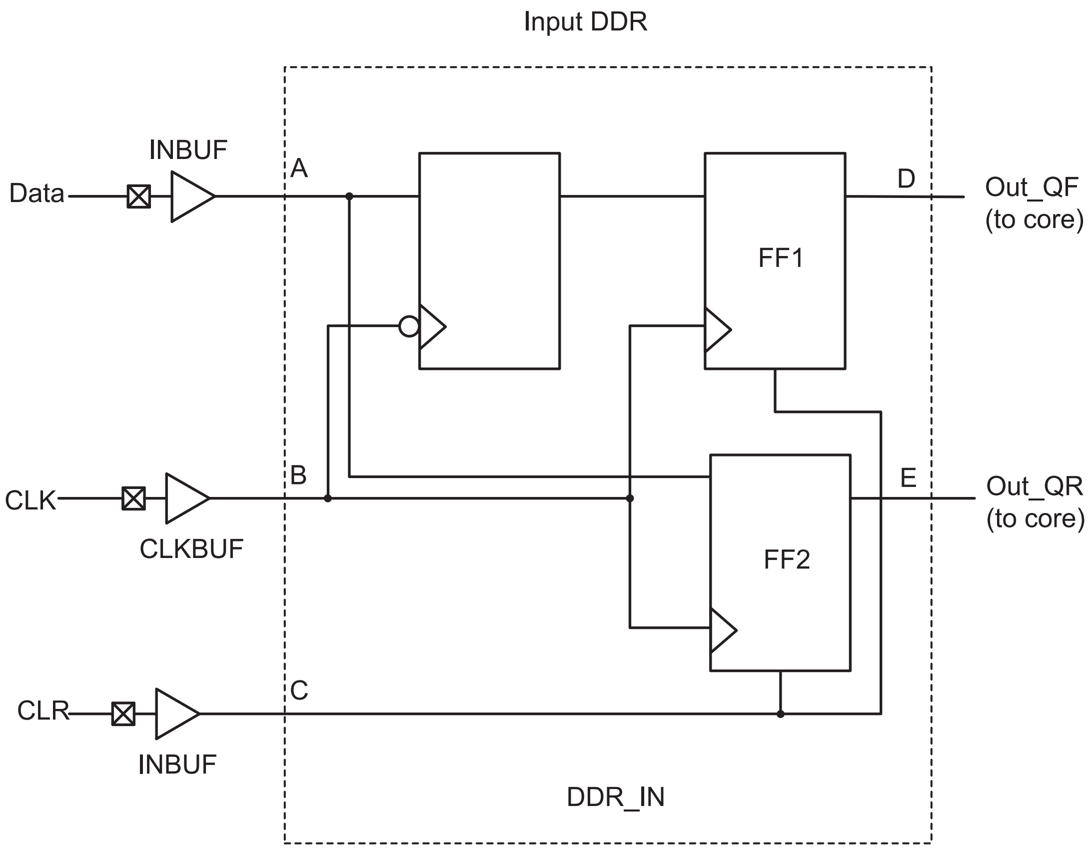

Figure 2-20 • **Input DDR Timing Model**

Table 2-101 • **Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

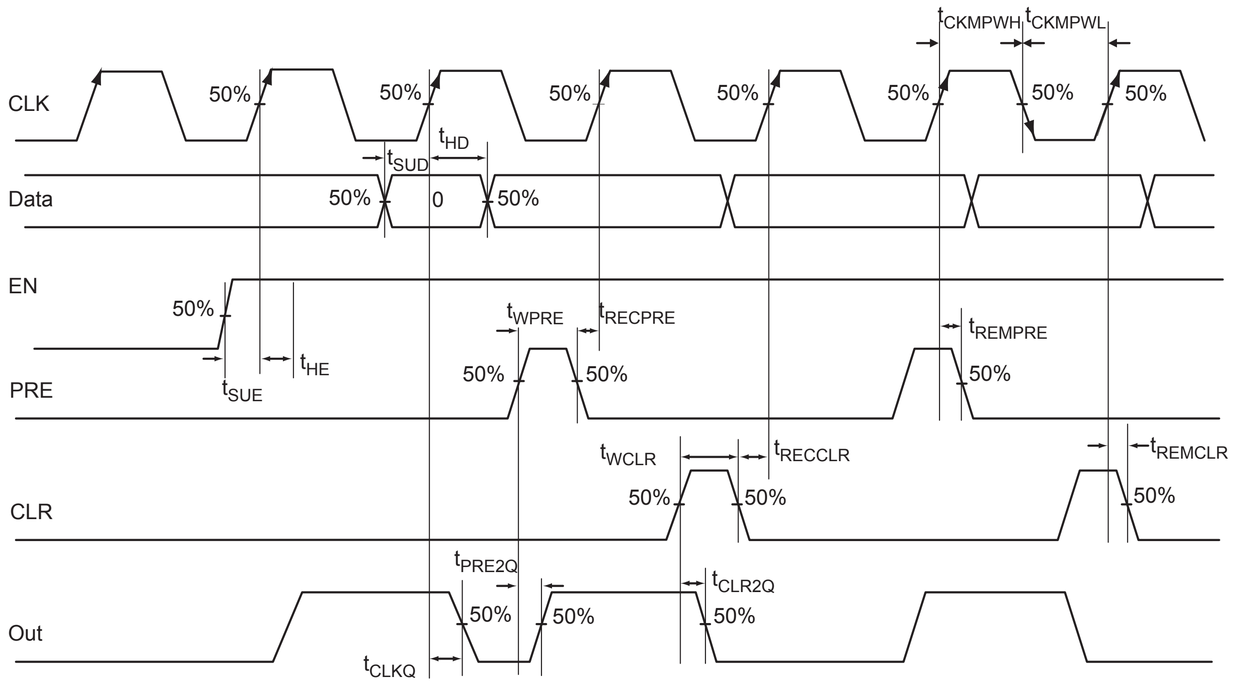

Figure 2-27 • **Timing Model and Waveforms**

Timing Characteristics

Table 2-106 • **Register Delays**
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V

Parameter	Description	–2	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.55	0.63	0.74	ns
t_{SUD}	Data Setup Time for the Core Register	0.43	0.49	0.57	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.45	0.52	0.61	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.40	0.45	0.53	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.22	0.25	0.30	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.37	0.43	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.41	0.48	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

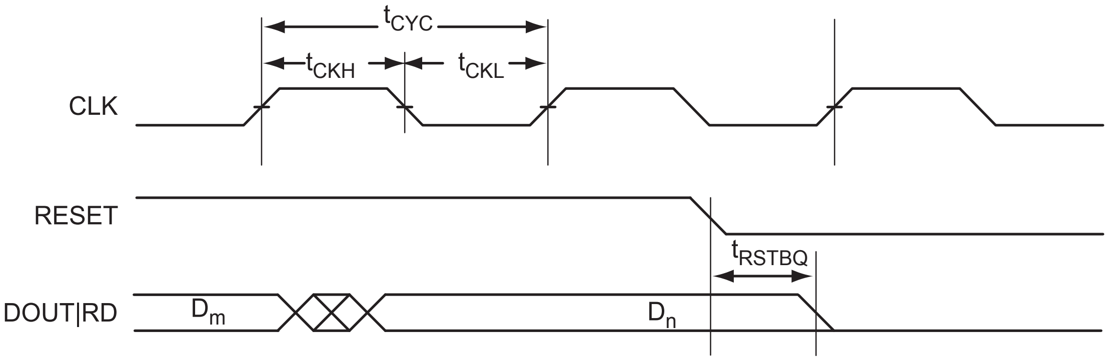

***Figure 2-35* • RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

PQ208	
Pin Number	**A3P250 Function**
1	GND
2	GAA2/IO118UDB3
3	IO118VDB3
4	GAB2/IO117UDB3
5	IO117VDB3
6	GAC2/IO116UDB3
7	IO116VDB3
8	IO115UDB3
9	IO115VDB3
10	IO114UDB3
11	IO114VDB3
12	IO113PDB3
13	IO113NDB3
14	IO112PDB3
15	IO112NDB3
16	VCC
17	GND
18	VCCIB3
19	IO111PDB3
20	IO111NDB3
21	GFC1/IO110PDB3
22	GFC0/IO110NDB3
23	GFB1/IO109PDB3
24	GFB0/IO109NDB3
25	VCOMPLF
26	GFA0/IO108NPB3
27	VCCPLF
28	GFA1/IO108PPB3
29	GND
30	GFA2/IO107PDB3
31	IO107NDB3
32	GFB2/IO106PDB3
33	IO106NDB3
34	GFC2/IO105PDB3
35	IO105NDB3
36	NC
37	IO104PDB3
38	IO104NDB3
39	IO103PSB3
40	VCCIB3
41	GND
42	IO101PDB3
43	IO101NDB3
44	GEC1/IO100PDB3
45	GEC0/IO100NDB3
46	GEB1/IO99PDB3
47	GEB0/IO99NDB3
48	GEA1/IO98PDB3
49	GEA0/IO98NDB3
50	VMV3
51	GNDQ
52	GND
53	NC
54	NC
55	GEA2/IO97RSB2
56	GEB2/IO96RSB2
57	GEC2/IO95RSB2
58	IO94RSB2
59	IO93RSB2
60	IO92RSB2
61	IO91RSB2
62	VCCIB2
63	IO90RSB2
64	IO89RSB2
65	GND
66	IO88RSB2
67	IO87RSB2
68	IO86RSB2
69	IO85RSB2
70	IO84RSB2
71	VCC
72	VCCIB2
73	IO83RSB2
74	IO82RSB2
75	IO81RSB2
76	IO80RSB2
77	IO79RSB2
78	IO78RSB2
79	IO77RSB2
80	IO76RSB2
81	GND
82	IO75RSB2
83	IO74RSB2
84	IO73RSB2
85	IO72RSB2
86	IO71RSB2
87	IO70RSB2
88	VCC
89	VCCIB2
90	IO69RSB2
91	IO68RSB2
92	IO67RSB2
93	IO66RSB2
94	IO65RSB2
95	IO64RSB2
96	GDC2/IO63RSB2
97	GND
98	GDB2/IO62RSB2
99	GDA2/IO61RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

FG144	
Pin Number	**A3P060 Function**
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	VCCIB1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	VJTAG
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	VCCIB1
M11	VPUMP
M12	GNDQ

FG256	
Pin Number	**A3P1000 Function**
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO16RSB0
A6	IO22RSB0
A7	IO28RSB0
A8	IO35RSB0
A9	IO45RSB0
A10	IO50RSB0
A11	IO55RSB0
A12	IO61RSB0
A13	GBB1/IO75RSB0
A14	GBA0/IO76RSB0
A15	GBA1/IO77RSB0
A16	GND
B1	GAB2/IO224PDB3
B2	GAA2/IO225PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO17RSB0
B6	IO21RSB0
B7	IO27RSB0
B8	IO34RSB0
B9	IO44RSB0
B10	IO51RSB0
B11	IO57RSB0
B12	GBC1/IO73RSB0
B13	GBB0/IO74RSB0
B14	IO71RSB0
B15	GBA2/IO78PDB1
B16	IO81PDB1
C1	IO224NDB3
C2	IO225NDB3
C3	VMV3
C4	IO11RSB0
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO25RSB0
C8	IO36RSB0
C9	IO42RSB0
C10	IO49RSB0
C11	IO56RSB0
C12	GBC0/IO72RSB0
C13	IO62RSB0
C14	VMV0
C15	IO78NDB1
C16	IO81NDB1
D1	IO222NDB3
D2	IO222PDB3
D3	GAC2/IO223PDB3
D4	IO223NDB3
D5	GNDQ
D6	IO23RSB0
D7	IO29RSB0
D8	IO33RSB0
D9	IO46RSB0
D10	IO52RSB0
D11	IO60RSB0
D12	GNDQ
D13	IO80NDB1
D14	GBB2/IO79PDB1
D15	IO79NDB1
D16	IO82NSB1
E1	IO217PDB3
E2	IO218PDB3
E3	IO221NDB3
E4	IO221PDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO38RSB0
E9	IO47RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO80PDB1
E14	IO83PPB1
E15	IO86PPB1
E16	IO87PDB1
F1	IO217NDB3
F2	IO218NDB3
F3	IO216PDB3
F4	IO216NDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO83NPB1
F14	IO86NPB1
F15	IO90PPB1
F16	IO87NDB1
G1	IO210PSB3
G2	IO213NDB3
G3	IO213PDB3
G4	GFC1/IO209PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1
G13	GCC1/IO91PPB1
G14	IO90NPB1
G15	IO88PDB1
G16	IO88NDB1
H1	GFB0/IO208NPB3
H2	GFA0/IO207NDB3

FG484	
Pin Number	**A3P600 Function**
A1	GND
A2	GND
A3	VCCIB0
A4	NC
A5	NC
A6	IO09RSB0
A7	IO15RSB0
A8	NC
A9	NC
A10	IO22RSB0
A11	IO23RSB0
A12	IO29RSB0
A13	IO35RSB0
A14	NC
A15	NC
A16	IO46RSB0
A17	IO48RSB0
A18	NC
A19	NC
A20	VCCIB0
A21	GND
A22	GND
B1	GND
B2	VCCIB3
B3	NC
B4	NC
B5	NC
B6	IO08RSB0
B7	IO12RSB0
B8	NC
B9	NC
B10	IO17RSB0
B11	NC
B12	NC
B13	IO36RSB0
B14	NC
B15	NC
B16	IO47RSB0
B17	IO49RSB0
B18	NC
B19	NC
B20	NC
B21	VCCIB1
B22	GND
C1	VCCIB3
C2	NC
C3	NC
C4	NC
C5	GND
C6	NC
C7	NC
C8	VCC
C9	VCC
C10	NC
C11	NC
C12	NC
C13	NC
C14	VCC
C15	VCC
C16	NC
C17	NC
C18	GND
C19	NC
C20	NC
C21	NC
C22	VCCIB1
D1	NC
D2	NC
D3	NC
D4	GND
D5	GAA0/IO00RSB0
D6	GAA1/IO01RSB0
D7	GAB0/IO02RSB0
D8	IO11RSB0
D9	IO16RSB0
D10	IO18RSB0
D11	IO28RSB0
D12	IO34RSB0
D13	IO37RSB0
D14	IO41RSB0
D15	IO43RSB0
D16	GBB1/IO57RSB0
D17	GBA0/IO58RSB0
D18	GBA1/IO59RSB0
D19	GND
D20	NC
D21	NC
D22	NC
E1	NC
E2	NC
E3	GND
E4	GAB2/IO173PDB3
E5	GAA2/IO174PDB3
E6	GNDQ
E7	GAB1/IO03RSB0
E8	IO13RSB0
E9	IO14RSB0
E10	IO21RSB0
E11	IO27RSB0
E12	IO32RSB0
E13	IO38RSB0
E14	IO42RSB0
E15	GBC1/IO55RSB0
E16	GBB0/IO56RSB0
E17	IO52RSB0
E18	GBA2/IO60PDB1
E19	IO60NDB1
E20	GND

Revision	Changes	Page
Revision 11 (March 2012)	Note indicating that A3P015 is not recommended for new designs has been added. The "Devices Not Recommended For New Designs" section is new (SAR 36760).	I to IV
	The following sentence was removed from the Advanced Architecture section: "In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of IGLOO devices via an IEEE 1532 JTAG interface" (SAR 34687).	NA
	The reference to guidelines for global spines and VersaTile rows, given in the "Global Clock Contribution—PCLOCK" section, was corrected to the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide* (SAR 34734).	2-12
	Figure 2-4 • Input Buffer Timing Model and Delays (Example) has been modified for the DIN waveform; the Rise and Fall time label has been changed to tDIN (35430).	2-16
	The AC Loading figures in the "Single-Ended I/O Characteristics" section were updated to match tables in the "Summary of I/O Timing Characteristics – Default I/O Software Settings" section (SAR 34883).	2-32
	Added values for minimum pulse width and removed the FRMAX row from Table 2-107 through Table 2-114 in the "Global Tree Timing Characteristics" section. Use the software to determine the FRMAX for the device you are using (SARs 37279, 29269).	2-85

Revision	Changes	Page
Revision 9 (Oct 2009) Product Brief v1.3	The CS121 package was added to table under "Features and Benefits" section, the "I/Os Per Package 1" table, Table 1 • ProASIC3 FPGAs Package Sizes Dimensions, "ProASIC3 Ordering Information", and the "Temperature Grade Offerings" table.	I – IV
	"ProASIC3 Ordering Information" was revised to include the fact that some RoHS compliant packages are halogen-free.	IV
Packaging v1.5	The "CS121 – Bottom View" figure and pin table for A3P060 are new.	4-15
Revision 8 (Aug 2009) Product Brief v1.2	All references to M7 devices (CoreMP7) and speed grade –F were removed from this document.	N/A
	Table 1-1 I/O Standards supported is new.	1-7
	The I/Os with Advanced I/O Standards section was revised to add definitions of hot-swap and cold-sparing.	1-7
DC and Switching Characteristics v1.4	3.3 V LVCMOS and 1.2 V LVCMOS Wide Range support was added to the datasheet. This affects all tables that contained 3.3 V LVCMOS and 1.2 V LVCMOS data.	N/A
	I_{IL} and I_{IH} input leakage current information was added to all "Minimum and Maximum DC Input and Output Levels" tables.	N/A
	–F was removed from the datasheet. The speed grade is no longer supported.	N/A
	The notes in Table 2-2 • Recommended Operating Conditions 1 were updated.	2-2
	Table 2-4 • Overshoot and Undershoot Limits 1 was updated.	2-3
	Table 2-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	2-6
	In Table 2-116 • RAM4K9, the following specifications were removed: t_{WRO} t_{CCKH}	2-96
	In Table 2-117 • RAM512X18, the following specifications were removed: t_{WRO} t_{CCKH}	2-97
	In the title of Table 2-74 • 1.8 V LVCMOS High Slew, VCCI had a typo. It was changed from 3.0 V to 1.7 V.	2-58
Revision 7 (Feb 2009) Product Brief v1.1	The "Advanced I/O" section was revised to add a bullet regarding wide range power supply voltage support.	I
	The table under "Features and Benefits" section, was updated to include a value for typical equivalent macrocells for A3P250.	I
	The QN48 package was added to the following tables: the table under "Features and Benefits" section, "I/Os Per Package 1" "ProASIC3 FPGAs Package Sizes Dimensions", and "Temperature Grade Offerings". The number of singled-ended I/Os for QN68 was added to the "I/Os Per Package 1" table.	N/A
	The Wide Range I/O Support section is new.	1-7
Revision 6 (Dec 2008) Packaging v1.4	The "QN48 – Bottom View" section is new.	4-1
	The "QN68" pin table for A3P030 is new.	4-5

Revision	Changes	Page
Advance v0.6 (continued)	The "RESET" section was updated.	2-25
	The "WCLK and RCLK" section was updated.	2-25
	The "RESET" section was updated.	2-25
	The "RESET" section was updated.	2-27
	The "Introduction" of the "Advanced I/Os" section was updated.	2-28
	The "I/O Banks" section is new. This section explains the following types of I/Os: Advanced Standard+ Standard Table 2-12 • Automotive ProASIC3 Bank Types Definition and Differences is new. This table describes the standards listed above.	2-29
	PCI-X 3.3 V was added to the Compatible Standards for 3.3 V in Table 2-11 • VCCI Voltages and Compatible Standards	2-29
	Table 2-13 • ProASIC3 I/O Features was updated.	2-30
	The "Double Data Rate (DDR) Support" section was updated to include information concerning implementation of the feature.	2-32
	The "Electrostatic Discharge (ESD) Protection" section was updated to include testing information.	2-35
	Level 3 and 4 descriptions were updated in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices.	2-64
	The notes in Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices were updated.	2-64
	The "Simultaneous Switching Outputs (SSOs) and Printed Circuit Board Layout" section is new.	2-41
	A footnote was added to Table 2-14 • Maximum I/O Frequency for Single-Ended and Differential I/Os in All Banks in Automotive ProASIC3 Devices (maximum drive strength and high slew selected).	2-30
	Table 2-18 • Automotive ProASIC3 I/O Attributes vs. I/O Standard Applications	2-45
	Table 2-50 • ProASIC3 Output Drive (OUT_DRIVE) for Standard I/O Bank Type (A3P030 device)	2-83
	Table 2-51 • ProASIC3 Output Drive for Standard+ I/O Bank Type was updated.	2-84
	Table 2-54 • ProASIC3 Output Drive for Advanced I/O Bank Type was updated.	2-84
	The "x" was updated in the "User I/O Naming Convention" section.	2-48
	The "VCC Core Supply Voltage" pin description was updated.	2-50
	The "VMVx I/O Supply Voltage (quiet)" pin description was updated to include information concerning leaving the pin unconnected.	2-50
	The "VJTAG JTAG Supply Voltage" pin description was updated.	2-50
	The "VPUMP Programming Supply Voltage" pin description was updated to include information on what happens when the pin is tied to ground.	2-50
	The "I/O User Input/Output" pin description was updated to include information on what happens when the pin is unused.	2-50
	The "JTAG Pins" section was updated to include information on what happens when the pin is unused.	2-51