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Understanding Embedded - FPGAs (Field Programmable Gate Array)

Embedded - FPGAs, or Field Programmable Gate Arrays, are advanced integrated circuits that offer unparalleled flexibility and performance for digital systems. Unlike traditional fixed-function logic devices, FPGAs can be programmed and reprogrammed to execute a wide array of logical operations, enabling customized functionality tailored to specific applications. This reprogrammability allows developers to iterate designs quickly and implement complex functions without the need for custom hardware.

Applications of Embedded - FPGAs

The versatility of Embedded - FPGAs makes them indispensable in numerous fields. In telecommunications.

Details	
Product Status	Active
Number of LABs/CLBs	-
Number of Logic Elements/Cells	-
Total RAM Bits	147456
Number of I/O	300
Number of Gates	1000000
Voltage - Supply	1.425V ~ 1.575V
Mounting Type	Surface Mount
Operating Temperature	0°C ~ 85°C (TJ)
Package / Case	484-BGA
Supplier Device Package	484-FPBGA (23x23)
Purchase URL	https://www.e-xfl.com/product-detail/microchip-technology/m7a3p1000-fgg484

I/Os with Advanced I/O Standards

The ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported (Table 1-1).

Table 1-1 • **I/O Standards Supported**

I/O Bank Type	Device and Bank Location	I/O Standards Supported		
		LVTTL/ LVCMOS	PCI/PCI-X	LVPECL, LVDS, B-LVDS, M-LVDS
Advanced	East and west Banks of A3P250 and larger devices	✓	✓	✓
Standard Plus	North and south banks of A3P250 and larger devices All banks of A3P060 and A3P125	✓	✓	Not supported
Standard	All banks of A3P015 and A3P030	✓	Not supported	Not supported

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

ProASIC3 banks for the A3P250 device and above support LVPECL, LVDS, B-LVDS and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Hot-swap (also called hot-plug, or hot-insertion) is the operation of hot-insertion or hot-removal of a card in a powered-up system.

Cold-sparing (also called cold-swap) refers to the ability of a device to leave system data undisturbed when the system is powered up, while the component itself is powered down, or when power supplies are floating.

Wide Range I/O Support

ProASIC3 devices support JEDEC-defined wide range I/O operation. ProASIC3 supports the JESD8-B specification, covering both 3 V and 3.3 V supplies, for an effective operating range of 2.7 V to 3.6 V.

Wider I/O range means designers can eliminate power supplies or power conditioning components from the board or move to less costly components with greater tolerances. Wide range eases I/O bank management and provides enhanced protection from system voltage spikes, while providing the flexibility to easily run custom voltage applications.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-4 on page 1-8).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges.

In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-5.

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCI are above the minimum specified trip points (Figure 2-2 on page 2-5).
2. VCCI > VCC – 0.75 V (typical)
3. Chip is in the operating mode.

VCCI Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCI ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCI.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

Microsemi recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLX exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-5 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation.

Thermal Characteristics

Introduction

The temperature variable in the Microsemi Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ can be used to calculate junction temperature.

T_J = Junction Temperature = $\Delta T + T_A$

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-5 on page 2-6.

P = Power dissipation

Table 2-15 • Different Components Contributing to the Static Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Static Power (mW)							
		A3P1000	A3P600	A3P400	A3P250	A3P125	A3P060	A3P030	A3P015
PDC1	Array static power in Active mode	See Table 2-7 on page 2-7.							
PDC2	I/O input pin static power (standard-dependent)	See Table 2-8 on page 2-7 through Table 2-10 on page 2-8.							
PDC3	I/O output pin static power (standard-dependent)	See Table 2-11 on page 2-9 through Table 2-13 on page 2-10.							
PDC4	Static PLL contribution	2.55 mW							
PDC5	Bank quiescent power (VCCI-dependent)	See Table 2-7 on page 2-7.							

*Note: *For a different output load, drive strength, or slew rate, Microsemi recommends using the Microsemi Power spreadsheet calculator or SmartPower tool in Libero SoC software.*

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-16 on page 2-14.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-17 on page 2-14.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-17 on page 2-14. The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

$P_{STAT} = P_{DC1} + N_{INPUTS}* P_{DC2} + N_{OUTPUTS}* P_{DC3}$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption—P_{DYN}

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$

Global Clock Contribution—P_{CLOCK}

$P_{CLOCK} = (P_{AC1} + N_{SPINE}*P_{AC2} + N_{ROW}*P_{AC3} + N_{S\text{-}CELL}* P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Spine Architecture" section of the Global Resources chapter in the *ProASIC3 FPGA Fabric User's Guide*.

Table 2-30 • I/O Output Buffer Maximum Resistances[1]
Applicable to Standard I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
3.3 V LVCMOS Wide Range[4]	100 µA	Same as regular 3.3 V LVCMOS	Same as regular 3.3 V LVCMOS
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCI, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)}$ = (VOLspec) / IOLspec
3. $R_{(PULL\text{-}UP\text{-}MAX)}$ = (VCCImax – VOHspec) / IOHspec
4. *All LVCMOS 3.3 V software macros support LVCMOS 3.3 V wide range as specified in the JESD-8B specification.*

Table 2-31 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

	$R_{(WEAK\ PULL\text{-}UP)}$[1] ($\Omega$)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] ($\Omega$)	
VCCI	Min	Max	Min	Max
3.3 V	10 k	45 k	10 k	45 k
3.3 V (wide range I/Os)	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCI_{MAX} - VOH_{spec}) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOL_{spec}) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$

Table 2-45 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
	–2	0.49	3.29	0.03	0.75	0.32	3.36	2.80	1.79	2.01	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-46 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V
Applicable to Standard I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
4 mA	Std.	0.66	9.46	0.04	1.00	0.43	9.64	8.54	2.07	2.04	ns
	–1	0.56	8.05	0.04	0.85	0.36	8.20	7.27	1.76	1.73	ns
	–2	0.49	7.07	0.03	0.75	0.32	7.20	6.38	1.55	1.52	ns
6 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns
8 mA	Std.	0.66	6.57	0.04	1.00	0.43	6.69	5.98	2.40	2.57	ns
	–1	0.56	5.59	0.04	0.85	0.36	5.69	5.09	2.04	2.19	ns
	–2	0.49	4.91	0.03	0.75	0.32	5.00	4.47	1.79	1.92	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-93 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCI	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-94 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)
1.64	1.94	Cross point

*Note: *Measuring point = V_{trip}. See Table 2-22 on page 2-22 for a complete table of trip points.*

Timing Characteristics

Table 2-95 • LVPECL
Commercial-Case Conditions: T_J = 70°C, Worst-Case VCC = 1.425 V, Worst-Case VCCI = 3.0 V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.66	1.80	0.04	1.40	ns
–1	0.56	1.53	0.04	1.19	ns
–2	0.49	1.34	0.03	1.05	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.

Table 2-109 • A3P060 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.71	0.93	0.81	1.05	0.95	1.24	ns
t_{RCKH}	Input High Delay for Global Clock	0.70	0.96	0.80	1.09	0.94	1.28	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-110 • A3P125 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.77	0.99	0.87	1.12	1.03	1.32	ns
t_{RCKH}	Input High Delay for Global Clock	0.76	1.02	0.87	1.16	1.02	1.37	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-113 • A3P600 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.87	1.09	0.99	1.24	1.17	1.46	ns
t_{RCKH}	Input High Delay for Global Clock	0.86	1.11	0.98	1.27	1.15	1.49	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.34	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

Table 2-114 • A3P1000 Global Resource
Commercial-Case Conditions: T_J = 70°C, VCC = 1.425 V

Parameter	Description	–2		–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.94	1.16	1.07	1.32	1.26	1.55	ns
t_{RCKH}	Input High Delay for Global Clock	0.93	1.19	1.06	1.35	1.24	1.59	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.75		0.85		1.00		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.85		0.96		1.13		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.26		0.29		0.35	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage supply levels, refer to Table 2-6 on page 2-6 for derating values.*

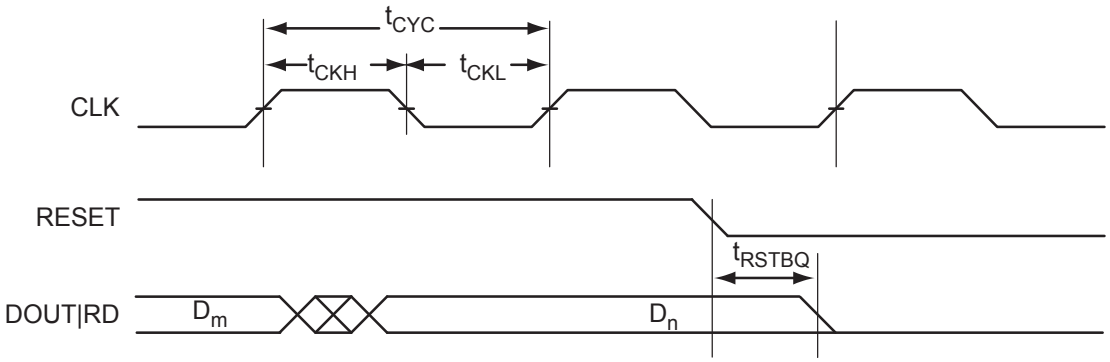


Figure 2-35 • **RAM Reset. Applicable to Both RAM4K9 and RAM512x18.**

In critical applications, an upset in the JTAG circuit could allow entrance to an undesired JTAG state. In such cases, Microsemi recommends tying off TRST to GND through a resistor placed close to the FPGA pin.

Note that to operate at all VJTAG voltages, 500 Ω to 1 kΩ will satisfy the requirements.

Special Function Pins

NC **No Connect**

This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.

DC **Do Not Connect**

This pin should not be connected to any signals on the PCB. These pins should be left unconnected.

Related Documents

User's Guides

ProASIC FPGA Fabric User's Guide

http://www.microsemi.com/soc/documents/PA3_UG.pdf

Packaging

The following documents provide packaging information and device selection for low power flash devices.

Product Catalog

http://www.microsemi.com/soc/documents/ProdCat_PIB.pdf

Lists devices currently recommended for new designs and the packages available for each member of the family. Use this document or the datasheet tables to determine the best package for your design, and which package drawing to use.

Package Mechanical Drawings

http://www.microsemi.com/soc/documents/PckgMechDrwngs.pdf

This document contains the package mechanical drawings for all packages currently or previously supplied by Actel. Use the bookmarks to navigate to the package mechanical drawings.

Additional packaging materials are at *http://www.microsemi.com/products/solutions/package/docs.aspx*.

QN68	
Pin Number	A3P015 Function
1	IO82RSB1
2	IO80RSB1
3	IO78RSB1
4	IO76RSB1
5	GEC0/IO73RSB1
6	GEA0/IO72RSB1
7	GEB0/IO71RSB1
8	VCC
9	GND
10	VCCIB1
11	IO68RSB1
12	IO67RSB1
13	IO66RSB1
14	IO65RSB1
15	IO64RSB1
16	IO63RSB1
17	IO62RSB1
18	IO60RSB1
19	IO58RSB1
20	IO56RSB1
21	IO54RSB1
22	IO52RSB1
23	IO51RSB1
24	VCC
25	GND
26	VCCIB1
27	IO50RSB1
28	IO48RSB1
29	IO46RSB1
30	IO44RSB1
31	IO42RSB1
32	TCK
33	TDI
34	TMS
35	VPUMP
36	TDO

QN68	
Pin Number	A3P015 Function
37	TRST
38	VJTAG
39	IO40RSB0
40	IO37RSB0
41	GDB0/IO34RSB0
42	GDA0/IO33RSB0
43	GDC0/IO32RSB0
44	VCCIB0
45	GND
46	VCC
47	IO31RSB0
48	IO29RSB0
49	IO28RSB0
50	IO27RSB0
51	IO25RSB0
52	IO24RSB0
53	IO22RSB0
54	IO21RSB0
55	IO19RSB0
56	IO17RSB0
57	IO15RSB0
58	IO14RSB0
59	VCCIB0
60	GND
61	VCC
62	IO12RSB0
63	IO10RSB0
64	IO08RSB0
65	IO06RSB0
66	IO04RSB0
67	IO02RSB0
68	IO00RSB0

QN132	
Pin Number	A3P125 Function
A1	GAB2/IO69RSB1
A2	IO130RSB1
A3	VCCIB1
A4	GFC1/IO126RSB1
A5	GFB0/IO123RSB1
A6	VCCPLF
A7	GFA1/IO121RSB1
A8	GFC2/IO118RSB1
A9	IO115RSB1
A10	VCC
A11	GEB1/IO110RSB1
A12	GEA0/IO107RSB1
A13	GEC2/IO104RSB1
A14	IO100RSB1
A15	VCC
A16	IO99RSB1
A17	IO96RSB1
A18	IO94RSB1
A19	IO91RSB1
A20	IO85RSB1
A21	IO79RSB1
A22	VCC
A23	GDB2/IO71RSB1
A24	TDI
A25	TRST
A26	GDC1/IO61RSB0
A27	VCC
A28	IO60RSB0
A29	GCC2/IO59RSB0
A30	GCA2/IO57RSB0
A31	GCA0/IO56RSB0
A32	GCB1/IO53RSB0
A33	IO49RSB0
A34	VCC
A35	IO44RSB0
A36	GBA2/IO41RSB0

QN132	
Pin Number	A3P125 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO68RSB1
B2	GAC2/IO131RSB1
B3	GND
B4	GFC0/IO125RSB1
B5	VCOMPLF
B6	GND
B7	GFB2/IO119RSB1
B8	IO116RSB1
B9	GND
B10	GEB0/IO109RSB1
B11	VMV1
B12	GEB2/IO105RSB1
B13	IO101RSB1
B14	GND
B15	IO98RSB1
B16	IO95RSB1
B17	GND
B18	IO87RSB1
B19	IO81RSB1
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO62RSB0

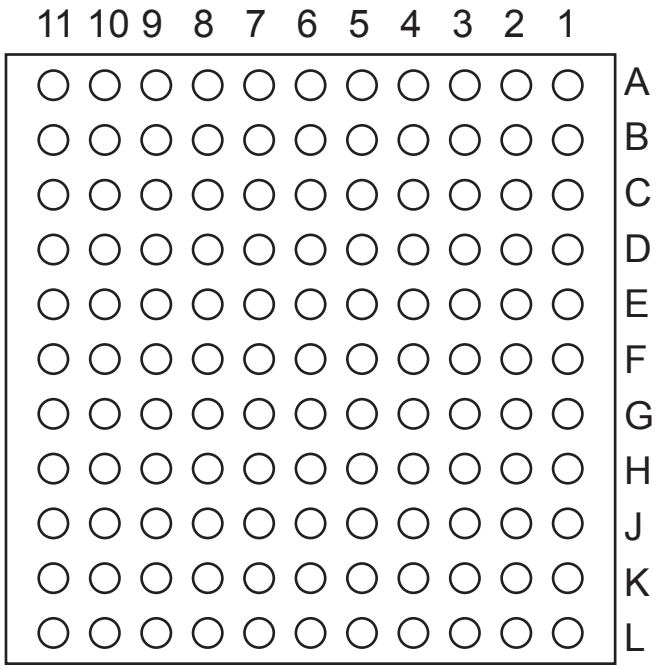
QN132	
Pin Number	A3P125 Function
B25	GND
B26	NC
B27	GCB2/IO58RSB0
B28	GND
B29	GCB0/IO54RSB0
B30	GCC1/IO51RSB0
B31	GND
B32	GBB2/IO43RSB0
B33	VMV0
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO67RSB1
C2	IO132RSB1
C3	VCC
C4	GFB1/IO124RSB1
C5	GFA0/IO122RSB1
C6	GFA2/IO120RSB1
C7	IO117RSB1
C8	VCCIB1
C9	GEA1/IO108RSB1
C10	GNDQ
C11	GEA2/IO106RSB1
C12	IO103RSB1
C13	VCCIB1
C14	IO97RSB1
C15	IO93RSB1
C16	IO89RSB1

QN132	
Pin Number	A3P250 Function
A1	GAB2/IO117UPB3
A2	IO117VPB3
A3	VCCIB3
A4	GFC1/IO110PDB3
A5	GFB0/IO109NPB3
A6	VCCPLF
A7	GFA1/IO108PPB3
A8	GFC2/IO105PPB3
A9	IO103NDB3
A10	VCC
A11	GEA1/IO98PPB3
A12	GEA0/IO98NPB3
A13	GEC2/IO95RSB2
A14	IO91RSB2
A15	VCC
A16	IO90RSB2
A17	IO87RSB2
A18	IO85RSB2
A19	IO82RSB2
A20	IO76RSB2
A21	IO70RSB2
A22	VCC
A23	GDB2/IO62RSB2
A24	TDI
A25	TRST
A26	GDC1/IO58UDB1
A27	VCC
A28	IO54NDB1
A29	IO52NDB1
A30	GCA2/IO51PPB1
A31	GCA0/IO50NPB1
A32	GCB1/IO49PDB1
A33	IO47NSB1
A34	VCC
A35	IO41NPB1
A36	GBA2/IO41PPB1

QN132	
Pin Number	A3P250 Function
A37	GBB1/IO38RSB0
A38	GBC0/IO35RSB0
A39	VCCIB0
A40	IO28RSB0
A41	IO22RSB0
A42	IO18RSB0
A43	IO14RSB0
A44	IO11RSB0
A45	IO07RSB0
A46	VCC
A47	GAC1/IO05RSB0
A48	GAB0/IO02RSB0
B1	IO118VDB3
B2	GAC2/IO116UDB3
B3	GND
B4	GFC0/IO110NDB3
B5	VCOMPLF
B6	GND
B7	GFB2/IO106PSB3
B8	IO103PDB3
B9	GND
B10	GEB0/IO99NDB3
B11	VMV3
B12	GEB2/IO96RSB2
B13	IO92RSB2
B14	GND
B15	IO89RSB2
B16	IO86RSB2
B17	GND
B18	IO78RSB2
B19	IO72RSB2
B20	GND
B21	GNDQ
B22	TMS
B23	TDO
B24	GDC0/IO58VDB1

QN132	
Pin Number	A3P250 Function
B25	GND
B26	IO54PDB1
B27	GCB2/IO52PDB1
B28	GND
B29	GCB0/IO49NDB1
B30	GCC1/IO48PDB1
B31	GND
B32	GBB2/IO42PDB1
B33	VMV1
B34	GBA0/IO39RSB0
B35	GBC1/IO36RSB0
B36	GND
B37	IO26RSB0
B38	IO21RSB0
B39	GND
B40	IO13RSB0
B41	IO08RSB0
B42	GND
B43	GAC0/IO04RSB0
B44	GNDQ
C1	GAA2/IO118UDB3
C2	IO116VDB3
C3	VCC
C4	GFB1/IO109PPB3
C5	GFA0/IO108NPB3
C6	GFA2/IO107PSB3
C7	IO105NPB3
C8	VCCIB3
C9	GEB1/IO99PDB3
C10	GNDQ
C11	GEA2/IO97RSB2
C12	IO94RSB2
C13	VCCIB2
C14	IO88RSB2
C15	IO84RSB2
C16	IO80RSB2

CS121 – Bottom View



Note: The die attach paddle center of the package is tied to ground (GND).

Note

For more information on package drawings, see *PD3068: Package Mechanical Drawings*.

VQ100	
Pin Number	A3P125 Function
1	GND
2	GAA2/IO67RSB1
3	IO68RSB1
4	GAB2/IO69RSB1
5	IO132RSB1
6	GAC2/IO131RSB1
7	IO130RSB1
8	IO129RSB1
9	GND
10	GFB1/IO124RSB1
11	GFB0/IO123RSB1
12	VCOMPLF
13	GFA0/IO122RSB1
14	VCCPLF
15	GFA1/IO121RSB1
16	GFA2/IO120RSB1
17	VCC
18	VCCIB1
19	GEC0/IO111RSB1
20	GEB1/IO110RSB1
21	GEB0/IO109RSB1
22	GEA1/IO108RSB1
23	GEA0/IO107RSB1
24	VMV1
25	GNDQ
26	GEA2/IO106RSB1
27	GEB2/IO105RSB1
28	GEC2/IO104RSB1
29	IO102RSB1
30	IO100RSB1
31	IO99RSB1
32	IO97RSB1
33	IO96RSB1
34	IO95RSB1
35	IO94RSB1
36	IO93RSB1

VQ100	
Pin Number	A3P125 Function
37	VCC
38	GND
39	VCCIB1
40	IO87RSB1
41	IO84RSB1
42	IO81RSB1
43	IO75RSB1
44	GDC2/IO72RSB1
45	GDB2/IO71RSB1
46	GDA2/IO70RSB1
47	TCK
48	TDI
49	TMS
50	VMV1
51	GND
52	VPUMP
53	NC
54	TDO
55	TRST
56	VJTAG
57	GDA1/IO65RSB0
58	GDC0/IO62RSB0
59	GDC1/IO61RSB0
60	GCC2/IO59RSB0
61	GCB2/IO58RSB0
62	GCA0/IO56RSB0
63	GCA1/IO55RSB0
64	GCC0/IO52RSB0
65	GCC1/IO51RSB0
66	VCCIB0
67	GND
68	VCC
69	IO47RSB0
70	GBC2/IO45RSB0
71	GBB2/IO43RSB0
72	IO42RSB0

VQ100	
Pin Number	A3P125 Function
73	GBA2/IO41RSB0
74	VMV0
75	GNDQ
76	GBA1/IO40RSB0
77	GBA0/IO39RSB0
78	GBB1/IO38RSB0
79	GBB0/IO37RSB0
80	GBC1/IO36RSB0
81	GBC0/IO35RSB0
82	IO32RSB0
83	IO28RSB0
84	IO25RSB0
85	IO22RSB0
86	IO19RSB0
87	VCCIB0
88	GND
89	VCC
90	IO15RSB0
91	IO13RSB0
92	IO11RSB0
93	IO09RSB0
94	IO07RSB0
95	GAC1/IO05RSB0
96	GAC0/IO04RSB0
97	GAB1/IO03RSB0
98	GAB0/IO02RSB0
99	GAA1/IO01RSB0
100	GAA0/IO00RSB0

PQ208	
Pin Number	A3P400 Function
1	GND
2	GAA2/IO155UDB3
3	IO155VDB3
4	GAB2/IO154UDB3
5	IO154VDB3
6	GAC2/IO153UDB3
7	IO153VDB3
8	IO152UDB3
9	IO152VDB3
10	IO151UDB3
11	IO151VDB3
12	IO150PDB3
13	IO150NDB3
14	IO149PDB3
15	IO149NDB3
16	VCC
17	GND
18	VCCIB3
19	IO148PDB3
20	IO148NDB3
21	GFC1/IO147PDB3
22	GFC0/IO147NDB3
23	GFB1/IO146PDB3
24	GFB0/IO146NDB3
25	VCOMPLF
26	GFA0/IO145NPB3
27	VCCPLF
28	GFA1/IO145PPB3
29	GND
30	GFA2/IO144PDB3
31	IO144NDB3
32	GFB2/IO143PDB3
33	IO143NDB3
34	GFC2/IO142PDB3
35	IO142NDB3
36	NC

PQ208	
Pin Number	A3P400 Function
37	IO141PSB3
38	IO140PDB3
39	IO140NDB3
40	VCCIB3
41	GND
42	IO138PDB3
43	IO138NDB3
44	GEC1/IO137PDB3
45	GEC0/IO137NDB3
46	GEB1/IO136PDB3
47	GEB0/IO136NDB3
48	GEA1/IO135PDB3
49	GEA0/IO135NDB3
50	VMV3
51	GNDQ
52	GND
53	VMV2
54	NC
55	GEA2/IO134RSB2
56	GEB2/IO133RSB2
57	GEC2/IO132RSB2
58	IO131RSB2
59	IO130RSB2
60	IO129RSB2
61	IO128RSB2
62	VCCIB2
63	IO125RSB2
64	IO123RSB2
65	GND
66	IO121RSB2
67	IO119RSB2
68	IO117RSB2
69	IO115RSB2
70	IO113RSB2
71	VCC
72	VCCIB2

PQ208	
Pin Number	A3P400 Function
73	IO112RSB2
74	IO111RSB2
75	IO110RSB2
76	IO109RSB2
77	IO108RSB2
78	IO107RSB2
79	IO106RSB2
80	IO104RSB2
81	GND
82	IO102RSB2
83	IO101RSB2
84	IO100RSB2
85	IO99RSB2
86	IO98RSB2
87	IO97RSB2
88	VCC
89	VCCIB2
90	IO94RSB2
91	IO92RSB2
92	IO90RSB2
93	IO88RSB2
94	IO86RSB2
95	IO84RSB2
96	GDC2/IO82RSB2
97	GND
98	GDB2/IO81RSB2
99	GDA2/IO80RSB2
100	GNDQ
101	TCK
102	TDI
103	TMS
104	VMV2
105	GND
106	VPUMP
107	NC
108	TDO

FG144	
Pin Number	**A3P1000 Function**
A1	GNDQ
A2	VMV0
A3	GAB0/IO02RSB0
A4	GAB1/IO03RSB0
A5	IO10RSB0
A6	GND
A7	IO44RSB0
A8	VCC
A9	IO69RSB0
A10	GBA0/IO76RSB0
A11	GBA1/IO77RSB0
A12	GNDQ
B1	GAB2/IO224PDB3
B2	GND
B3	GAA0/IO00RSB0
B4	GAA1/IO01RSB0
B5	IO13RSB0
B6	IO26RSB0
B7	IO35RSB0
B8	IO60RSB0
B9	GBB0/IO74RSB0
B10	GBB1/IO75RSB0
B11	GND
B12	VMV1
C1	IO224NDB3
C2	GFA2/IO206PPB3
C3	GAC2/IO223PDB3
C4	VCC
C5	IO16RSB0
C6	IO29RSB0
C7	IO32RSB0
C8	IO63RSB0
C9	IO66RSB0
C10	GBA2/IO78PDB1
C11	IO78NDB1
C12	GBC2/IO80PPB1

FG144	
Pin Number	**A3P1000 Function**
D1	IO213PDB3
D2	IO213NDB3
D3	IO223NDB3
D4	GAA2/IO225PPB3
D5	GAC0/IO04RSB0
D6	GAC1/IO05RSB0
D7	GBC0/IO72RSB0
D8	GBC1/IO73RSB0
D9	GBB2/IO79PDB1
D10	IO79NDB1
D11	IO80NPB1
D12	GCB1/IO92PPB1
E1	VCC
E2	GFC0/IO209NDB3
E3	GFC1/IO209PDB3
E4	VCCIB3
E5	IO225NPB3
E6	VCCIB0
E7	VCCIB0
E8	GCC1/IO91PDB1
E9	VCCIB1
E10	VCC
E11	GCA0/IO93NDB1
E12	IO94NDB1
F1	GFB0/IO208NPB3
F2	VCOMPLF
F3	GFB1/IO208PPB3
F4	IO206NPB3
F5	GND
F6	GND
F7	GND
F8	GCC0/IO91NDB1
F9	GCB0/IO92NPB1
F10	GND
F11	GCA1/IO93PDB1
F12	GCA2/IO94PDB1

FG144	
Pin Number	**A3P1000 Function**
G1	GFA1/IO207PPB3
G2	GND
G3	VCCPLF
G4	GFA0/IO207NPB3
G5	GND
G6	GND
G7	GND
G8	GDC1/IO111PPB1
G9	IO96NDB1
G10	GCC2/IO96PDB1
G11	IO95NDB1
G12	GCB2/IO95PDB1
H1	VCC
H2	GFB2/IO205PDB3
H3	GFC2/IO204PSB3
H4	GEC1/IO190PDB3
H5	VCC
H6	IO105PDB1
H7	IO105NDB1
H8	GDB2/IO115RSB2
H9	GDC0/IO111NPB1
H10	VCCIB1
H11	IO101PSB1
H12	VCC
J1	GEB1/IO189PDB3
J2	IO205NDB3
J3	VCCIB3
J4	GEC0/IO190NDB3
J5	IO160RSB2
J6	IO157RSB2
J7	VCC
J8	TCK
J9	GDA2/IO114RSB2
J10	TDO
J11	GDA1/IO113PDB1
J12	GDB1/IO112PDB1

FG256	
Pin Number	**A3P250 Function**
G13	GCC1/IO48PPB1
G14	IO47NPB1
G15	IO54PDB1
G16	IO54NDB1
H1	GFB0/IO109NPB3
H2	GFA0/IO108NDB3
H3	GFB1/IO109PPB3
H4	VCOMPLF
H5	GFC0/IO110NPB3
H6	VCC
H7	GND
H8	GND
H9	GND
H10	GND
H11	VCC
H12	GCC0/IO48NPB1
H13	GCB1/IO49PPB1
H14	GCA0/IO50NPB1
H15	NC
H16	GCB0/IO49NPB1
J1	GFA2/IO107PPB3
J2	GFA1/IO108PDB3
J3	VCCPLF
J4	IO106NDB3
J5	GFB2/IO106PDB3
J6	VCC
J7	GND
J8	GND
J9	GND
J10	GND
J11	VCC
J12	GCB2/IO52PPB1
J13	GCA1/IO50PPB1
J14	GCC2/IO53PPB1
J15	NC
J16	GCA2/IO51PDB1

FG256	
Pin Number	**A3P250 Function**
K1	GFC2/IO105PDB3
K2	IO107NPB3
K3	IO104PPB3
K4	NC
K5	VCCIB3
K6	VCC
K7	GND
K8	GND
K9	GND
K10	GND
K11	VCC
K12	VCCIB1
K13	IO52NPB1
K14	IO55RSB1
K15	IO53NPB1
K16	IO51NDB1
L1	IO105NDB3
L2	IO104NPB3
L3	NC
L4	IO102RSB3
L5	VCCIB3
L6	GND
L7	VCC
L8	VCC
L9	VCC
L10	VCC
L11	GND
L12	VCCIB1
L13	GDB0/IO59VPB1
L14	IO57VDB1
L15	IO57UDB1
L16	IO56PDB1
M1	IO103PDB3
M2	NC
M3	IO101NPB3
M4	GEC0/IO100NPB3

FG256	
Pin Number	**A3P250 Function**
M5	VMV3
M6	VCCIB2
M7	VCCIB2
M8	NC
M9	IO74RSB2
M10	VCCIB2
M11	VCCIB2
M12	VMV2
M13	NC
M14	GDB1/IO59UPB1
M15	GDC1/IO58UDB1
M16	IO56NDB1
N1	IO103NDB3
N2	IO101PPB3
N3	GEC1/IO100PPB3
N4	NC
N5	GNDQ
N6	GEA2/IO97RSB2
N7	IO86RSB2
N8	IO82RSB2
N9	IO75RSB2
N10	IO69RSB2
N11	IO64RSB2
N12	GNDQ
N13	NC
N14	VJTAG
N15	GDC0/IO58VDB1
N16	GDA1/IO60UDB1
P1	GEB1/IO99PDB3
P2	GEB0/IO99NDB3
P3	NC
P4	NC
P5	IO92RSB2
P6	IO89RSB2
P7	IO85RSB2
P8	IO81RSB2

FG256	
Pin Number	A3P600 Function
A1	GND
A2	GAA0/IO00RSB0
A3	GAA1/IO01RSB0
A4	GAB0/IO02RSB0
A5	IO11RSB0
A6	IO16RSB0
A7	IO18RSB0
A8	IO28RSB0
A9	IO34RSB0
A10	IO37RSB0
A11	IO41RSB0
A12	IO43RSB0
A13	GBB1/IO57RSB0
A14	GBA0/IO58RSB0
A15	GBA1/IO59RSB0
A16	GND
B1	GAB2/IO173PDB3
B2	GAA2/IO174PDB3
B3	GNDQ
B4	GAB1/IO03RSB0
B5	IO13RSB0
B6	IO14RSB0
B7	IO21RSB0
B8	IO27RSB0
B9	IO32RSB0
B10	IO38RSB0
B11	IO42RSB0
B12	GBC1/IO55RSB0
B13	GBB0/IO56RSB0
B14	IO52RSB0
B15	GBA2/IO60PDB1
B16	IO60NDB1
C1	IO173NDB3
C2	IO174NDB3
C3	VMV3
C4	IO07RSB0

FG256	
Pin Number	A3P600 Function
C5	GAC0/IO04RSB0
C6	GAC1/IO05RSB0
C7	IO20RSB0
C8	IO24RSB0
C9	IO33RSB0
C10	IO39RSB0
C11	IO44RSB0
C12	GBC0/IO54RSB0
C13	IO51RSB0
C14	VMV0
C15	IO61NPB1
C16	IO63PDB1
D1	IO171NDB3
D2	IO171PDB3
D3	GAC2/IO172PDB3
D4	IO06RSB0
D5	GNDQ
D6	IO10RSB0
D7	IO19RSB0
D8	IO26RSB0
D9	IO30RSB0
D10	IO40RSB0
D11	IO45RSB0
D12	GNDQ
D13	IO50RSB0
D14	GBB2/IO61PPB1
D15	IO53RSB0
D16	IO63NDB1
E1	IO166PDB3
E2	IO167NPB3
E3	IO172NDB3
E4	IO169NDB3
E5	VMV0
E6	VCCIB0
E7	VCCIB0
E8	IO25RSB0

FG256	
Pin Number	A3P600 Function
E9	IO31RSB0
E10	VCCIB0
E11	VCCIB0
E12	VMV1
E13	GBC2/IO62PDB1
E14	IO67PPB1
E15	IO64PPB1
E16	IO66PDB1
F1	IO166NDB3
F2	IO168NPB3
F3	IO167PPB3
F4	IO169PDB3
F5	VCCIB3
F6	GND
F7	VCC
F8	VCC
F9	VCC
F10	VCC
F11	GND
F12	VCCIB1
F13	IO62NDB1
F14	IO64NPB1
F15	IO65PPB1
F16	IO66NDB1
G1	IO165NDB3
G2	IO165PDB3
G3	IO168PPB3
G4	GFC1/IO164PPB3
G5	VCCIB3
G6	VCC
G7	GND
G8	GND
G9	GND
G10	GND
G11	VCC
G12	VCCIB1

Revision	Changes	Page
v2.0 (April 2007)	In the "Packaging Tables", Ambient was deleted.	ii
	The timing characteristics tables were updated.	N/A
	The "PLL Macro" section was updated to add information on the VCO and PLL outputs during power-up.	2-15
	The "PLL Macro" section was updated to include power-up information.	2-15
	Table 2-11 • ProASIC3 CCC/PLL Specification was updated.	2-29
	Figure 2-19 • Peak-to-Peak Jitter Definition is new.	2-18
	The "SRAM and FIFO" section was updated with operation and timing requirement information.	2-21
	The "RESET" section was updated with read and write information.	2-25
	The "RESET" section was updated with read and write information.	2-25
	The "Introduction" in the "Advanced I/Os" section was updated to include information on input and output buffers being disabled.	2-28
	PCI-X 3.3 V was added to Table 2-11 • VCCI Voltages and Compatible Standards.	2-29
	In the Table 2-15 • Levels of Hot-Swap Support, the ProASIC3 compliance descriptions were updated for levels 3 and 4.	2-34
	Table 2-43 • I/O Hot-Swap and 5 V Input Tolerance Capabilities in ProASIC3 Devices was updated.	2-64
	Notes 3, 4, and 5 were added to Table 2-17 • Comparison Table for 5 V–Compliant Receiver Scheme. 5 x 52.72 was changed to 52.7 and the Maximum current was updated from 4 x 52.7 to 5 x 52.7.	2-40
	The "VCCPLF PLL Supply Voltage" section was updated.	2-50
	The "VPUMP Programming Supply Voltage" section was updated.	2-50
	The "GL Globals" section was updated to include information about direct input into quadrant clocks.	2-51
	V_{JTAG} was deleted from the "TCK Test Clock" section.	2-51
	In Table 2-22 • Recommended Tie-Off Values for the TCK and TRST Pins, TSK was changed to TCK in note 2. Note 3 was also updated.	2-51
	Ambient was deleted from Table 3-2 • Recommended Operating Conditions. VPUMP programming mode was changed from "3.0 to 3.6" to "3.15 to 3.45".	3-2
	Note 3 is new in Table 3-4 • Overshoot and Undershoot Limits (as measured on quiet I/Os)1.	3-2
	In EQ 3-2, 150 was changed to 110 and the result changed from 3.9 to 1.951.	3-5
	Table 3-6 • Temperature and Voltage Derating Factors for Timing Delays was updated.	3-6
	Table 3-5 • Package Thermal Resistivities was updated.	3-5
	Table 3-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings (Advanced) and Table 3-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Commercial and Industrial Conditions (Standard Plus) were updated.	3-17 to 3-17