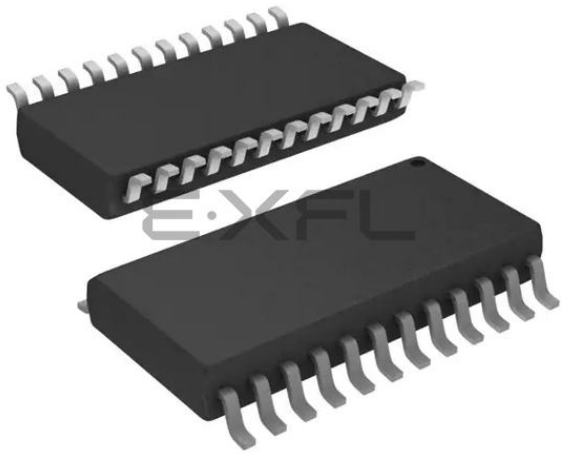

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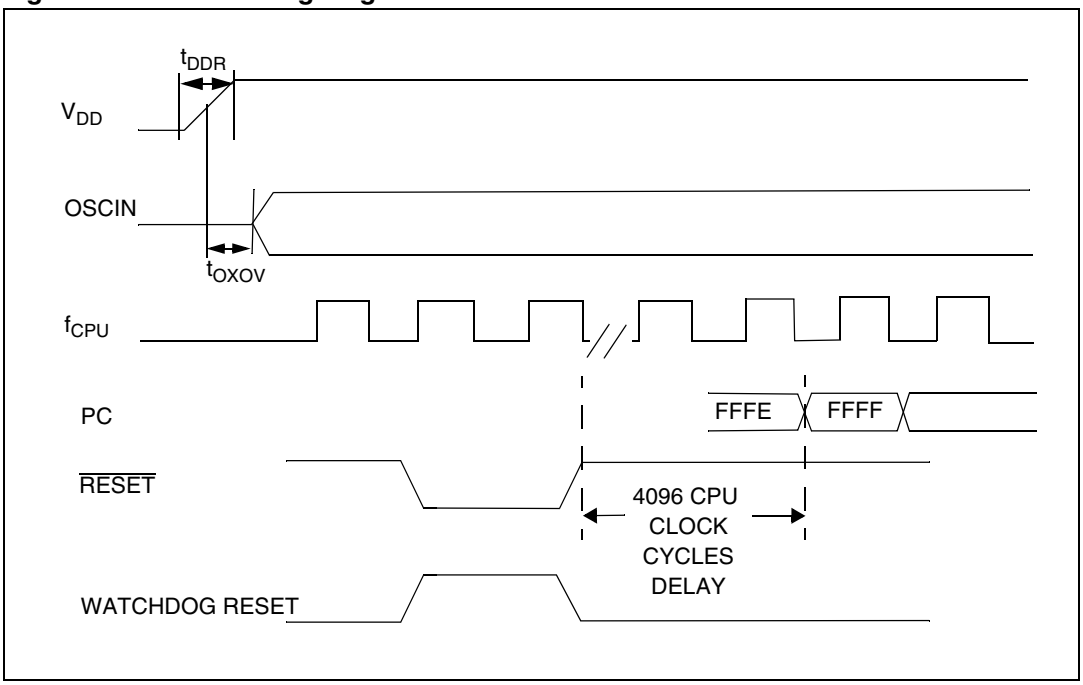
What is "Embedded - Microcontrollers"?

"Embedded - Microcontrollers" refer to small, integrated circuits designed to perform specific tasks within larger systems. These microcontrollers are essentially compact computers on a single chip, containing a processor core, memory, and programmable input/output peripherals. They are called "embedded" because they are embedded within electronic devices to control various functions, rather than serving as standalone computers. Microcontrollers are crucial in modern electronics, providing the intelligence and control needed for a wide range of applications.

Applications of "Embedded - Microcontrollers"

Details	
Product Status	Obsolete
Core Processor	ST7
Core Size	8-Bit
Speed	8MHz
Connectivity	SCI, UART/USART, USB
Peripherals	DMA, LVD, POR, PWM, WDT
Number of I/O	14
Program Memory Size	8KB (8K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	384 x 8
Voltage - Supply (Vcc/Vdd)	4V ~ 5.5V
Data Converters	-
Oscillator Type	Internal
Operating Temperature	0°C ~ 70°C (TA)
Mounting Type	Surface Mount
Package / Case	24-SOIC (0.295", 7.50mm Width)
Supplier Device Package	-
Purchase URL	https://www.e-xfl.com/product-detail/stmicroelectronics/st72f60e2m1

Figure 12. Reset timing diagram



Note: Refer to Electrical Characteristics for values of t_{DDR}, t_{oxov}, V_{IT+}, V_{IT-} and V_{hys}

7.3 Clock system

7.3.1 General description

The MCU accepts either a crystal or ceramic resonator, or an external clock signal to drive the internal oscillator. The internal clock (f_{CPU}) is derived from the external oscillator frequency (f_{OSC}), which is divided by 3 (and by 2 or 4 for USB, depending on the external clock used). The internal clock is further divided by 2 by setting the SMS bit in the Miscellaneous Register.
Using the OSC24/12 bit in the option byte, a 12 MHz or a 24 MHz external clock can be used to provide an internal frequency of either 2, 4 or 8 MHz while maintaining a 6 MHz for the USB (refer to *Figure 15*).

The internal clock signal (f_{CPU}) is also routed to the on-chip peripherals. The CPU clock signal consists of a square wave with a duty cycle of 50%.

The internal oscillator is designed to operate with an AT-cut parallel resonant quartz or ceramic resonator in the frequency range specified for f_{osc}. The circuit shown in *Figure 14* is recommended when using a crystal, and *Table 9* lists the recommended capacitance. The crystal and associated components should be mounted as close as possible to the input pins in order to minimize output distortion and start-up stabilisation time.

Figure 15. Clock block diagram

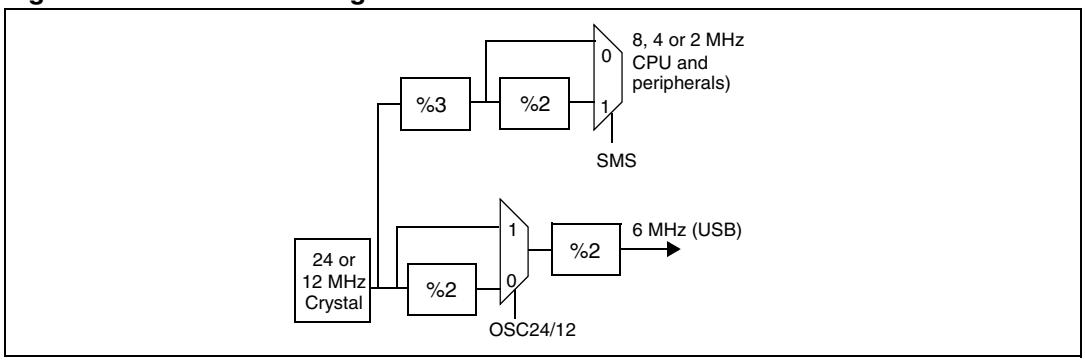


Table 10. Interrupt mapping

N°	Source block	Description	Register label	Priority order	Exit from Halt	Vector address
	RESET	Reset	N/A	Highest Priority	yes	FFFEh-FFFFh
	TRAP	Software Interrupt			no	FFFCh-FFFDh
	FLASH	Flash Start Programming Interrupt			yes	FFFAh-FFFBh
	USB	End Suspend Mode	ISTR		yes	FFF8h-FFF9h
1	ITi	External Interrupts	ITRFRE			FFF6h-FFF7h
2	TIMER	Timer Peripheral Interrupts	TIMSR		no	FFF4h-FFF5h
3	Reserved					FFF2h-FFF3h
4	SCI	SCI Peripheral Interrupts	SCISR	Lowest Priority		FFF0h-FFF1h
5	USB	USB Peripheral Interrupts	ISTR			FFEEh-FFEFh

8.0.1 Interrupt register (ITRFRE)

ITRFRE — Reset value: 0000 0000 (00h)

7	6	5	4	3	2	1	0
IT8E	IT7E	IT6E	IT5E	IT4E	IT3E	IT2E	IT1E
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 11. ITRFRE register description

Bit	Name	Function
7:0	ITiE (i=1 to 8)	Interrupt enable control bits If an ITiE bit is set, the corresponding interrupt is generated when: – a rising edge occurs on the pin PA4/IT1 or PA5/IT2 or PB4/IT5 or PB5/IT6 or – a falling edge occurs on the pin PA6/IT3 or PA7/IT4 or PB6/IT7 or PB7/IT8 No interrupt is generated elsewhere..

Table 12. Interrupt register map and reset values

Address (Hex.)	Register label	7	6	5	4	3	2	1	0
0008h	ITRFRE reset value	IT8E 0	IT7E 0	IT6E 0	IT5E 0	IT4E 0	IT3E 0	IT2E 0	IT1E 0

Figure 19. PA0, PA3, PA4, PA5, PA6, PA7 configuration

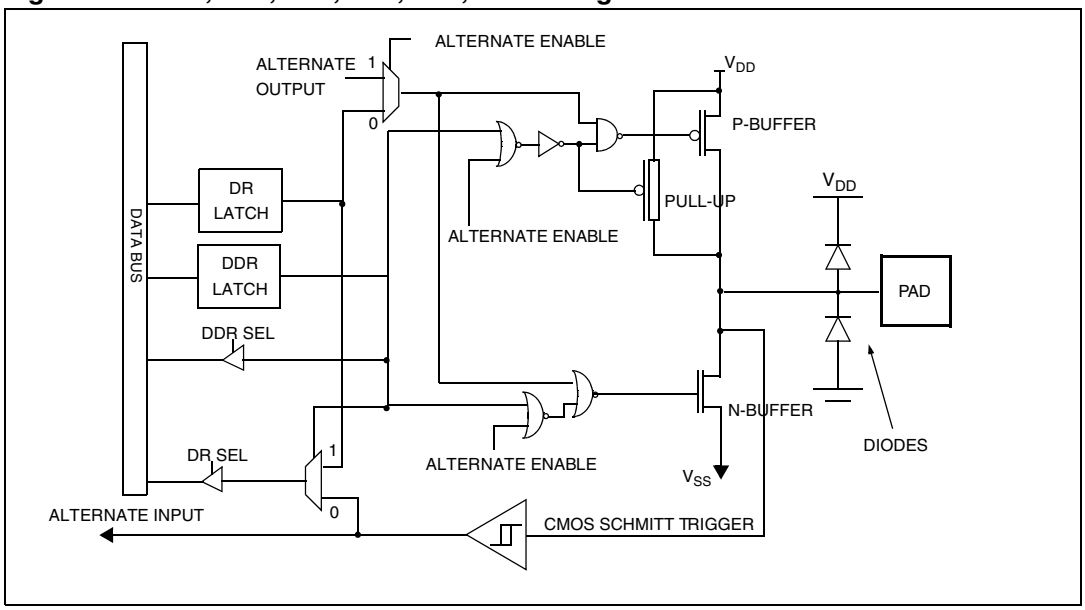


Table 15. PA1, PA2 description

Port A	I/O		Alternate function	
	Input(1)	Output	Signal	Condition
PA1	without pull-up	Very High Current open drain		
PA2	without pull-up	Very High Current open drain		

1. Reset state

Figure 31. Output compare block diagram

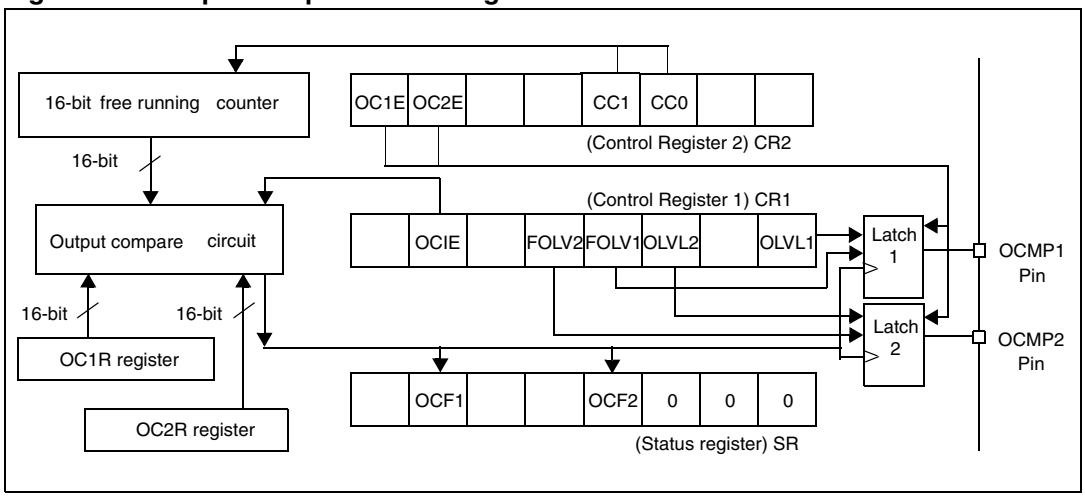


Figure 32. Output compare timing diagram, $f_{TIMER} = f_{CPU}/2$

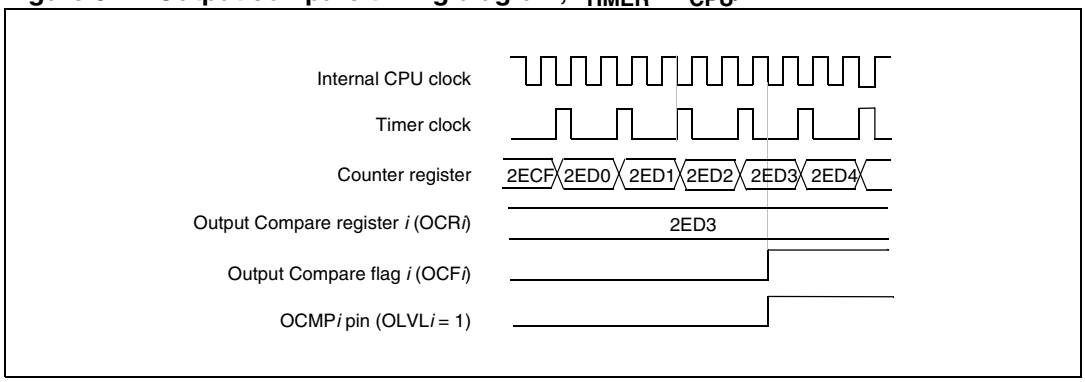


Figure 33. Output compare timing diagram, $f_{TIMER} = f_{CPU}/4$

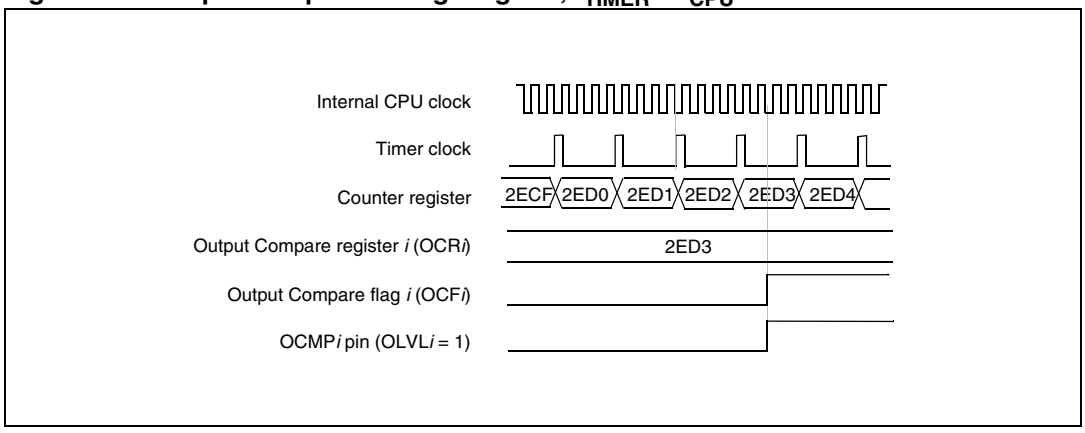


Table 33. CSR register description (continued)

Bit	Name	Function
6	OCF1	Output Compare Flag 1 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC1R register. To clear this bit, first read the SR register, then read or write the low byte of the OC1R (OC1LR) register.
5	TOF	Timer Overflow Flag 0: No timer overflow (reset value). 1: The free running counter rolled over from FFFFh to 0000h. To clear this bit, first read the SR register, then read or write the low byte of the CR (CLR) register. *Note: Reading or writing the ACLR register does not clear TOF.*
4	ICF2	Input Capture Flag 2 0: No input capture (reset value). 1: An Input Capture has occurred on the ICAP2 pin. To clear this bit, first read the SR register, then read or write the low byte of the IC2R (IC2LR) register.
3	OCF2	Output Compare Flag 2 0: No match (reset value). 1: The content of the free running counter has matched the content of the OC2R register. To clear this bit, first read the SR register, then read or write the low byte of the OC2R (OC2LR) register.
2	TIMD	Timer Disable This bit is set and cleared by software. When set, it freezes the timer prescaler and counter and disabled the output functions (OCMP1 and OCMP2 pins) to reduce power consumption. Access to the timer registers is still available, allowing the timer configuration to be changed, or the counter reset, while it is disabled. 0: Timer enabled. 1: Timer prescaler, counter and outputs disabled.
1:0	-	Reserved, must be kept cleared.

Input capture 1 high register (IC1HR)

This is an 8-bit register that contains the high part of the counter value (transferred by the input capture 1 event).

IC1HR Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Alternate counter low register (ACLR)

This is an 8-bit register that contains the low part of the counter value. A write to this register resets the counter. An access to this register after an access to CSR register does not clear the TOF bit in the CSR register.

ACLR — Reset value: 1111 1100 (FCh)

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Input capture 2 high register (IC2HR)

This is an 8-bit register that contains the high part of the counter value (transferred by the Input Capture 2 event).

1C2HR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

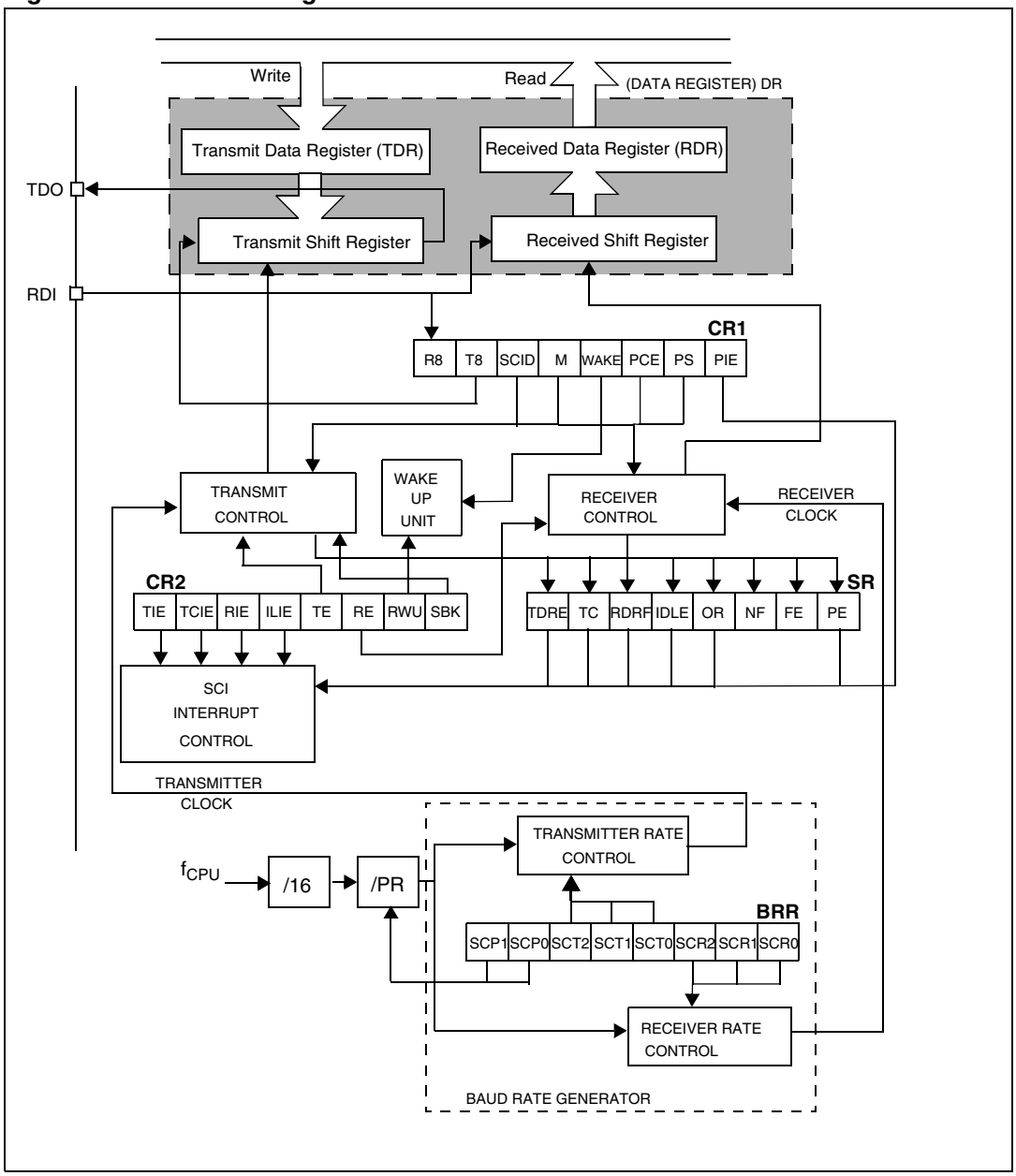
Input capture 2 low register (IC2LR)

This is an 8-bit register that contains the low part of the counter value (transferred by the Input Capture 2 event).

1C2LR — Reset value: undefined

7	6	5	4	3	2	1	0
MSB							LSB
RO	RO	RO	RO	RO	RO	RO	RO

Figure 38. SCI block diagram



13.2.2 Functional description

The block diagram of the Serial Control Interface, is shown in *Figure 38*. It contains 6 dedicated registers:

- Two control registers (SCICR1 & SCICR2)
- A status register (SCISR)
- A baud rate register (SCIBRR)

Refer to the register descriptions in *Section 13.3* for the definitions of each bit.

Noise error

Oversampling techniques are used for data recovery by discriminating between valid incoming data and noise. Normal data bits are considered valid if three consecutive samples (8th, 9th, 10th) have the same bit value, otherwise the NF flag is set. In the case of start bit detection, the NF flag is set on the basis of an algorithm combining both valid edge detection and three samples (8th, 9th, 10th). Therefore, to prevent the NF flag getting set during start bit reception, there should be a valid edge detection as well as three valid samples.

When noise is detected in a frame:

- The NF flag is set at the rising edge of the RDRF bit.
- Data is transferred from the Shift register to the SCIDR register.
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The NF flag is reset by a SCISR register read operation followed by a SCIDR register read operation.

During reception, if a false start bit is detected (e.g. 8th, 9th, 10th samples are 011,101,110), the frame is discarded and the receiving sequence is not started for this frame. There is no RDRF bit set for this frame and the NF flag is set internally (not accessible to the user). This NF flag is accessible along with the RDRF bit when a next valid frame is received.

Note: If the application Start Bit is not long enough to match the above requirements, then the NF Flag may get set due to the short Start Bit. In this case, the NF flag may be ignored by the application software when the first valid byte is received.

See also *Noise error causes*.

Framing Error

A framing error is detected when:

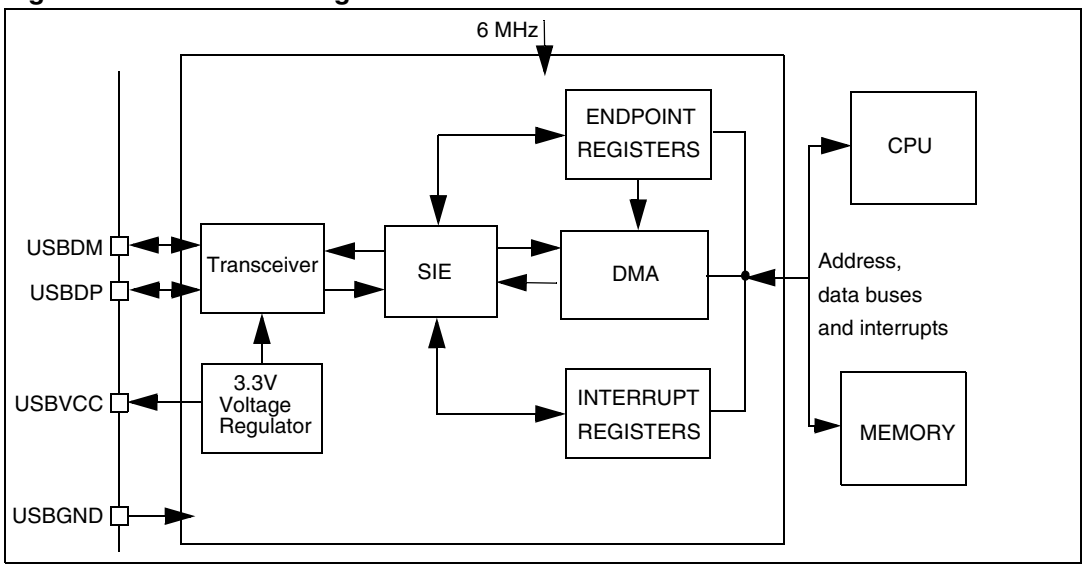
- The stop bit is not recognized on reception at the expected time, following either a de-synchronization or excessive noise.
- A break is received.

When the framing error is detected:

- The FE bit is set by hardware
- Data is transferred from the Shift register to the SCIDR register.
- No interrupt is generated. However this bit rises at the same time as the RDRF bit which itself generates an interrupt.

The FE bit is reset by a SCISR register read operation followed by a SCIDR register read operation.

Figure 41. USB block diagram



14.4 Register description

14.4.1 DMA address register (DMAR)

DMAR — Reset value: undefined (xxh)

7	6	5	4	3	2	1	0
DA15	DA14	DA13	DA12	DA11	DA10	DA9	DA8
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:0=**DA[15:8]** *DMA address bits 15-8.*
Software must write the start address of the DMA memory area whose most significant bits are given by DA15-DA6. The remaining 6 address bits are set by hardware. See the description of the IDR register and *Figure 42*.

14.4.2 Interrupt/DMA register (IDR)

IDR — Reset value: xxxx 0000 (x0h)

7	6	5	4	3	2	1	0
DA7	DA6	EP1	EP0	CNT3	CNT2	CNT1	CNT0
R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bits 7:6 = **DA[7:6]** *DMA address bits 7-6.*
Software must reset these bits. See the description of the DMAR register and *Figure 42*.

Bits 5:4 = **EP[1:0]** *Endpoint number* (read-only). These bits identify the endpoint which required attention.
00: Endpoint 0
01: Endpoint 1
10: Endpoint 2

Table 62. Control timings (continued)

Symbol	Parameter	Conditions	Value			Unit
			Min	Typ	Max	
t_{DOG}	Watchdog time-out	f_{CPU} = 8 MHz	49152 6.144		3145728 393.216	t_{CPU} ms
t_{OXOV}	Crystal oscillator start-up time		20(1)	30	40(1)	ms
t_{DDR}	Power up rise time	from V_{DD} = 0 to 4 V			100(1)	ms

1. Not tested in production, guaranteed by characterization.

16.8.2 Output driving current

Subject to general operating condition for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 71. Output current characteristics

Symbol	Parameter	Conditions		Min	Max	Unit
V_{OL} (1)	Output low level voltage for a standard I/O pin when up to 8 pins are sunk at the same time, Port A0, Port A(3:7), Port C(0:2)	V_{DD}=5 V	I_{IO}=+1.6 mA		0.4	V
	Output low level voltage for a high sink I/O pin when up to 4 pins are sunk at the same time, Port B(0:7)		I_{IO}=+10 mA		1.3	
	Output low level voltage for a very high sink I/O pin when up to 2 pins are sunk at the same time, Port A1, Port A2		I_{IO}=+25 mA		1.5	
V_{OH} (2)	Output high level voltage for an I/O pin when up to 8 pins are sourced at same time		I_{IO}=-10 mA	V_{DD}-1.3		
			I_{IO}=-1.6 mA	V_{DD}-0.8		

1. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 16.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
2. The I_{IO} current sourced must always respect the absolute maximum rating specified in *Section 16.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VDD}. True open drain I/O pins does not have V_{OH}.

Figure 54. V_{OL} standard V_{DD}=5 V

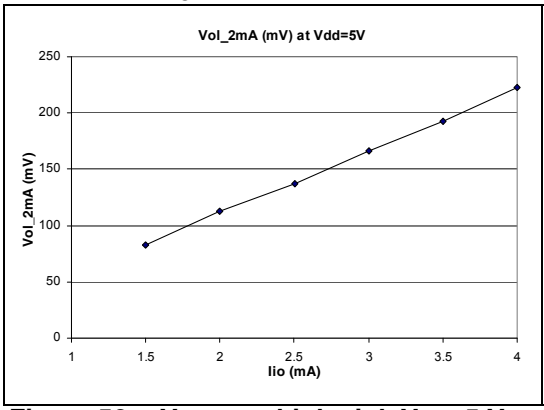


Figure 55. V_{OL} high sink V_{DD}=5 V

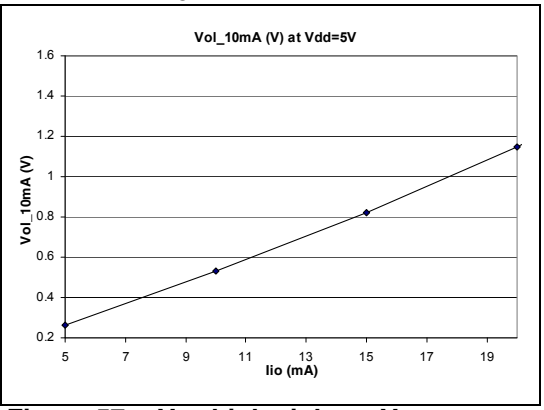


Figure 56. V_{OL} very high sink V_{DD}=5 V

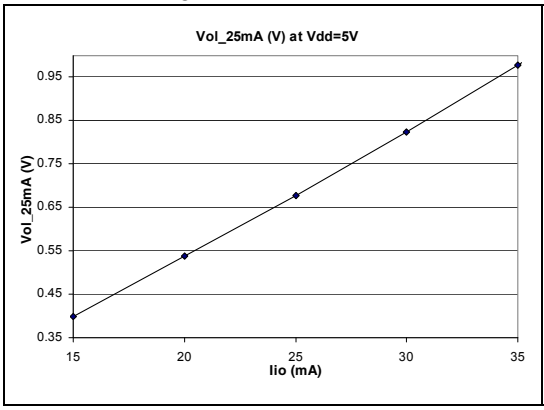
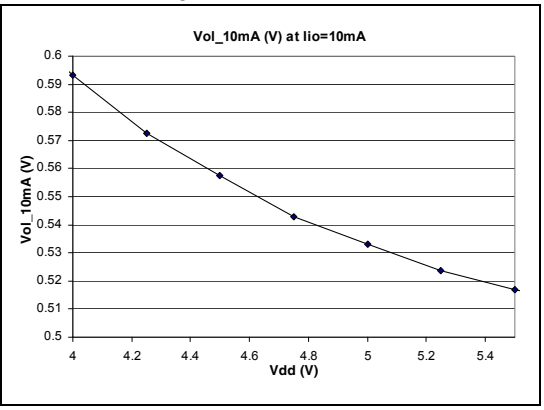


Figure 57. V_{OL} high sink vs. V_{DD}



16.9 Control pin characteristics

16.9.1 Asynchronous $\overline{\text{RESET}}$ pin

Subject to general operating conditions for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Table 72. RESET pin characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V_{IH}	Input high level voltage			$0.7xV_{DD}$		V_{DD}	V
V_{IL}	Input low voltage			V_{SS}		$0.3xV_{DD}$	V
V_{hys}	Schmitt trigger voltage hysteresis (1)				400		mV
V_{OL}	Output low level voltage (2)	V_{DD}=5V	I_{IO}=5 mA			0.8	V
			I_{IO}=7.5 mA			1.3	
R_{ON}	Weak pull-up equivalent resistor (3)	V_{IN}=V_{SS}	V_{DD}=5 V	50	80	100	kΩ
$t_{w(RSTL)out}$	Generated reset pulse duration	External pin or internal reset sources			6 30		$1/f_{SFOSC}$ µs
$t_{h(RSTL)in}$	External reset pulse hold time (4)			5			µs

1. Hysteresis voltage between Schmitt trigger switching levels. Based on characterization results, not tested.
2. The I_{IO} current sunk must always respect the absolute maximum rating specified in *Section 16.2* and the sum of I_{IO} (I/O ports and control pins) must not exceed I_{VSS}.
3. The R_{ON} pull-up equivalent resistor is based on a resistive transistor. This data is based on characterization results, not tested in production.
4. To guarantee the reset of the device, a minimum pulse has to be applied to $\overline{\text{RESET}}$ pin. All short pulses applied on $\overline{\text{RESET}}$ pin with a duration below $t_{h(RSTL)in}$ can be ignored.

Figure 66. USB: data signal rise and fall time

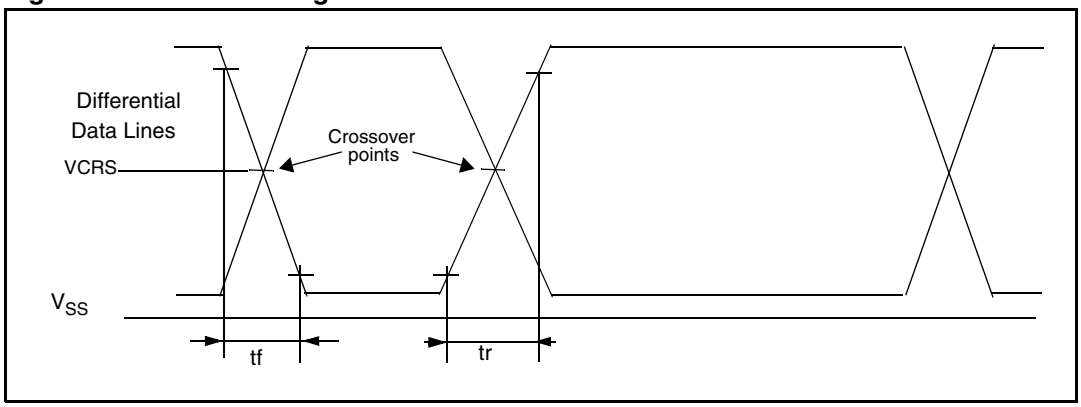


Table 74. USB: low-speed electrical characteristics

Symbol	Parameter	Conditions	Min	Max	Unit
	Driver characteristics:				
t_r	Rise time	CL=50 pF (1)	75		ns
		CL=600 pF (1)		300	ns
t_f	Fall Time	CL=50 pF (1)	75		ns
		CL=600 pF (1)		300	ns
t_{rfm}	Rise/ Fall Time matching	tr/tf	80	120	%
V_{CRS}	Output signal Crossover Voltage		1.3	2.0	V

1. For more detailed information, please refer to Chapter 7 (Electrical) of the USB specification (version 1.1).

16.9.3 SCI - serial communications interface

Subject to general operating condition for V_{DD}, f_{CPU}, and T_A unless otherwise specified.

Refer to I/O port characteristics for more details on the input/output alternate function characteristics (RDI and TDO).

Table 75. SCI characteristics

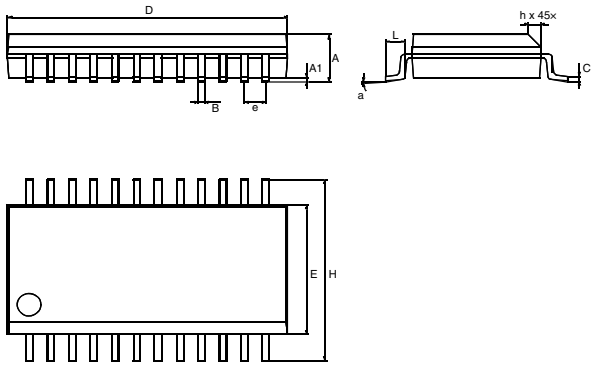
Symbol	Parameter	Conditions			Standard	Baud Rate	Unit
		f_{CPU}	Accuracy vs. Standard	Prescaler			
f_{Tx} f_{Rx}	Communication frequency	8 MHz	~0.16%	Conventional Mode TR (or RR)=128, PR=13 TR (or RR)= 32, PR=13 TR (or RR)= 16, PR=13 TR (or RR)= 8, PR=13 TR (or RR)= 4, PR=13 TR (or RR)= 16, PR= 3 TR (or RR)= 2, PR=13 TR (or RR)= 1, PR=13	 300 1200 2400 4800 9600 10400 19200 38400	 ~300.48 ~1201.92 ~2403.84 ~4807.69 ~9615.38 ~10416.67 ~19230.77 ~38461.54	Hz

17 Package characteristics

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

17.1 Package mechanical data

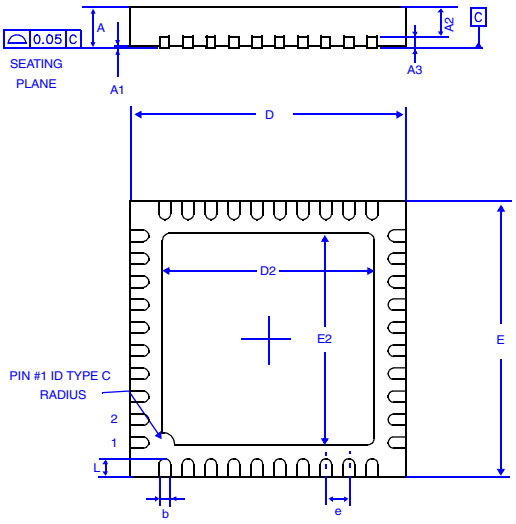
Figure 67. 24-pin plastic small outline package, 300-mil width



Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	2.35		2.65	0.0925		0.1043
A1	0.10		0.30	0.0039		0.0118
B	0.33		0.51	0.0130		0.0201
C	0.23		0.32	0.0091		0.0126
D	15.20		15.60	0.5984		0.6142
E	7.40		7.60	0.2913		0.2992
e		1.27			0.0500	
H	10.00		10.65	0.3937		0.4193
h	0.25		0.75	0.098		0.0295
α	0°		8°	0°		8°
L	0.40		1.27	0.0157		0.0500
	Number of Pins					
N	24					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 68. 40-lead very thin fine pitch quad flat no-lead package



Dim.	mm			inches(1)		
	Min	Typ	Max	Min	Typ	Max
A	0.80	0.90	1.00	0.0315	0.0354	0.0394
A1		0.02	0.05		0.0008	0.0020
A2		0.65	1.00		0.0256	0.0394
A3		0.20			0.0079	
b	0.18	0.25	0.30	0.0071	0.0098	0.0118
D	5.85	6.00	6.15	0.2303	0.2362	0.2421
D2	2.75	2.9	3.05	0.1083	0.1142	0.1201
E	5.85	6	6.15	0.2303	0.2362	0.2421
E2	2.75	2.9	3.05	0.1083	0.1142	0.1201
e		0.50			0.0197	
L	0.30	0.40	0.50	0.0118	0.0157	0.0197
	Number of Pins					
N	40					

1.Values in inches are converted from mm and rounded to 4 decimal digits.

ST7260 MICROCONTROLLER OPTION LIST
(Last update: January 2009)

Customer: . . . . . .
Address: . . . . . .
. . . . . .
Contact: . . . . . .
Phone No: . . . . . .
Reference: . . . . . .

FASTROM code must be sent in .S19 format.
Hex extension cannot be processed.
STMicroelectronics references:

Device Type/Memory Size/Package (check only one option):

FASTROM:	4K	8K
SO24:	[ ] ST72P60E1M1	[ ] ST72P60E2M1
QFN40:	[ ] ST72P60K1U1	[ ] ST72P60K2U1

Conditioning (check only one option):
Packaged Product

[ ] Tape & Reel (SO package only)
[ ] Tube

Special Marking: [ ] No [ ] Yes "_ _ _ _ _ _ _ _ _ _ _ _ _"
Authorized characters are letters, digits, '.', '-', '/' and spaces only.
For marking, one line is possible with a maximum of 13 characters.

Watchdog Selection: [ ] Software activation [ ] Hardware activation
Halt when Watchdog on: [ ] Reset [ ] No reset
LVD Reset * [ ] Disabled* [ ] Enabled*

Oscillator Selection: [ ] 24 MHz. [ ] 12 MHz.
Readout Protection: [ ] Disabled [ ] Enabled

Date . . . . . .

Signature . . . . . .
Please download the latest version of this option list from:
http://www.st.com/

19 Known limitations

19.1 PA2 limitation with OCMP1 enabled

Description

This limitation affects only Rev B Flash devices (with Internal Sales Type 72F60xxxxx$x7); it has been corrected in Rev W Flash devices (with Internal Sales Type 72F60xxxxx$x9).

Refer to *Figure 69 on page 137*.

When Output Compare 1 function (OCMP1) on pin PA6 is enabled by setting the OC1E bit in the TCR2 register, pin PA2 is also affected.

In particular, the PA2 pin is forced to be floating even if port configuration (PADDR+PADR) has set it as output low. However, it can be still used as an input.

19.2 Unexpected reset fetch

If an interrupt request occurs while a "POP CC" instruction is executed, the interrupt controller does not recognise the source of the interrupt and, by default, passes the RESET vector address to the CPU.

Workaround

To solve this issue, a "POP CC" instruction must always be preceded by a "SIM" instruction.

19.3 SCI wrong break duration

Description

A single break character is sent by setting and resetting the SBK bit in the SCICR2 register. In some cases, the break character may have a longer duration than expected:

- 20 bits instead of 10 bits if M=0
- 22 bits instead of 11 bits if M=1

In the same way, as long as the SBK bit is set, break characters are sent to the TDO pin. This may lead to generate one break more than expected.

Occurrence

The occurrence of the problem is random and proportional to the baudrate. With a transmit frequency of 19200 baud (f_{CPU}=8 MHz and SCIBRR=0xC9), the wrong break duration occurrence is around 1%.

Workaround

If this wrong duration is not compliant with the communication protocol in the application, software can request that an Idle line be generated before the break character. In this case, the break duration is always correct assuming the application is not doing anything between the idle and the break. This can be ensured by temporarily disabling interrupts.

The exact sequence is:

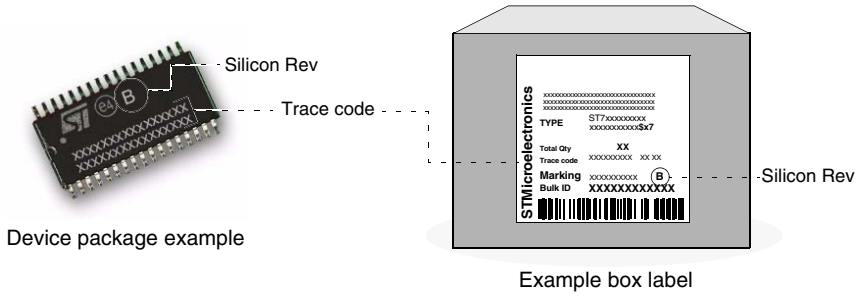
- Disable interrupts
- Reset and Set TE (IDLE request)
- Set and Reset SBK (Break Request)
- Re-enable interrupts

20 Device marking

The silicon revision can be identified either by Rev letter or obtained via a trace code. Follow the procedure below:

1. Identify the silicon revision letter from either the device package or the box label. For example, “**B**”, etc. Refer to *Figure 69*.
2. If the revision letter is not present, obtain the silicon revision by contacting your local ST office with the trace code information printed on either the box label or the device package.

Figure 69. Identifying silicon revision from device marking and box label



21 Revision history

Table 81. Document revision history

Date	Revision	Changes
13-Feb-2006	1	Initial release.
18-Oct-2006	2	Added known limitations section
05-Feb-2009	3	Added caution in *Section 7.1 on page 25* Added reference to watchdog reset pulse t_{DOG} in *Section 12.3 on page 44* Removed EMC protective circuitry in *Figure 65 on page 127* (device works correctly without these components) Modified notes below *Table 76: Package thermal characteristics on page 130* Replaced soldering information with ECOPACK reference in *Section 17 on page 129*