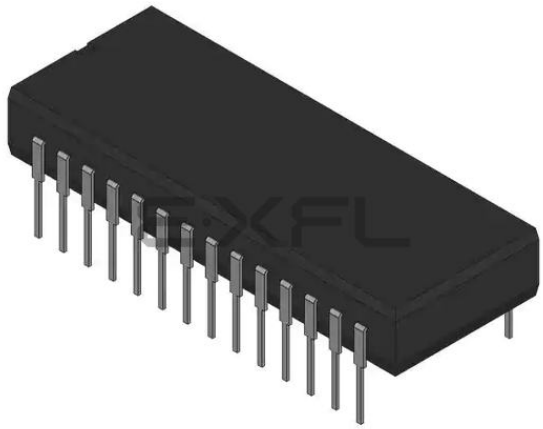

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Details	
Product Status	Obsolete
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	15
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc68hrc98jl3ecdw

Appendix C
MC68HC908KL3E/KK3E

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Chapter 1
General Description

1.1 Introduction

The MC68H(R)C908JL3E is a member of the low-cost, high-performance M68HC08 Family of 8-bit microcontroller units (MCUs). The M68HC08 Family is based on the customer-specified integrated circuit (CSIC) design strategy. All MCUs in the family use the enhanced M68HC08 central processor unit (CPU08) and are available with a variety of modules, memory sizes and types, and package types.

A list of MC68H(R)C908JL3E device variations is shown in Table 1-1.

Table 1-1. Summary of Device Variations

Device Type	Operating Voltage	LVI	ADC	Oscillator Option	Memory	Pin Count	Device
Flash	3V, 5V	Yes	Yes	XTAL	4,096 bytes Flash	28	MC68HC908JL3E
						20	MC68HC908JK3E
					1,536 bytes Flash	20	MC68HC908JK1E
				RC	4,096 bytes Flash	28	MC68HRC908JL3E
						20	MC68HRC908JK3E
					1,536 bytes Flash	20	MC68HRC908JK1E
Low Voltage Flash(1)	2.2 to 5.5V	No	Yes	XTAL	4,096 bytes Flash	28	MC68HLC908JL3E
						20	MC68HLC908JK3E
					1,536 bytes Flash	20	MC68HLC908JK1E
ROM(2)	3V, 5V	Yes	Yes	XTAL	4,096 bytes ROM	28	MC68HC08JL3E
						20	MC68HC08JK3E
				RC		28	MC68HRC08JL3E
						20	MC68HRC08JK3E
Flash, ADC-less(3)	3V, 5V	Yes	No	XTAL	4,096 bytes Flash	28	MC68HC908KL3E
						20	MC68HC908KK3E

1. Low-voltage Flash devices are documented in Appendix A MC68HLC908JL3E/JK3E/JK1E.
2. ROM devices are documented in Appendix B MC68H(R)C08JL3E/JK3E.
3. Flash, ADC-less devices are documented in Appendix C MC68HC908KL3E/KK3E.

All references to the MC68H(R)C908JL3E in this data book apply equally to the MC68H(R)C908JK3E and MC68H(R)C908JK1E, unless otherwise stated.

1.3 MCU Block Diagram

Figure 1-1 shows the structure of the MC68H(R)C908JL3E.

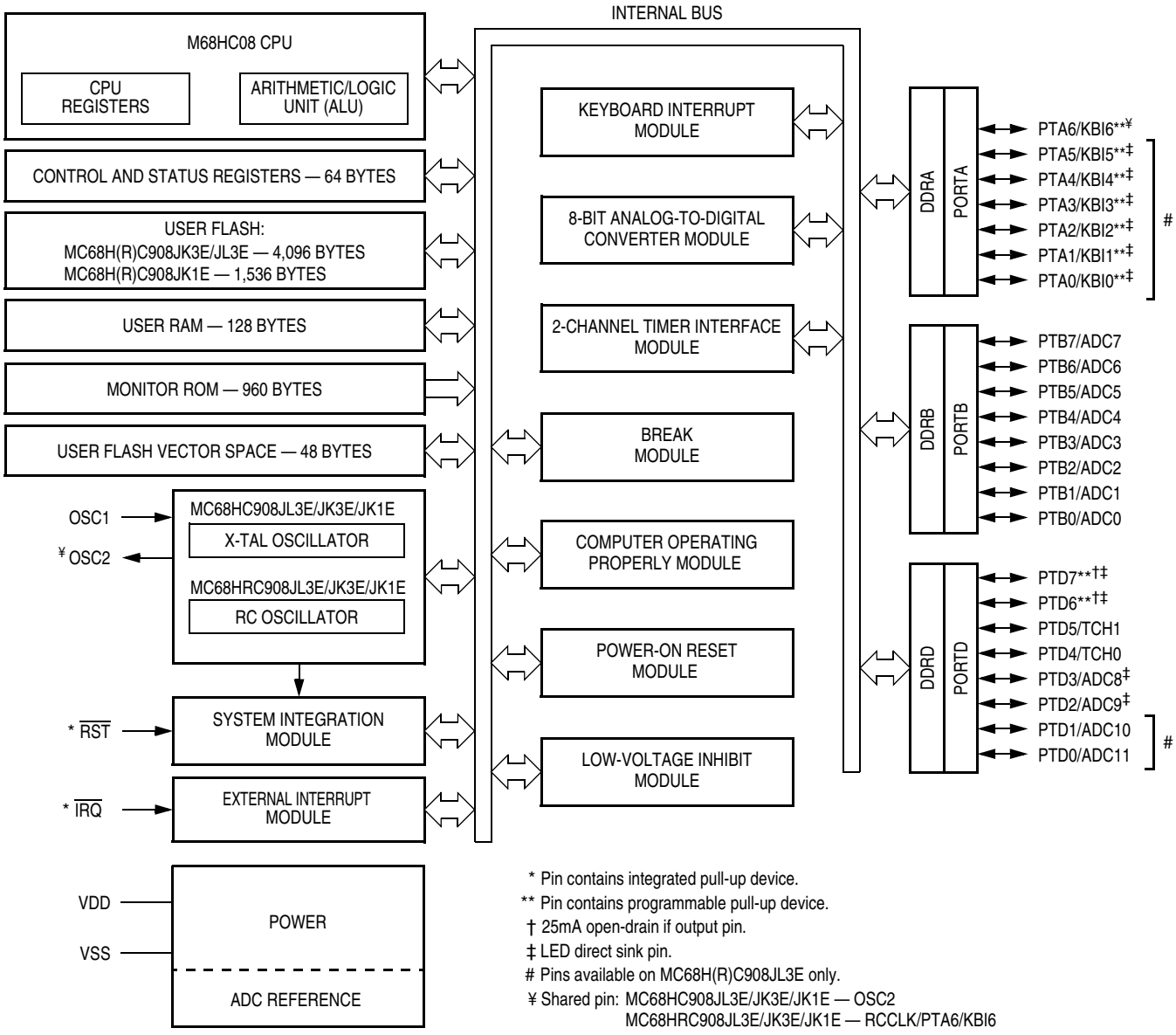


Figure 1-1. MCU Block Diagram

During a subroutine call, the CPU uses two bytes of the stack to store the return address. The stack pointer decrements during pushes and increments during pulls.

NOTE

Be careful when using nested subroutines. The CPU may overwrite data in the RAM during a subroutine or during the interrupt stacking operation.

2.5 Flash Memory

This sub-section describes the operation of the embedded Flash memory. The Flash memory can be read, programmed, and erased from a single external supply. The program and erase operations are enabled through the use of an internal charge pump.

Device	Flash Memory Size (Bytes)	Memory Address Range
MC68H(R)C908JL3E	4,096	$EC00—$FBFF
MC68H(R)C908JK3E	4,096	$EC00—$FBFF
MC68H(R)C908JK1E	1,536	$F600—$FBFF

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$FE08	Flash Control Register (FLCR)	Read:	0	0	0	0	HVEN	MASS	ERASE	PGM
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$FE09	Flash Block Protect Register (FLBPR)	Read:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 2-3. Flash I/O Register Summary

2.6 Functional Description

The Flash memory consists of an array of 4,096 or 1,536 bytes with an additional 48 bytes for user vectors. The minimum size of Flash memory that can be erased is 64 bytes (a page); and the maximum size of Flash memory that can be programmed in a program cycle is 32 bytes (a row). Program and erase operations are facilitated through control bits in the Flash Control Register (FLCR). Details for these operations appear later in this section. The address ranges for the user memory and vectors are:

- $EC00–$FBFF; user memory; 4,096 bytes; MC68H(R)C908JL3E/JK3E
  $F600–$FBFF; user memory; 1,536 bytes; MC68H(R)C908JK1E
- $FFD0–$FFFF; user interrupt vectors; 48 bytes

NOTE

An erased bit reads as 1 and a programmed bit reads as 0. A security feature prevents viewing of the Flash contents.[1]

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the Flash difficult for unauthorized users.

2.12 Flash Block Protect Register

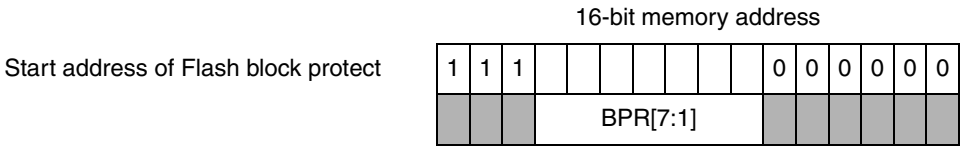
The Flash Block Protect Register is implemented as an 8-bit I/O register. The value in this register determines the starting address of the protected range within the Flash memory.

Address:	$FE09							
	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	BPR7	BPR6	BPR5	BPR4	BPR3	BPR2	BPR1	BPR0
Reset:	0	0	0	0	0	0	0	0

Figure 2-6. Flash Block Protect Register (FLBPR)

BPR[7:0] — Flash Block Protect Register Bit 7 to Bit 0

BPR[7:1] represent bits [12:6] of a 16-bit memory address. Bits [15:13] are 1's and bits [5:0] are 0's.



BPR0 is used only for BPR[7:0] = $FF, for no block protection.
The resultant 16-bit address is used for specifying the start address of the Flash memory for block protection. The Flash is protected from this start address to the end of Flash memory, at $FFFF. With this mechanism, the protect start address can be XX00, XX40, XX80, or XXC0 (at page boundaries — 64 bytes) within the Flash memory.

Examples of protect start address:

BPR[7:0]	Start of Address of Protect Range
$00–$60	The entire Flash memory is protected.
$62 or $63 (**0110 001x**)	$EC40 (111**0 1100 01**00 0000)
$64 or $65 (**0110 010x**)	$EC80 (111**0 1100 10**00 0000)
$68 or $69 (**0110 100x**)	$ED00 (111**0 1101 00**00 0000)
and so on...	
$DE or $DF (**1101 111x**)	$FBC0 (111**1 1011 11**00 0000)
$FE (**1111 1110**)	$FFC0 (111**1 1111 11**00 0000)
$FF	The entire Flash memory is not protected.

Note:
The end address of the protected range is always $FFFF.

Chapter 3
Configuration Registers (CONFIG)

3.1 Introduction

This section describes the configuration registers (CONFIG1 and CONFIG2). The configuration registers enables or disables the following options:

- Stop mode recovery time (32 × 2OSCOUT cycles or 4096 × 2OSCOUT cycles)
- STOP instruction
- Computer operating properly module (COP)
- COP reset period (COPRS), 8176 × 2OSCOUT or 262,128 × 2OSCOUT
- Enable LVI circuit
- Select LVI trip voltage

3.2 Functional Description

The configuration register is used in the initialization of various options. The configuration register can be written once after each reset. All of the configuration register bits are cleared during reset. Since the various options affect the operation of the MCU it is recommended that this register be written immediately after reset. The configuration register is located at $001E and $001F, and may be read at anytime.

NOTE

The CONFIG registers are one-time writable by the user after each reset. Upon a reset, the CONFIG registers default to predetermined settings as shown in Figure 3-1 and Figure 3-2.

3.3 Configuration Register 1 (CONFIG1)

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 3-1. Configuration Register 1 (CONFIG1)

COPRS — COP reset period selection bit

1 = COP reset cycle is 8176 × 2OSCOUT
0 = COP reset cycle is 262,128 × 2OSCOUT

5.3.2.5 LVI Reset

The low-voltage inhibit module (LVI) asserts its output to the SIM when the V_{DD} voltage falls to the LVI trip voltage V_{TRIP}. The LVI bit in the SIM reset status register (SRSR) is set, and the external reset pin (RSTB) is held low while the SIM counter counts out 4096 2OSCOUT cycles. Sixty-four 2OSCOUT cycles later, the CPU and memories are released from reset to allow the reset vector sequence to occur. The SIM actively pulls down the (RSTB) pin for all internal reset sources.

5.4 SIM Counter

The SIM counter is used by the power-on reset module (POR) and in stop mode recovery to allow the oscillator time to stabilize before enabling the internal bus (IBUS) clocks. The SIM counter also serves as a prescaler for the computer operating properly module (COP). The SIM counter uses 12 stages for counting, followed by a 13th stage that triggers a reset of SIM counters and supplies the clock for the COP module. The SIM counter is clocked by the falling edge of 2OSCOUT.

5.4.1 SIM Counter During Power-On Reset

The power-on reset module (POR) detects power applied to the MCU. At power-on, the POR circuit asserts the signal PORRST. Once the SIM is initialized, it enables the oscillator to drive the bus clock state machine.

5.4.2 SIM Counter During Stop Mode Recovery

The SIM counter also is used for stop mode recovery. The STOP instruction clears the SIM counter. After an interrupt, break, or reset, the SIM senses the state of the short stop recovery bit, SSREC, in the mask option register. If the SSREC bit is a one, then the stop recovery is reduced from the normal delay of 4096 2OSCOUT cycles down to 32 2OSCOUT cycles. This is ideal for applications using canned oscillators that do not require long start-up times from stop mode. External crystal applications should use the full stop recovery time, that is, with SSREC cleared in the configuration register (CONFIG).

5.4.3 SIM Counter and Reset States

External reset has no effect on the SIM counter. (See 5.6.2 Stop Mode for details.) The SIM counter is free-running after all reset states. (See 5.3.2 Active Resets from Internal Sources for counter control and internal reset recovery sequences.)

5.5 Exception Control

Normal, sequential program execution can be changed in three different ways:

- Interrupts
  - Maskable hardware CPU interrupts
  - Non-maskable software interrupt instruction (SWI)
- Reset
- Break interrupts

5.5.1 Interrupts

An interrupt temporarily changes the sequence of program execution to respond to a particular event. Figure 5-8 flow charts the handling of system interrupts.

8.4.1 TIM Counter Prescaler

The TIM clock source is one of the seven prescaler outputs. The prescaler generates seven clock rates from the internal bus clock. The prescaler select bits, PS[2:0], in the TIM status and control register (TSC) select the TIM clock source.

8.4.2 Input Capture

With the input capture function, the TIM can capture the time at which an external event occurs. When an active edge occurs on the pin of an input capture channel, the TIM latches the contents of the TIM counter into the TIM channel registers, TCHxH:TCHxL. The polarity of the active edge is programmable. Input captures can generate TIM CPU interrupt requests.

8.4.3 Output Compare

With the output compare function, the TIM can generate a periodic pulse with a programmable polarity, duration, and frequency. When the counter reaches the value in the registers of an output compare channel, the TIM can set, clear, or toggle the channel pin. Output compares can generate TIM CPU interrupt requests.

8.4.3.1 Unbuffered Output Compare

Any output compare channel can generate unbuffered output compare pulses as described in 8.4.3 Output Compare. The pulses are unbuffered because changing the output compare value requires writing the new value over the old value currently in the TIM channel registers.

An unsynchronized write to the TIM channel registers to change an output compare value could cause incorrect operation for up to two counter overflow periods. For example, writing a new value before the counter reaches the old value but after the counter reaches the new value prevents any compare during that counter overflow period. Also, using a TIM overflow interrupt routine to write a new, smaller output compare value may cause the compare to be missed. The TIM may pass the new value before it is written.

Use the following methods to synchronize unbuffered changes in the output compare value on channel x:

- When changing to a smaller value, enable channel x output compare interrupts and write the new value in the output compare interrupt routine. The output compare interrupt occurs at the end of the current output compare pulse. The interrupt routine has until the end of the counter overflow period to write the new value.
- When changing to a larger output compare value, enable TIM overflow interrupts and write the new value in the TIM overflow interrupt routine. The TIM overflow interrupt occurs at the end of the current counter overflow period. Writing a larger value in an output compare interrupt routine (at the end of the current pulse) could cause two output compares to occur in the same counter overflow period.

8.4.3.2 Buffered Output Compare

Channels 0 and 1 can be linked to form a buffered output compare channel whose output appears on the TCH0 pin. The TIM channel registers of the linked pair alternately control the output.

Setting the MS0B bit in TIM channel 0 status and control register (TSC0) links channel 0 and channel 1. The output compare value in the TIM channel 0 registers initially controls the output on the TCH0 pin. Writing to the TIM channel 1 registers enables the TIM channel 1 registers to synchronously control the output after the TIM overflows. At each subsequent overflow, the TIM channel registers (0 or 1) that

TOVx — Toggle-On-Overflow Bit

When channel x is an output compare channel, this read/write bit controls the behavior of the channel x output when the TIM counter overflows. When channel x is an input capture channel, TOVx has no effect. Reset clears the TOVx bit.

1 = Channel x pin toggles on TIM counter overflow.
0 = Channel x pin does not toggle on TIM counter overflow.

NOTE

When TOVx is set, a TIM counter overflow takes precedence over a channel x output compare if both occur at the same time.

CHxMAX — Channel x Maximum Duty Cycle Bit

When the TOVx bit is at one, setting the CHxMAX bit forces the duty cycle of buffered and unbuffered PWM signals to 100%. As Figure 8-8 shows, the CHxMAX bit takes effect in the cycle after it is set or cleared. The output stays at the 100% duty cycle level until the cycle after CHxMAX is cleared.

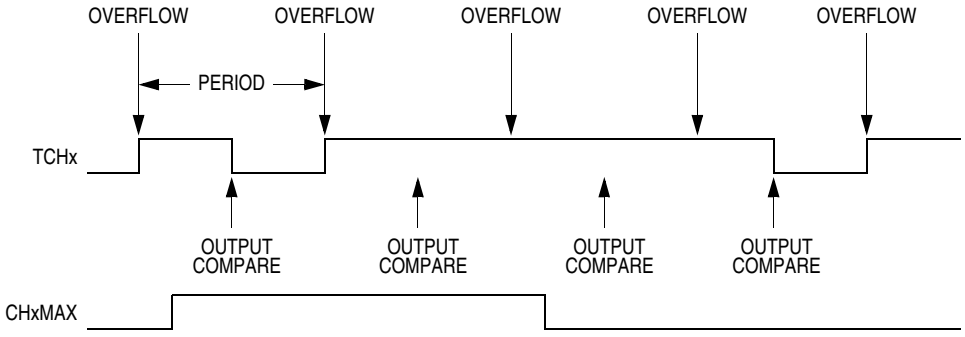


Figure 8-8. CHxMAX Latency

Chapter 9
Analog-to-Digital Converter (ADC)

9.1 Introduction

This section describes the 12-channel, 8-bit linear successive approximation analog-to-digital converter (ADC).

9.2 Features

Features of the ADC module include:

- 12 channels with multiplexed input
- Linear successive approximation with monotonicity
- 8-bit resolution
- Single or continuous conversion
- Conversion complete flag or conversion complete interrupt
- Selectable ADC clock

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$003C	ADC Status and Control Register (ADSCR)	Read:	COCO	AIEN	ADCO	ADCH4	ADCH3	ADCH2	ADCH1	ADCH0
		Write:								
		Reset:	0	0	0	1	1	1	1	1
$003D	ADC Data Register (ADR)	Read:	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0
		Write:								
		Reset:	Indeterminate after reset							
$003E	ADC Input Clock Register (ADICLK)	Read:	ADIV2	ADIV1	ADIV0	0	0	0	0	0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 9-1. ADC I/O Register Summary

9.3 Functional Description

Twelve ADC channels are available for sampling external sources at pins PTB0–PTB7 and PTD0–PTD3. An analog multiplexer allows the single ADC converter to select one of the 12 ADC channels as ADC voltage input (ADCVIN). ADCVIN is converted by the successive approximation register-based counters. The ADC resolution is 8 bits. When the conversion is completed, ADC puts the result in the ADC data register and sets a flag or generates an interrupt. Figure 9-2 shows a block diagram of the ADC.

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$000A	Port D Control Register (PDCR)	Read:	0	0	0	0	SLOWD7	SLOWD6	PTDPU7	PTDPU6
		Write:								
		Reset:	0	0	0	0	0	0	0	0
$000D	Port A Input Pull-up Enable Register (PTAPUE)	Read:	PTA6EN	PTAPUE6	PTAPUE5	PTAPUE4	PTAPUE3	PTAPUE2	PTAPUE1	PTAPUE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-1. I/O Port Register Summary

Table 10-1. Port Control Register Bits Summary

Port	Bit	DDR	Module Control			Pin
			Module	Register	Control Bit	
A	0	DDRA0	KBI	KBIER ($001B)	KBIE0	PTA0/KBI0
	1	DDRA1			KBIE1	PTA1/KBI1
	2	DDRA2			KBIE2	PTA2/KBI2
	3	DDRA3			KBIE3	PTA3/KBI3
	4	DDRA4			KBIE4	PTA4/KBI4
	5	DDRA5			KBIE5	PTA5/KBI5
	6	DDRA6	OSC KBI	PTAPUE ($000D) KBIER ($001B)	PTA6EN KBIE6	RCCLK/PTA6/KBI6[1]
B	0	DDRB0	ADC	ADSCR ($003C)	ADCH[4:0]	PTB0/ADC0
	1	DDRB1				PTB1/ADC1
	2	DDRB2				PTB2/ADC2
	3	DDRB3				PTB3/ADC3
	4	DDRB4				PTB4/ADC4
	5	DDRB5				PTB5/ADC5
	6	DDRB6				PTB6/ADC6
	7	DDRB7				PTB7/ADC7
D	0	DDRD0	ADC	ADSCR ($003C)	ADCH[4:0]	PTD0/ADC11
	1	DDRD1				PTD1/ADC10
	2	DDRD2				PTD2/ADC9
	3	DDRD3				PTD3/ADC8
	4	DDRD4	TIM	TSC0 ($0025)	ELS0B:ELS0A	PTD4/TCH0
	5	DDRD5		TSC1 ($0028)	ELS1B:ELS1A	PTD5/TCH1
	6	DDRD6	—	—	—	PTD6
	7	DDRD7	—	—	—	PTD7

1. RCCLK/PTA6/KBI6 pin is only available on MC68HRC908JL3E/JK3E/JK1E devices (RC option); PTAPUE register has priority control over the port pin. RCCLK/PTA6/KBI6 is the OSC2 pin on MC68HC908JL3E/JK3E/JK1E devices (X-TAL option).

10.3 Port B

Port B is an 8-bit special function port that shares all eight of its port pins with the analog-to-digital converter (ADC) module, see Chapter 9 Analog-to-Digital Converter (ADC).

10.3.1 Port B Data Register (PTB)

The port B data register contains a data latch for each of the eight port B pins.

Address: $0001

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	PTB7	PTB6	PTB5	PTB4	PTB3	PTB2	PTB1	PTB0
Reset:	Unaffected by reset							
Alternative Function:	ADC7	ADC6	AD4C5	ADC4	ADC3	ADC2	ADC2	ADC0

Figure 10-6. Port B Data Register (PTB)

PTB[7:0] — Port B Data Bits

These read/write bits are software programmable. Data direction of each port B pin is under the control of the corresponding bit in data direction register B. Reset has no effect on port B data.

ADC[7:0] — ADC channels 7 to 0

ADC[7:0] are pins used for the input channels to the analog-to-digital converter module. The channel select bits, ADCH[4:0], in the ADC status and control register define which port pin will be used as an ADC input and overrides any control from the port I/O logic. See Chapter 9 Analog-to-Digital Converter (ADC).

10.3.2 Data Direction Register B (DDRB)

Data direction register B determines whether each port B pin is an input or an output. Writing a one to a DDRB bit enables the output buffer for the corresponding port B pin; a zero disables the output buffer.

Address: $0005

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	DDRB7	DDRB6	DDRB5	DDRB4	DDRB3	DDRB2	DDRB1	DDRB0
Reset:	0	0	0	0	0	0	0	0

Figure 10-7. Data Direction Register B (DDRB)

DDRB[7:0] — Data Direction Register B Bits

These read/write bits control port B data direction. Reset clears DDRB[7:0], configuring all port B pins as inputs.

1 = Corresponding port B pin configured as output
0 = Corresponding port B pin configured as input

NOTE

Avoid glitches on port B pins by writing to the port B data register before changing data direction register B bits from 0 to 1.

The vector fetch or software clear may occur before or after the interrupt pin returns to one. As long as the pin is low, the interrupt request remains pending. A reset will clear the latch and the MODE control bit, thereby clearing the interrupt even if the pin stays low.

When set, the IMASK bit in the INTSCR mask all external interrupt requests. A latched interrupt request is not presented to the interrupt priority logic unless the IMASK bit is clear.

NOTE

The interrupt mask (I) in the condition code register (CCR) masks all interrupt requests, including external interrupt requests. See 5.5 Exception Control.

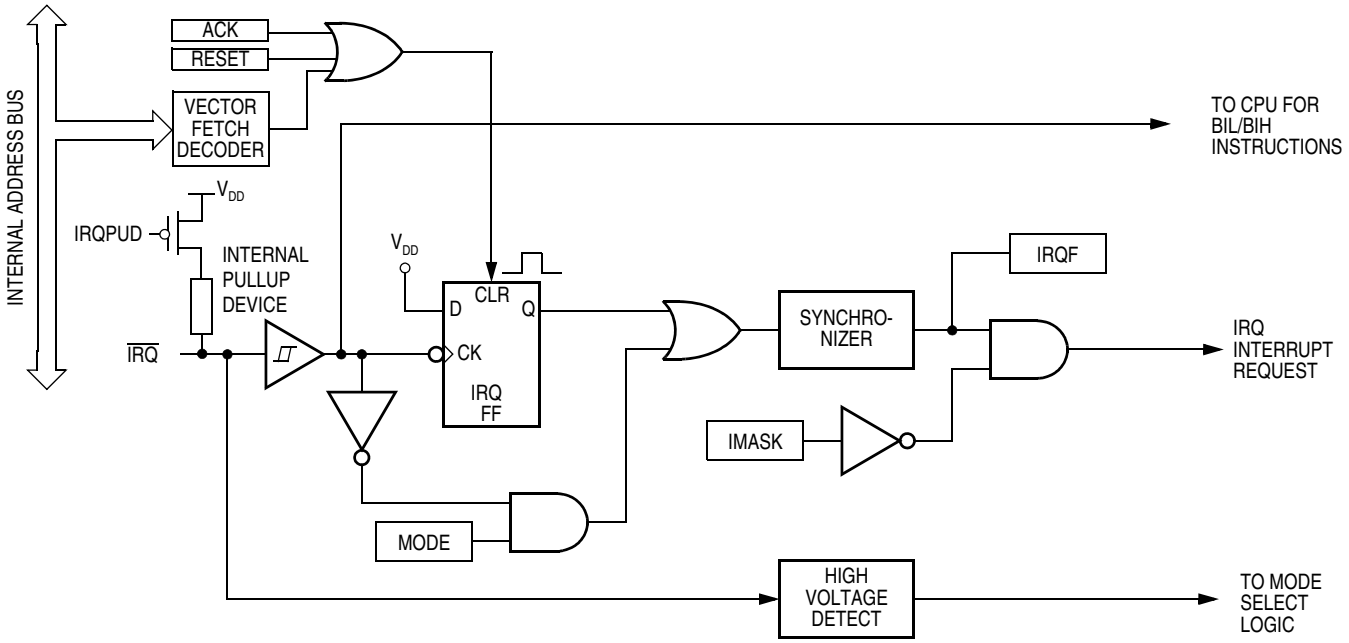


Figure 11-1. IRQ Module Block Diagram

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001D	IRQ Status and Control Register (INTSCR)	Read:	0	0	0	0	IRQF	0	IMASK	MODE
		Write:						ACK		
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 11-2. IRQ I/O Register Summary

Chapter 12
Keyboard Interrupt Module (KBI)

12.1 Introduction

The keyboard interrupt module (KBI) provides seven independently maskable external interrupts which are accessible via PTA0–PTA6 pins.

12.2 Features

Features of the keyboard interrupt module include the following:

- Seven keyboard interrupt pins with separate keyboard interrupt enable bits and one keyboard interrupt mask
- Software configurable pull-up device if input pin is configured as input port bit
- Programmable edge-only or edge- and level- interrupt sensitivity
- Exit from low-power modes

Addr.	Register Name		Bit 7	6	5	4	3	2	1	Bit 0
$001A	Keyboard Status and Control Register (KBSCR)	Read:	0	0	0	0	KEYF	0	IMASKK	MODEK
		Write:						ACKK		
		Reset:	0	0	0	0	0	0	0	0
$001B	Keyboard Interrupt Enable Register (KBIER)	Read:	0	KBIE6	KBIE5	KBIE4	KBIE3	KBIE2	KBIE1	KBIE0
		Write:								
		Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 12-1. KBI I/O Register Summary

12.3 I/O Pins

The seven keyboard interrupt pins are shared with standard port I/O pins. The full name of the KBI pins are listed in Table 12-1. The generic pin name appear in the text that follows.

Table 12-1. Pin Name Conventions

KBI Generic Pin Name	Full MCU Pin Name	Pin Selected for KBI Function by KBIEx Bit in KBIER
KBI0–KBI5	PTA0/KBI0–PTA5/KBI5	KBIE0–KBIE5
KBI6	RCCLK/PTA6/KBI6(1)	KBIE6

1. RCCLK/PTA6/KBI6 pin is only available on MC68HRC908JL3E/JK3E/JK1E devices (RC option).

13.3.7 COPRS (COP Rate Select)

The COPRS signal reflects the state of the COP rate select bit (COPRS) in the configuration register 1.

Address: $001F

	Bit 7	6	5	4	3	2	1	Bit 0
Read: / Write:	COPRS	R	R	LVID	R	SSREC	STOP	COPD
Reset:	0	0	0	0	0	0	0	0

R = Reserved

Figure 13-2. Configuration Register 1 (CONFIG1)

COPRS — COP Rate Select Bit

COPRS selects the COP timeout period. Reset clears COPRS.

1 = COP timeout period is 8176 × 2OSCOUT cycles

0 = COP timeout period is 262,128 × 2OSCOUT cycles

COPD — COP Disable Bit

COPD disables the COP module.

1 = COP module disabled

0 = COP module enabled

13.4 COP Control Register

The COP control register is located at address $FFFF and overlaps the reset vector. Writing any value to $FFFF clears the COP counter and starts a new timeout period. Reading location $FFFF returns the low byte of the reset vector.

Address: $FFFF

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	Low byte of reset vector							
Write:	Clear COP counter							
Reset:	Unaffected by reset							

Figure 13-3. COP Control Register (COPCTL)

13.5 Interrupts

The COP does not generate CPU interrupt requests.

13.6 Monitor Mode

The COP is disabled in monitor mode when V_{TST} is present on the $\overline{IRQ}$ pin or on the $\overline{RST}$ pin.

13.7 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power consumption standby modes.

15.4 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

15.4.1 Break Status and Control Register (BRKSCR)

The break status and control register contains break module enable and status bits.

Address: $FE0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a zero to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a one to BRKA generates a break interrupt. Clear BRKA by writing a zero to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match
0 = No break address match

A.5.5 ADC Characteristics

Table A-5. ADC Characteristics

Characteristic	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDAD}	2.2 (V_{DD} min)	5.5 (V_{DD} max)	V	
Input voltages	V_{ADIN}	V_{SS}	V_{DD}	V	
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy	A_{AD}	± 0.5	± 2	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.5	1.048	MHz	$t_{AIC} = 1/f_{ADIC}$, tested only at 1 MHz
Conversion range	R_{AD}	V_{SS}	V_{DD}	V	
Power-up time	t_{ADPU}	14	—	t_{AIC} cycles	
Conversion time	t_{ADC}	14	15	t_{AIC} cycles	
Sample time[1]	t_{ADS}	5	—	t_{AIC} cycles	
Zero input reading[2]	Z_{ADI}	00	01	Hex	$V_{IN} = V_{SS}$
Full-scale reading[3]	F_{ADI}	FE	FF	Hex	$V_{IN} = V_{DD}$
Input capacitance	C_{ADI}	—	(20) 8	pF	Not tested
Input leakage[3] Port B/port D	—	—	± 1	μA	

1. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
2. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
3. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

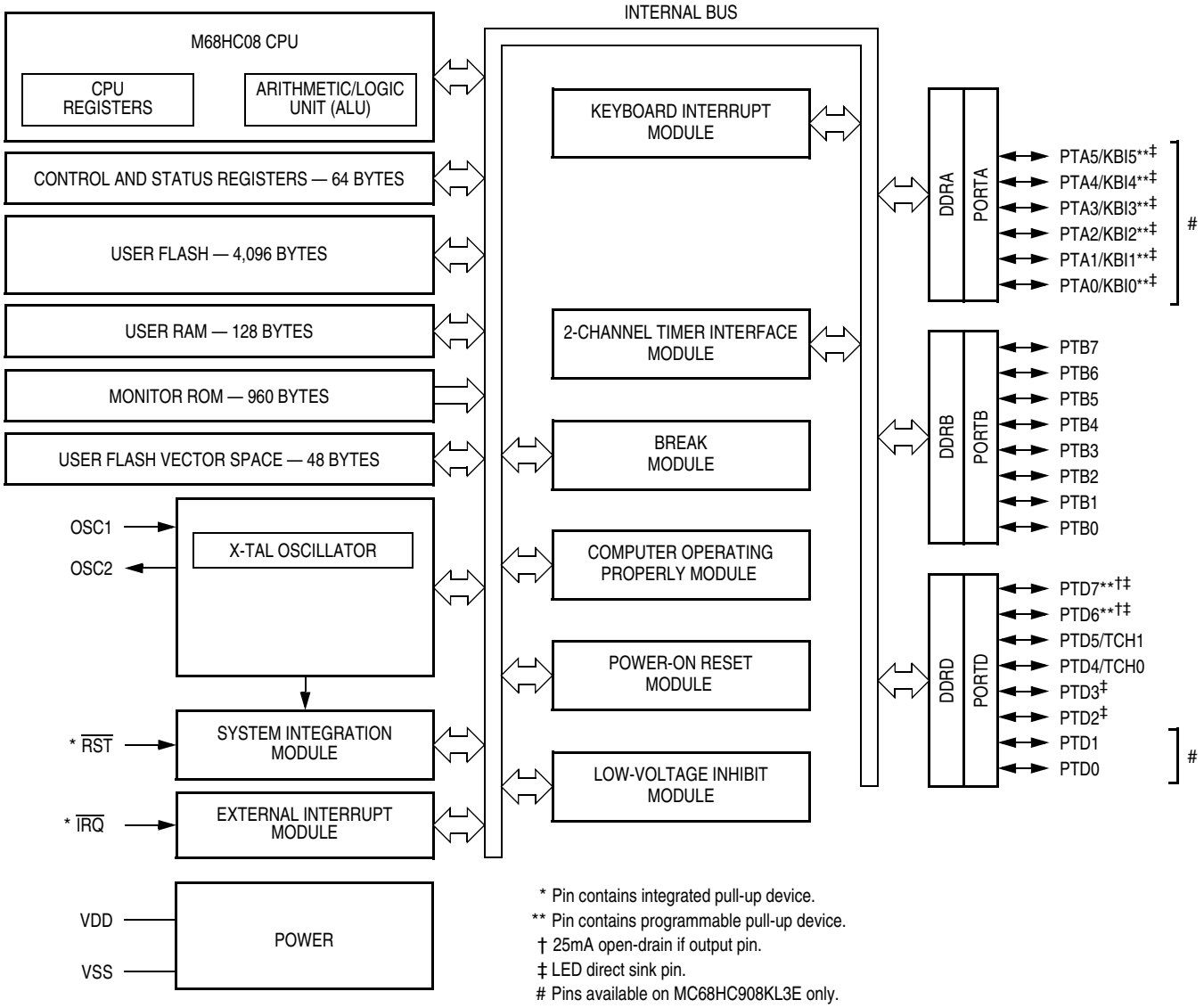


Figure C-1. MC68HC908KL3E/KK3E Block Diagram