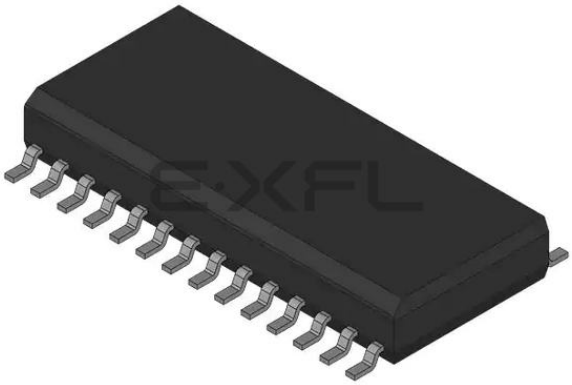

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Details	
Product Status	Active
Core Processor	HC08
Core Size	8-Bit
Speed	8MHz
Connectivity	-
Peripherals	LED, LVD, POR, PWM
Number of I/O	23
Program Memory Size	4KB (4K x 8)
Program Memory Type	FLASH
EEPROM Size	-
RAM Size	128 x 8
Voltage - Supply (Vcc/Vdd)	2.7V ~ 3.3V
Data Converters	A/D 12x8b
Oscillator Type	External
Operating Temperature	-40°C ~ 85°C (TA)
Mounting Type	Surface Mount
Package / Case	28-SOIC (0.295", 7.50mm Width)
Supplier Device Package	28-SOIC
Purchase URL	https://www.e-xfl.com/pro/item?MUrl=&PartUrl=mc908jl3ecdwer

Appendix C
MC68HC908KL3E/KK3E

1.2 Features

Features of the MC68H(R)C908JL3E include the following:

- EMC enhanced version of MC68H(R)C908JL3/JK3/JK1
- High-performance M68HC08 architecture
- Fully upward-compatible object code with M6805, M146805, and M68HC05 Families
- Low-power design; fully static with stop and wait modes
- Maximum internal bus frequency:
  - 8-MHz at 5V operating voltage
  - 4-MHz at 3V operating voltage
- Oscillator options:
  - Crystal oscillator for MC68HC908JL3E/JK3E/JK1E
  - RC oscillator for MC68HRC908JL3E/JK3E/JK1E
- User program Flash memory with security[1] feature
  - 4,096 bytes for MC68H(R)C908JL3E/JK3E
  - 1,536 bytes for MC68H(R)C908JK1E
- 128 bytes of on-chip RAM
- 2-channel, 16-bit timer interface module (TIM)
- 12-channel, 8-bit analog-to-digital converter (ADC)
- 23 general purpose I/O ports for MC68H(R)C908JL3E:
  - 7 keyboard interrupt with internal pull-up
    (6 keyboard interrupt for MC68HC908JL3E)
  - 10 LED drivers (sink)
  - 2 × 25mA open-drain I/O with pull-up
- 15 general purpose I/O ports for MC68H(R)C908JK3E/JK1E:
  - 1 keyboard interrupt with internal pull-up
    (MC68HRC908JK3E/JK1E only)
  - 4 LED drivers (sink)
  - 2 × 25mA open-drain I/O with pull-up
  - 10-channel ADC
- System protection features:
  - Optional computer operating properly (COP) reset
  - Optional low-voltage detection with reset and selectable trip points for 3V and 5V operation
  - Illegal opcode detection with reset
  - Illegal address detection with reset
- Master reset pin with internal pull-up and power-on reset
- $\overline{\text{IRQ}}$ with schmitt-trigger input and programmable pull-up
- 28-pin PDIP, 28-pin SOIC, and 48-pin LQFP packages for MC68H(R)C908JL3E
- 20-pin PDIP and 20-pin SOIC packages for MC68H(R)C908JK3E/JK1E

1. No security feature is absolutely secure. However, Freescale's strategy is to make reading or copying the Flash difficult for unauthorized users.

1.5 Pin Functions

Description of the pin functions are provided in Table 1-2.

Table 1-2. Pin Functions

PIN NAME	PIN DESCRIPTION	IN/OUT	VOLTAGE LEVEL
$V_{DDJL3JL3}$	Power supply.	In	5V or 3V
V_{SS}	Power supply ground	Out	0V
$\overline{RST}$	RESET input, active low. With Internal pull-up and Schmitt trigger input.	Input	V_{DD} to V_{TST}
$\overline{IRQ}$	External IRQ pin. With software programmable internal pull-up and schmitt trigger input. This pin is also used for mode entry selection.	Input	V_{DD} to V_{TST}
OSC1	X-tal or RC oscillator input.	In	Analog
OSC2	MC68HC908JL3E/JK3E/JK1E: X-tal oscillator output, this is the inverting OSC1 signal.	Out	Analog
	MC68HRC908JL3E/JK3E/JK1E: Default is RC oscillator clock output, RCCLK. Shared with PTA6/KBI6, with programmable pull-up.	In/Out	V_{DD}
PTA[0:6]	7-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 7 keyboard interrupts KBI[0:6].	In	V_{DD}
	Each pin has programmable internal pull-up device.	In	V_{DD}
	PTA[0:5] have LED direct sink capability	In	V_{SS}
PTB[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	Shared with 8 ADC inputs, ADC[0:7].	In	Analog
PTD[0:7]	8-bit general purpose I/O port.	In/Out	V_{DD}
	PTD[3:0] shared with 4 ADC inputs, ADC[8:11].	Input	Analog
	PTD[4:5] shared with TIM channels, TCH0 and TCH1.	In/Out	V_{DD}
	PTD[2:3], PTD[6:7] have LED direct sink capability	In	V_{SS}
	PTD[6:7] can be configured as 25mA open-drain output with pull-up.	In/Out	V_{DD}

NOTE

On the MC68H(R)C908JK3E/JK1E, the following pins are not available: PTA0, PTA1, PTA2, PTA3, PTA4, PTA5, PTD0, and PTD1.

Table 2-1. Vector Addresses

Vector Priority	INT Flag	Address	Vector
Lowest ↕ Highest	—	$FFD0 ↓ $FFDD	Not Used
	IF15	$FFDE	ADC Conversion Complete Vector (High)
		$FFDF	ADC Conversion Complete Vector (Low)
	IF14	$FFE0	Keyboard Vector (High)
		$FFE1	Keyboard Vector (Low)
	IF13 ↓ IF6	—	Not Used
	IF5	$FFF2	TIM Overflow Vector (High)
		$FFF3	TIM Overflow Vector (Low)
	IF4	$FFF4	TIM Channel 1 Vector (High)
		$FFF5	TIM Channel 1 Vector (Low)
	IF3	$FFF6	TIM Channel 0 Vector (High)
		$FFF7	TIM Channel 0 Vector (Low)
	IF2	—	Not Used
	IF1	$FFFA	$\overline{\text{IRQ}}$ Vector (High)
		$FFFB	$\overline{\text{IRQ}}$ Vector (Low)
	—	$FFFC	SWI Vector (High)
		$FFFD	SWI Vector (Low)
	—	$FFFE	Reset Vector (High)
		$FFFF	Reset Vector (Low)

2.4 Random-Access Memory (RAM)

Addresses $0080 through $00FF are RAM locations. The location of the stack RAM is programmable. The 16-bit stack pointer allows the stack to be anywhere in the 64-Kbyte memory space.

NOTE

For correct operation, the stack pointer must point only to RAM locations.

Within page zero are 128 bytes of RAM. Because the location of the stack RAM is programmable, all page zero RAM locations can be used for I/O control and user data or code. When the stack pointer is moved from its reset location at $00FF, direct addressing mode instructions can access efficiently all page zero RAM locations. Page zero RAM, therefore, provides ideal locations for frequently accessed global variables.

Before processing an interrupt, the CPU uses five bytes of the stack to save the contents of the CPU registers.

NOTE

For M6805 compatibility, the H register is not stacked.

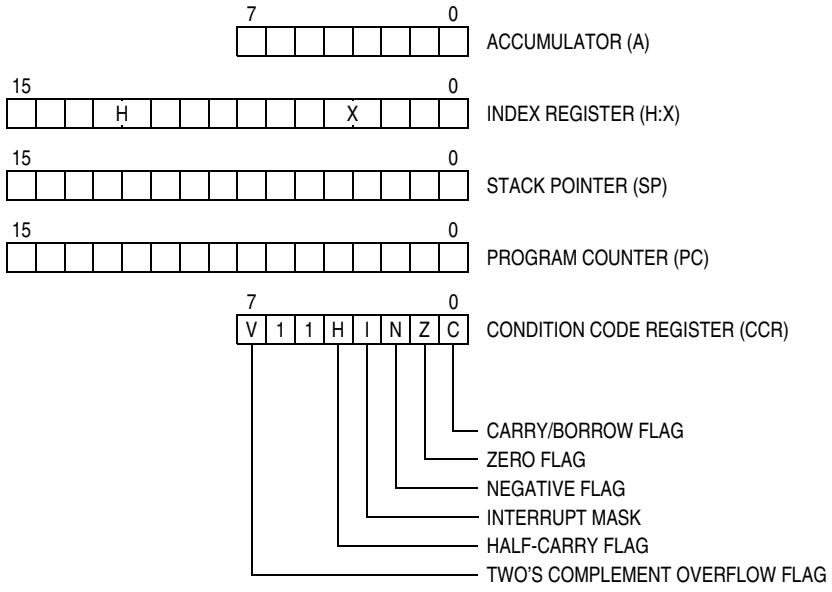


Figure 4-1. CPU Registers

4.3.1 Accumulator

The accumulator is a general-purpose 8-bit register. The CPU uses the accumulator to hold operands and the results of arithmetic/logic operations.

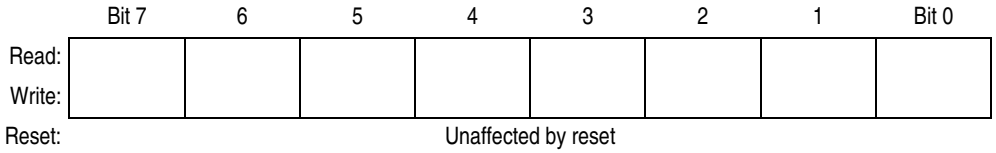


Figure 4-2. Accumulator (A)

4.3.2 Index Register

The 16-bit index register allows indexed addressing of a 64-Kbyte memory space. H is the upper byte of the index register, and X is the lower byte. H:X is the concatenated 16-bit index register.

In the indexed addressing modes, the CPU uses the contents of the index register to determine the conditional address of the operand.

The index register can serve also as a temporary data storage location.

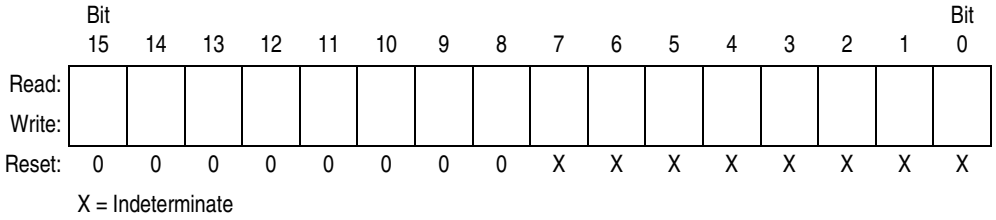


Figure 4-3. Index Register (H:X)

4.3.5 Condition Code Register

The 8-bit condition code register contains the interrupt mask and five flags that indicate the results of the instruction just executed. Bits 6 and 5 are set permanently to 1. The following paragraphs describe the functions of the condition code register.

	Bit 7	6	5	4	3	2	1	Bit 0
Read: Write:	V	1	1	H	I	N	Z	C
Reset:	X	1	1	X	1	X	X	X

X = Indeterminate

Figure 4-6. Condition Code Register (CCR)

V — Overflow Flag

The CPU sets the overflow flag when a two's complement overflow occurs. The signed branch instructions BGT, BGE, BLE, and BLT use the overflow flag.

1 = Overflow
0 = No overflow

H — Half-Carry Flag

The CPU sets the half-carry flag when a carry occurs between accumulator bits 3 and 4 during an add-without-carry (ADD) or add-with-carry (ADC) operation. The half-carry flag is required for binary-coded decimal (BCD) arithmetic operations. The DAA instruction uses the states of the H and C flags to determine the appropriate correction factor.

1 = Carry between bits 3 and 4
0 = No carry between bits 3 and 4

I — Interrupt Mask

When the interrupt mask is set, all maskable CPU interrupts are disabled. CPU interrupts are enabled when the interrupt mask is cleared. When a CPU interrupt occurs, the interrupt mask is set automatically after the CPU registers are saved on the stack, but before the interrupt vector is fetched.

1 = Interrupts disabled
0 = Interrupts enabled

NOTE

To maintain M6805 Family compatibility, the upper byte of the index register (H) is not stacked automatically. If the interrupt service routine modifies H, then the user must stack and unstack H using the PSHH and PULH instructions.

After the I bit is cleared, the highest-priority interrupt request is serviced first.

A return-from-interrupt (RTI) instruction pulls the CPU registers from the stack and restores the interrupt mask from the stack. After any reset, the interrupt mask is set and can be cleared only by the clear interrupt mask software instruction (CLI).

N — Negative Flag

The CPU sets the negative flag when an arithmetic operation, logic operation, or data manipulation produces a negative result, setting bit 7 of the result.

1 = Negative result
0 = Non-negative result

Table 4-1. Instruction Set Summary (Sheet 3 of 6)

Source Form	Operation	Description	Effect on CCR						Address Mode	Opcode	Operand	Cycles
			V	H	I	N	Z	C				
CLR *opr* CLRA CLRX CLRH CLR *opr*,X CLR ,X CLR *opr*,SP	Clear	M ← $00 A ← $00 X ← $00 H ← $00 M ← $00 M ← $00 M ← $00	0	–	–	0	1	–	DIR INH INH INH IX1 IX SP1	3F 4F 5F 8C 6F 7F 9E6F	dd ff ff	3 1 1 1 3 2 4
CMP #*opr* CMP *opr* CMP *opr* CMP *opr*,X CMP *opr*,X CMP ,X CMP *opr*,SP CMP *opr*,SP	Compare A with M	(A) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A1 B1 C1 D1 E1 F1 9EE1 9ED1	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
COM *opr* COMA COMX COM *opr*,X COM ,X COM *opr*,SP	Complement (One's Complement)	M ← ($\overline{M}$) = $FF – (M) A ← ($\overline{A}$) = $FF – (M) X ← ($\overline{X}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M) M ← ($\overline{M}$) = $FF – (M)	0	–	–	↕	↕	1	DIR INH INH IX1 IX SP1	33 43 53 63 73 9E63	dd ff ff	4 1 1 4 3 5
CPHX #*opr* CPHX *opr*	Compare H:X with M	(H:X) – (M:M + 1)	↕	–	–	↕	↕	↕	IMM DIR	65 75	ii ii+1 dd	3 4
CPX #*opr* CPX *opr* CPX *opr* CPX ,X CPX *opr*,X CPX *opr*,X CPX *opr*,SP CPX *opr*,SP	Compare X with M	(X) – (M)	↕	–	–	↕	↕	↕	IMM DIR EXT IX2 IX1 IX SP1 SP2	A3 B3 C3 D3 E3 F3 9EE3 9ED3	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
DAA	Decimal Adjust A	$(A)_{10}$	U	–	–	↕	↕	↕	INH	72		2
DBNZ *opr,rel* DBNZA *rel* DBNZX *rel* DBNZ *opr*,X,*rel* DBNZ X,*rel* DBNZ *opr*,SP,*rel*	Decrement and Branch if Not Zero	A ← (A) – 1 or M ← (M) – 1 or X ← (X) – 1 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 3 + *rel* ? (result) ≠ 0 PC ← (PC) + 2 + *rel* ? (result) ≠ 0 PC ← (PC) + 4 + *rel* ? (result) ≠ 0	–	–	–	–	–	–	DIR INH INH IX1 IX SP1	3B 4B 5B 6B 7B 9E6B	dd rr rr rr ff rr rr ff rr	5 3 3 5 4 6
DEC *opr* DECA DECX DEC *opr*,X DEC ,X DEC *opr*,SP	Decrement	M ← (M) – 1 A ← (A) – 1 X ← (X) – 1 M ← (M) – 1 M ← (M) – 1 M ← (M) – 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3A 4A 5A 6A 7A 9E6A	dd ff ff	4 1 1 4 3 5
DIV	Divide	A ← (H:A)/(X) H ← Remainder	–	–	–	–	↕	↕	INH	52		7
EOR #*opr* EOR *opr* EOR *opr* EOR *opr*,X EOR *opr*,X EOR ,X EOR *opr*,SP EOR *opr*,SP	Exclusive OR M with A	A ← (A ⊕ M)	0	–	–	↕	↕	–	IMM DIR EXT IX2 IX1 IX SP1 SP2	A8 B8 C8 D8 E8 F8 9EE8 9ED8	ii dd hh ll ee ff ff ff ee ff	2 3 4 4 3 2 4 5
INC *opr* INCA INCX INC *opr*,X INC ,X INC *opr*,SP	Increment	M ← (M) + 1 A ← (A) + 1 X ← (X) + 1 M ← (M) + 1 M ← (M) + 1 M ← (M) + 1	↕	–	–	↕	↕	–	DIR INH INH IX1 IX SP1	3C 4C 5C 6C 7C 9E6C	dd ff ff	4 1 1 4 3 5

5.3 Reset and System Initialization

The MCU has these reset sources:

- Power-on reset module (POR)
- External reset pin ($\overline{RST}$)
- Computer operating properly module (COP)
- Low-voltage inhibit module (LVI)
- Illegal opcode
- Illegal address

All of these resets produce the vector $FFFE–$FFFF ($FEFE–$FEFF in Monitor mode) and assert the internal reset signal (IRST). IRST causes all registers to be returned to their default values and all modules to be returned to their reset states.

An internal reset clears the SIM counter (see 5.4 SIM Counter), but an external reset does not. Each of the resets sets a corresponding bit in the reset status register (RSR). (See 5.7 SIM Registers.)

5.3.1 External Pin Reset

The $\overline{RST}$ pin circuits include an internal pull-up device. Pulling the asynchronous $\overline{RST}$ pin low halts all processing. The PIN bit of the reset status register (RSR) is set as long as $\overline{RST}$ is held low for a minimum of 67 2OSCOUT cycles, assuming that the POR was not the source of the reset. See Table 5-2 for details. Figure 5-4 shows the relative timing.

Table 5-2. PIN Bit Set Timing

Reset Type	Number of Cycles Required to Set PIN
POR	4163 (4096 + 64 + 3)
All others	67 (64 + 3)

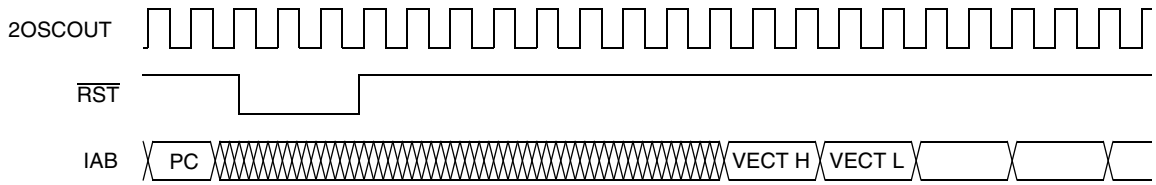


Figure 5-4. External Reset Timing

5.3.2 Active Resets from Internal Sources

All internal reset sources actively pull the $\overline{RST}$ pin low for 32 2OSCOUT cycles to allow resetting of external peripherals. The internal reset signal IRST continues to be asserted for an additional 32 cycles (Figure 5-5). An internal reset can be caused by an illegal address, illegal opcode, COP time-out, or POR. (See Figure 5-6.) Note that for POR resets, the SIM cycles through 4096 2OSCOUT cycles during which the SIM forces the $\overline{RST}$ pin low. The internal reset signal then follows the sequence from the falling edge of $\overline{RST}$ shown in Figure 5-5.

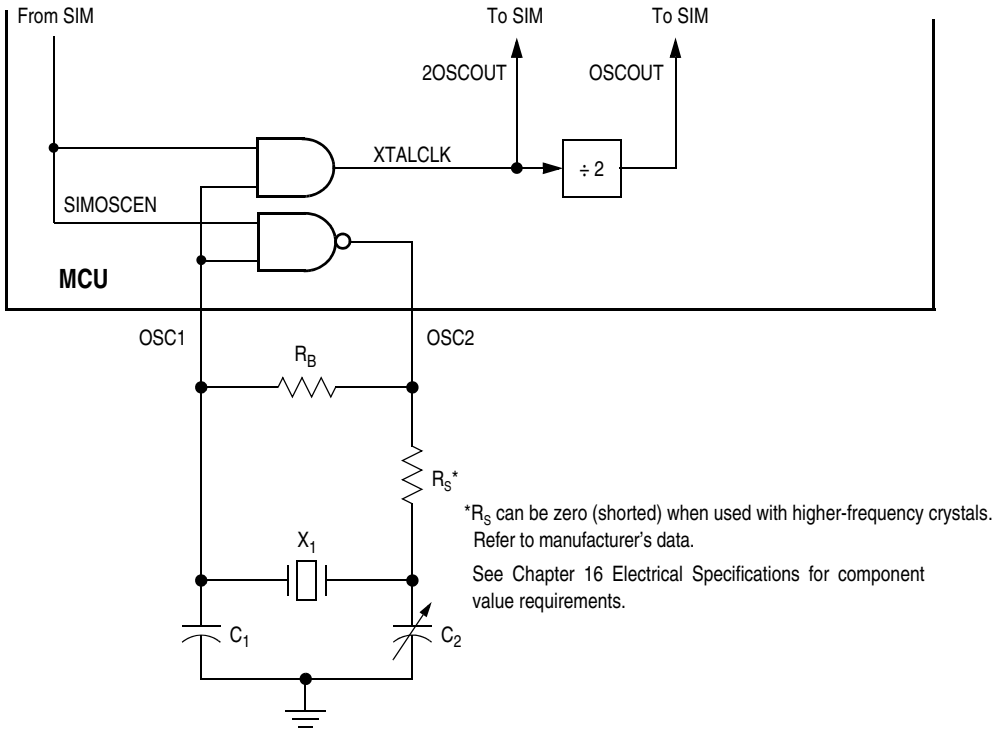


Figure 6-1. X-tal Oscillator External Connections

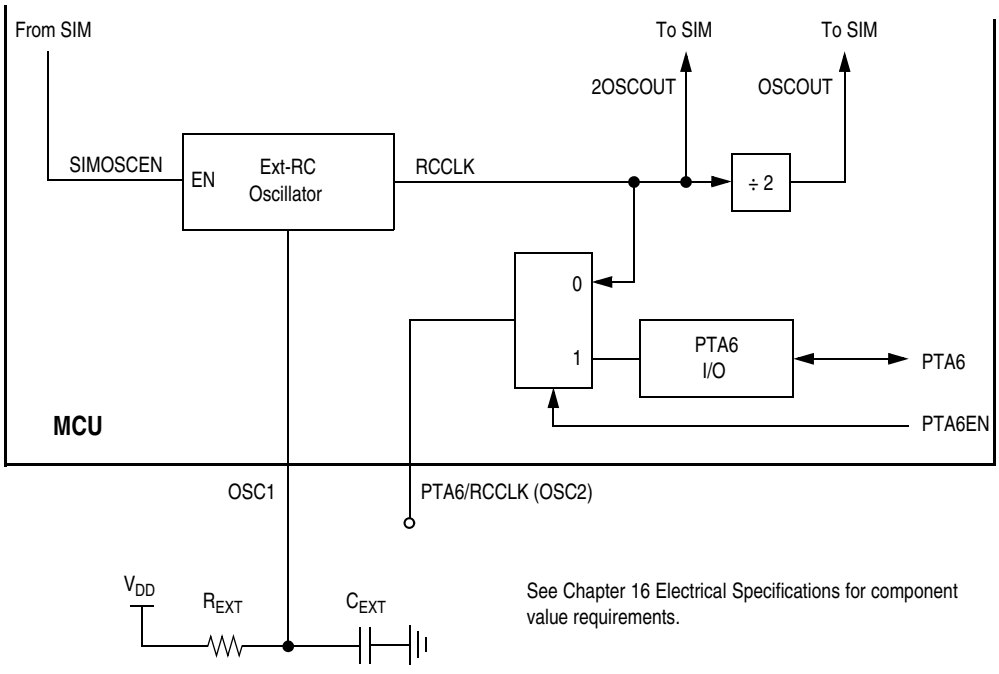


Figure 6-2. RC Oscillator External Connections

Table 7-2 is a summary of the vector differences between user mode and monitor mode.

Table 7-2. Monitor Mode Vector Differences

Modes	Functions						
	COP	Reset Vector High	Reset Vector Low	Break Vector High	Break Vector Low	SWI Vector High	SWI Vector Low
User	Enabled	$FFFE	$FFFF	$FFFC	$FFFD	$FFFC	$FFFD
Monitor	Disabled(1)	$FEFE	$FEFF	$FEFC	$FEFD	$FEFC	$FEFD

1. If the high voltage (V_{TST}) is removed from the $\overline{IRQ}$ pin or the $\overline{RST}$ pin, the SIM asserts its COP enable output. The COP is a mask option enabled or disabled by the COPD bit in the configuration register.

When the host computer has completed downloading code into the MCU RAM, the host then sends a RUN command, which executes an RTI, which sends control to the address on the stack pointer.

7.3.2 Baud Rate

The communication baud rate is dependant on oscillator frequency. The state of PTB3 also affects baud rate if entry to monitor mode is by $\overline{IRQ}$ = V_{TST}. When PTB3 is high, the divide by ratio is 1024. If the PTB3 pin is at logic zero upon entry into monitor mode, the divide by ratio is 512.

Table 7-3. Monitor Baud Rate Selection

Monitor Mode Entry By:	Input Clock Frequency	PTB3	Baud Rate
$\overline{IRQ}$ = V_{TST}	4.9152 MHz	0	9600 bps
	9.8304 MHz	1	9600 bps
	4.9152 MHz	1	4800 bps
Blank reset vector, $\overline{IRQ}$ = V_{DD}	9.8304 MHz	X	9600 bps
	4.9152 MHz	X	4800 bps

10.2.2 Data Direction Register A (DDRA)

Data direction register A determines whether each port A pin is an input or an output. Writing a one to a DDRA bit enables the output buffer for the corresponding port A pin; a zero disables the output buffer.

Address: $0004

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	0	DDRA6	DDRA5	DDRA4	DDRA3	DDRA2	DDRA1	DDRA0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 10-3. Data Direction Register A (DDRA)

DDRA[6:0] — Data Direction Register A Bits

These read/write bits control port A data direction. Reset clears DDRA[6:0], configuring all port A pins as inputs.

1 = Corresponding port A pin configured as output
0 = Corresponding port A pin configured as input

NOTE

Avoid glitches on port A pins by writing to the port A data register before changing data direction register A bits from 0 to 1.

Figure 10-4 shows the port A I/O logic.

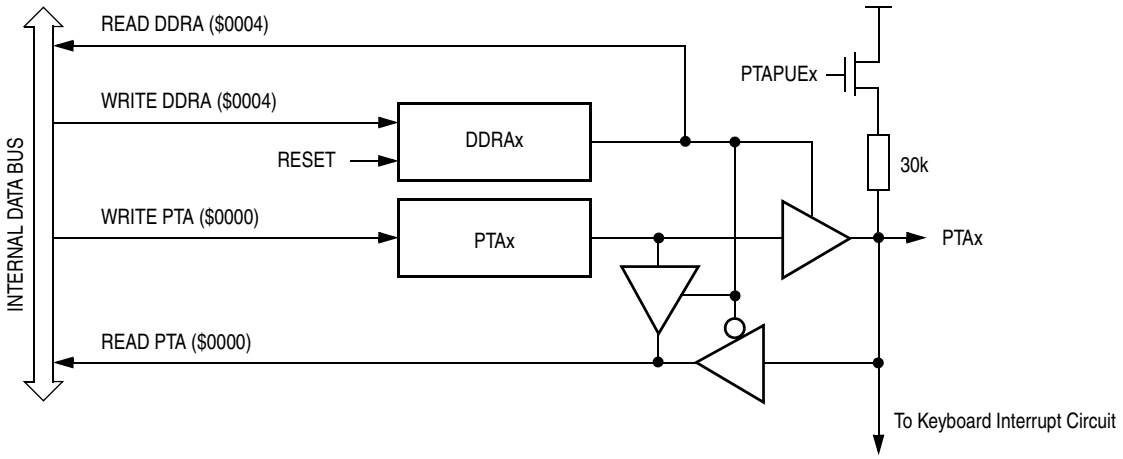


Figure 10-4. Port A I/O Circuit

When DDRAx is a 1, reading address $0000 reads the PTAx data latch. When DDRAx is a 0, reading address $0000 reads the voltage level on the pin. The data latch can always be written, regardless of the state of its data direction bit.

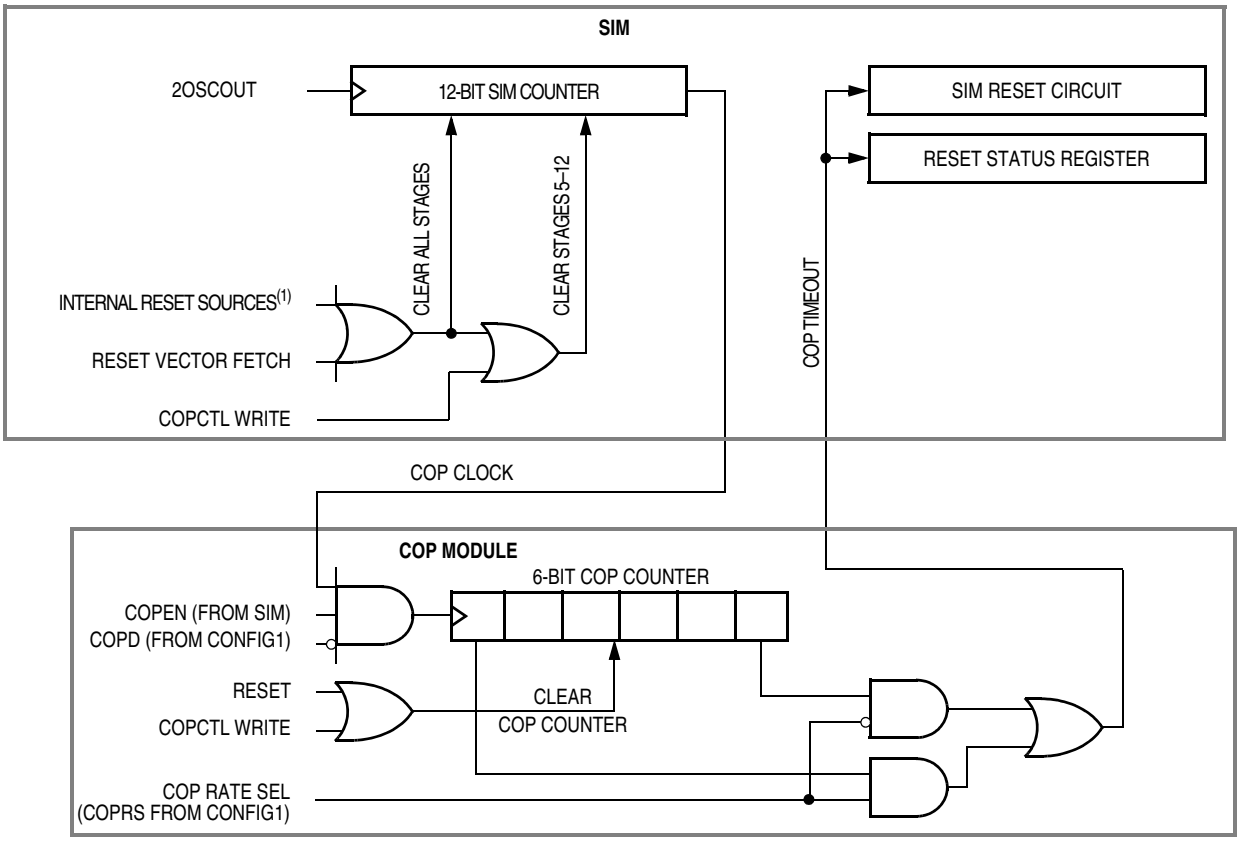
Chapter 13
Computer Operating Properly (COP)

13.1 Introduction

The computer operating properly (COP) module contains a free-running counter that generates a reset if allowed to overflow. The COP module helps software recover from runaway code. Prevent a COP reset by clearing the COP counter periodically. The COP module can be disabled through the COPD bit in the CONFIG1 register.

13.2 Functional Description

Figure 13-1 shows the structure of the COP module.



NOTE: See Chapter 5 System Integration Module (SIM) for more details.

Figure 13-1. COP Block Diagram

15.4 Break Module Registers

These registers control and monitor operation of the break module:

- Break status and control register (BRKSCR)
- Break address register high (BRKH)
- Break address register low (BRKL)
- Break status register (BSR)
- Break flag control register (BFCR)

15.4.1 Break Status and Control Register (BRKSCR)

The break status and control register contains break module enable and status bits.

Address: $FE0E

	Bit 7	6	5	4	3	2	1	Bit 0
Read:	BRKE	BRKA	0	0	0	0	0	0
Write:								
Reset:	0	0	0	0	0	0	0	0

= Unimplemented

Figure 15-3. Break Status and Control Register (BRKSCR)

BRKE — Break Enable Bit

This read/write bit enables breaks on break address register matches. Clear BRKE by writing a zero to bit 7. Reset clears the BRKE bit.

1 = Breaks enabled on 16-bit address match
0 = Breaks disabled

BRKA — Break Active Bit

This read/write status and control bit is set when a break address match occurs. Writing a one to BRKA generates a break interrupt. Clear BRKA by writing a zero to it before exiting the break routine. Reset clears the BRKA bit.

1 = Break address match
0 = No break address match

15.4.4 Break Flag Control Register (BFCR)

The break control register contains a bit that enables software to clear status bits while the MCU is in a break state.

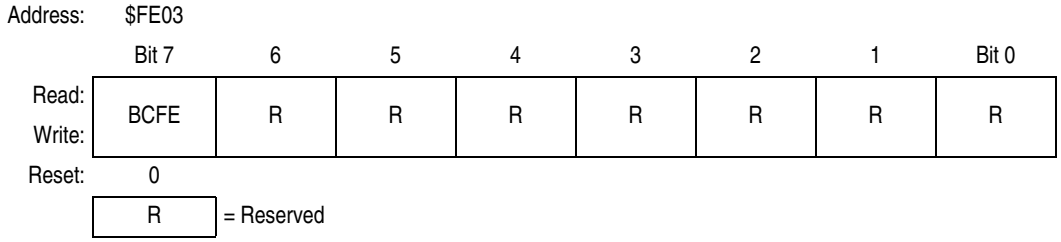


Figure 15-7. Break Flag Control Register (BFCR)

BCFE — Break Clear Flag Enable Bit

This read/write bit enables software to clear status bits by accessing status registers while the MCU is in a break state. To clear status bits during the break state, the BCFE bit must be set.

1 = Status bits clearable during break
0 = Status bits not clearable during break

15.5 Low-Power Modes

The WAIT and STOP instructions put the MCU in low-power-consumption standby modes.

15.5.1 Wait Mode

If enabled, the break module is active in wait mode. In the break routine, the user can subtract one from the return address on the stack if SBSW is set (see 5.6 Low-Power Modes). Clear the SBSW bit by writing zero to it.

15.5.2 Stop Mode

A break interrupt causes exit from stop mode and sets the SBSW bit in the break status register. See 5.7 SIM Registers.

16.7 5V Oscillator Characteristics

Table 16-6. Oscillator Component Specifications (5V)

Characteristic	Symbol	Min	Typ	Max	Unit
Crystal frequency, XTALCLK	$f_{OSCXCLK}$	—	10	32	MHz
RC oscillator frequency, RCCLK	f_{RCCLK}	2	10	12	MHz
External clock reference frequency(1)	$f_{OSCXCLK}$	dc	—	32	MHz
Crystal load capacitance(2)	C_L	—	—	—	
Crystal fixed capacitance(2)	C_1	—	$2 \times C_L$	—	
Crystal tuning capacitance(2)	C_2	—	$2 \times C_L$	—	
Feedback bias resistor	R_B	—	10 MΩ	—	
Series resistor(2), (3)	R_S	—	—	—	
RC oscillator external R	R_{EXT}	See Figure 16-1			
RC oscillator external C	C_{EXT}	—	10	—	pF

1. No more than 10% duty cycle deviation from 50%.
2. Consult crystal vendor data sheet.
3. Not required for high frequency crystals.

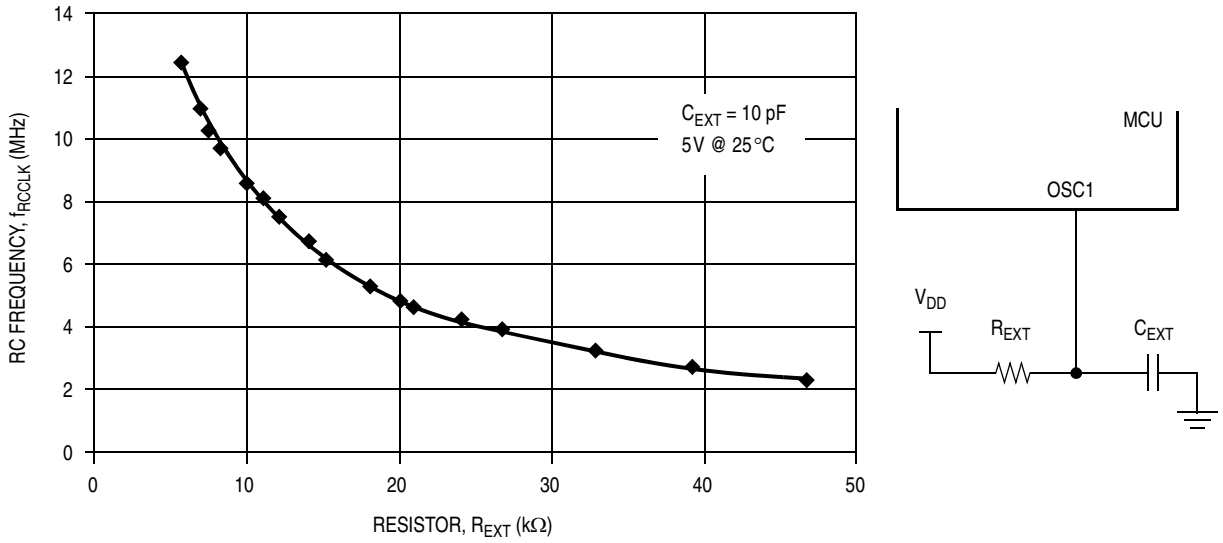


Figure 16-1. RC vs. Frequency (5V @25°C)

Chapter 17
Mechanical Specifications

17.1 Introduction

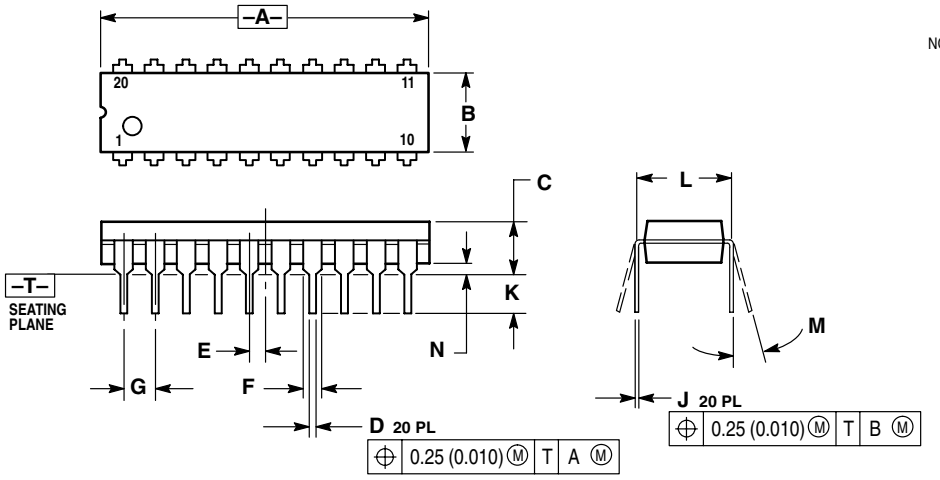
This section gives the dimensions for:

- 20-pin plastic dual in-line package (case #738)
- 20-pin small outline integrated circuit package (case #751D)
- 28-pin plastic dual in-line package (case #710)
- 28-pin small outline integrated circuit package (case #751F)
- 48-pin low-profile quad flat pack (case #932)

The following figures show the latest package drawings at the time of this publication. To make sure that you have the latest package specifications, contact your local Freescale Sales Office.

17.2 Package Dimensions

Refer to the following pages for detailed package dimensions.



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEAD WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	1.010	1.070	25.66	27.17
B	0.240	0.260	6.10	6.60
C	0.150	0.180	3.81	4.57
D	0.015	0.022	0.39	0.55
E	0.050 BSC		1.27 BSC	
F	0.050	0.070	1.27	1.77
G	0.100 BSC		2.54 BSC	
J	0.008	0.015	0.21	0.38
K	0.110	0.140	2.80	3.55
L	0.300 BSC		7.62 BSC	
M	0°	15°	0°	15°
N	0.020	0.040	0.51	1.01

20-Pin PDIP (Case #738)

NOTES:

1. DIMENSIONS ARE IN MILLIMETERS.

2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M–1994.

3. THIS DIMENSION DOES NOT INCLUDE MOLD PROTRUSION. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.

4. 751F–01 THRU –04 OBSOLETE. NEW STANDARD: 751F–05

5. THIS DIMENSION DOES NOT INCLUDE DAM BAR PROTRUSION ALLOWABLE DAM BAR PROTRUSION SHALL BE 0.13 TOTAL IN EXCESS OF THIS DIMENSION AT MAXIMUM MATERIAL CONDITION.

MECHANICAL OUTLINE	PRINT VERSION NOT TO SCALE

TITLE: SOIC, WIDE BODY, 28 LEAD CASEOUTLINE	DOCUMENT NO: 98ASB42345B	REV: G
	CASE NUMBER: 751F–05	10 MAR 2005
	STANDARD: MS–013AE	

A.5.5 ADC Characteristics

Table A-5. ADC Characteristics

Characteristic	Symbol	Min	Max	Unit	Comments
Supply voltage	V_{DDAD}	2.2 (V_{DD} min)	5.5 (V_{DD} max)	V	
Input voltages	V_{ADIN}	V_{SS}	V_{DD}	V	
Resolution	B_{AD}	8	8	Bits	
Absolute accuracy	A_{AD}	± 0.5	± 2	LSB	Includes quantization
ADC internal clock	f_{ADIC}	0.5	1.048	MHz	$t_{AIC} = 1/f_{ADIC}$, tested only at 1 MHz
Conversion range	R_{AD}	V_{SS}	V_{DD}	V	
Power-up time	t_{ADPU}	14	—	t_{AIC} cycles	
Conversion time	t_{ADC}	14	15	t_{AIC} cycles	
Sample time[1]	t_{ADS}	5	—	t_{AIC} cycles	
Zero input reading[2]	Z_{ADI}	00	01	Hex	$V_{IN} = V_{SS}$
Full-scale reading[3]	F_{ADI}	FE	FF	Hex	$V_{IN} = V_{DD}$
Input capacitance	C_{ADI}	—	(20) 8	pF	Not tested
Input leakage[3] Port B/port D	—	—	± 1	μA	

1. Source impedances greater than 10 kΩ adversely affect internal RC charging time during input sampling.
2. Zero-input/full-scale reading requires sufficient decoupling measures for accurate conversions.
3. The external system error caused by input leakage current is approximately equal to the product of R source and input current.

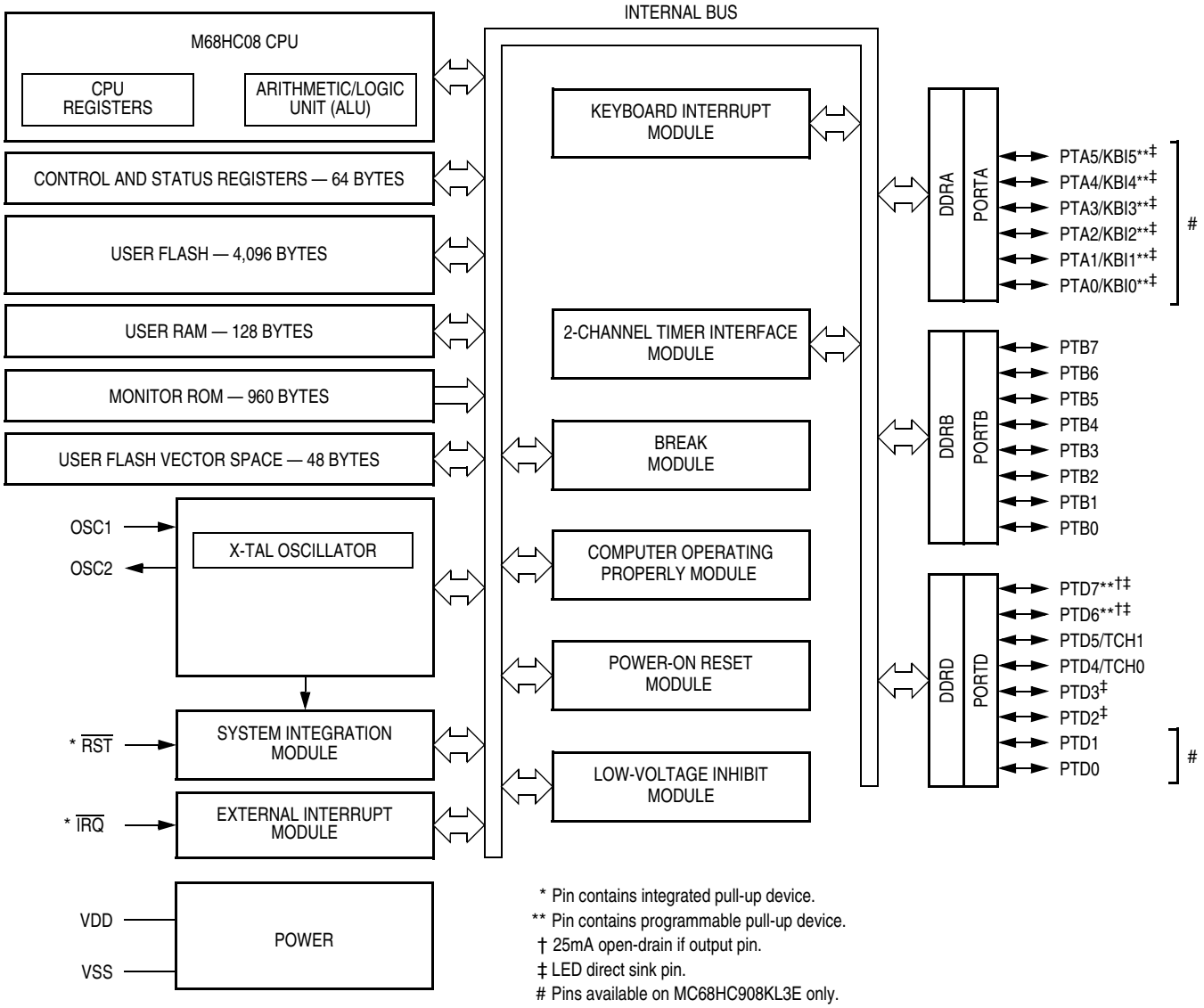


Figure C-1. MC68HC908KL3E/KK3E Block Diagram